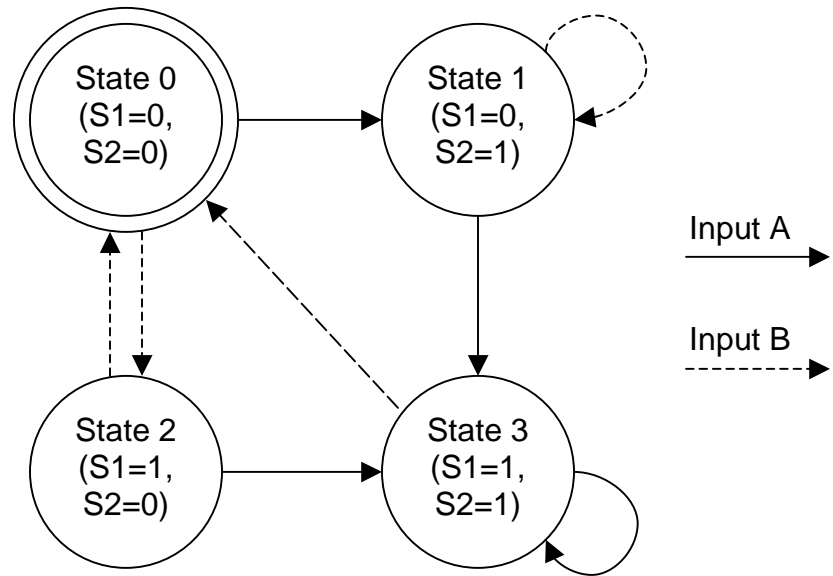


(state diagram for problem 9)



10. Datapath control (10 points):

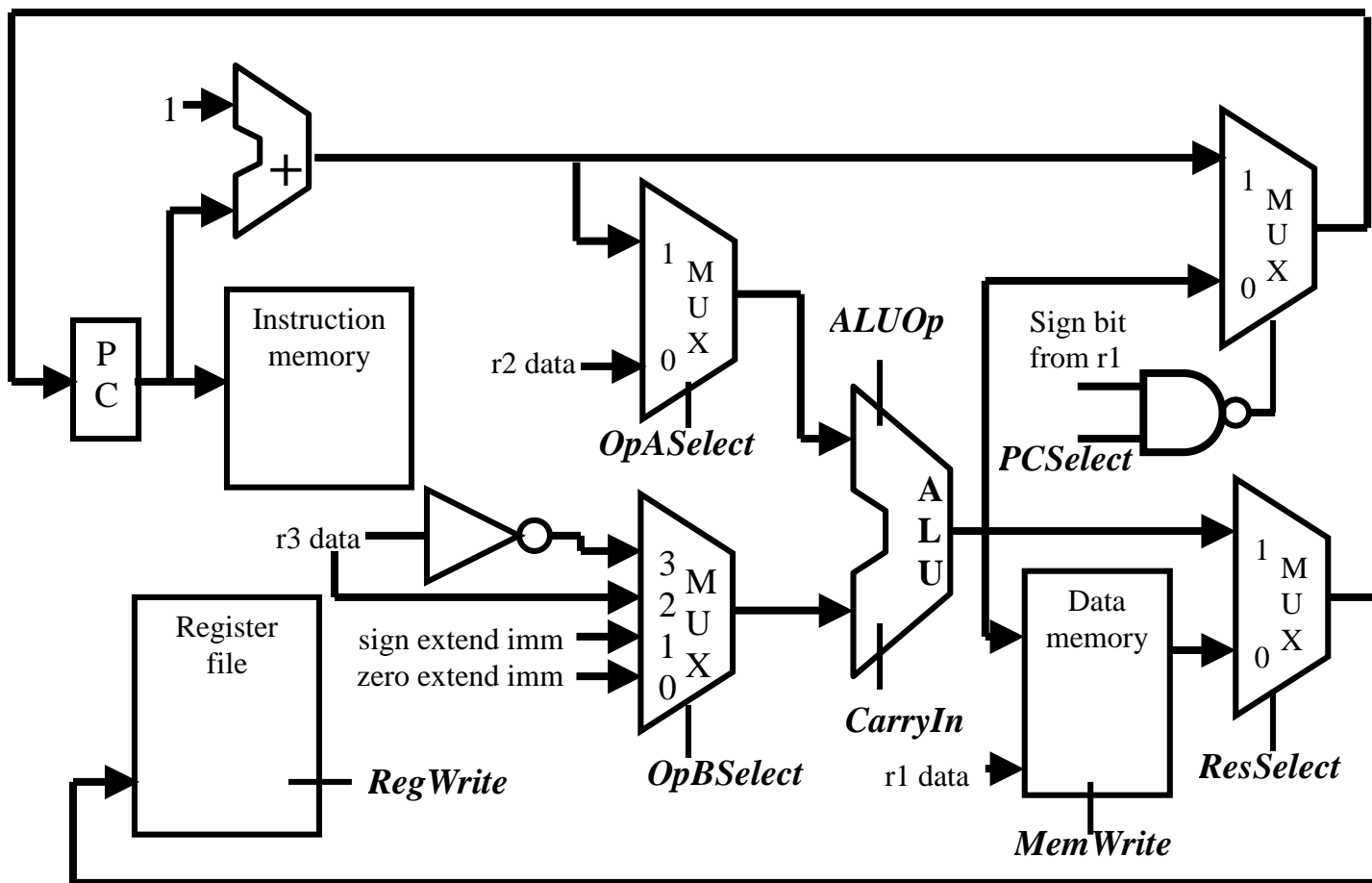
Imagine you are on the design team for a processor that implements a new instruction set called the E370. There are eight instructions:

Instruction	Semantics	Description
add r1, r2, r3	$r1 = r2 + r3$	Places the sum of r2 and r3 into r1.
addi r1, r2, imm	$r1 = r2 + \text{imm}$	Places the sum of r2 and the immediate value into r1. The immediate value should be treated as a signed two's complement number.
sub r1, r2, r3	$r1 = r2 - r3$	Places the difference $r2 - r3$ into r1.
and r1, r2, r3	$r1 = r2 \& r3$	Places the result of the bitwise and of r2 and r3.
andiu r1, r2, imm	$r1 = r2 \& \text{imm}$	Places the result of the bitwise and of r2 and the immediate value. The immediate value should be treated as an unsigned value.
lw r1, r2(imm)	$r1 = M[r2 + \text{imm}]$	Loads the value at memory address $r2 + \text{imm}$ into r1.
sw r1, r2(imm)	$M[r2 + \text{imm}] = r1$	Stores the value of r1 at memory address $r2 + \text{imm}$.
bltz r1, imm	if ($r1 < 0$) $PC = PC + 1 + \text{imm}$	If the value of r1 is less than zero, branch to $PC + 1 + \text{imm}$ (PC-relative branch).

Some useful information about the E370:

- The E370 is a 32-bit machine and is word addressable.
- The displacement field for addi, andiu, lw, sw, and bltz is 16 bits.
- For the “andiu” instruction, the immediate should be treated as an unsigned value. For all other instructions, the immediate field should be treated as a signed two's complement number.
- The ALU has two modes of operation determined by the control line *ALUOp*: 0 is add, 1 is bitwise-and. If bitwise-and is selected, the *CarryIn* line is ignored.

On the following page is a diagram of the single-cycle datapath for the E370. For clarity, the decoding of the instruction and the register file output lines are not shown. Your job is to determine the value of each control signal for each instruction. Indicate don't care conditions using the letter 'X'.



<i>Instruction</i>	<i>OpASelect</i> (1 bit)	<i>OpBSelect</i> (2 bits)	<i>ALUOp</i> (1 bit)	<i>CarryIn</i> (1 bit)	<i>MemWrite</i> (1 bit)	<i>ResSelect</i> (1 bit)	<i>PCSelect</i> (1 bit)	<i>RegWrite</i> (1 bit)
Add								
Addi								
Sub								
And								
Andiu								
Lw								
Sw								
Bltz								