

Midterm Examination

Instructions

1. This is a **closed book/notes** examination.
2. Record your answers on the answer sheet provided.
3. Each multiple choice question has a single correct answer.
4. Each question in Part 1 of the exam is worth 2 points.
5. Each question in Part 2 of the exam is worth 3 points.
6. This examination has 100 points total.

Name:

Student ID:

Student email address:

Honor Pledge:

Do not write below this line.

1. Part 1: _____ (out of 40 points)

2. Part 2: _____ (out of 60 points)

Total _____ (out of 100 points)

Part 1: Multiple Choice (2 points each)

Question 1. Which of the following is NOT a MIPS addressing mode?

- (a) Base Displacement
- (b) PC-Relative
- (c) Immediate
- (d) Register
- (e) All of the above are MIPS addressing modes

Question 2. Which of the following addressing modes are used by an R-type instruction in MIPS?

- (a) Base Displacement
- (b) PC-Relative
- (c) Immediate
- (d) Register
- (e) None of the Above

Question 3. What is the advantage of a single-cycle implementation over a multicycle one?

- (a) Single-cycle implementation is faster, because it performs one instruction each cycle.
- (b) Single-cycle implementation supports more instructions.
- (c) Single-cycle implementation control requires no state and is thus simpler to implement.
- (d) A, B, and C are correct.
- (e) A, B, and C are incorrect.

Question 4. What does Amdahl's law say:

- (a) Execution time = Instruction Count * CPI / MHz
- (b) Performance improvement is limited by the amount the improved feature is used.
- (c) The clock frequency of a processor is determined by the speed of performing an integer addition.
- (d) Processor performance approximately doubles every 18 months.
- (e) Internet companies stocks valuations approximately double every 18 months.

Question 5. I-type instructions in MIPS can specify AT MOST how many registers in the instruction?

- (a) 0
- (b) 1
- (c) 2
- (d) 3
- (e) More than 3

Question 6. Which of the following is not allocated to an activation record:

- (a) Parameters to a function
- (b) Registers saved by caller
- (c) Registers saved by callee
- (d) Return address
- (e) Static local variables

Question 7. Use the grammar school method to multiply the following two numbers: The multiplier is 00001101 and the multiplicand is 00111101. How many adds are needed?

- (a) 1
- (b) 3
- (c) 4
- (d) 8
- (e) 9

Question 8. If you are using Booth's algorithm to multiply two 8-bit numbers together and the multiplier is 00110110 and the multiplicand is 11110100, how many subtractions are needed?

- (a) 1
- (b) 2
- (c) 6
- (d) 7
- (e) 8

Question 9. Convert 15 to IEEE 754 floating point representation.

- (a) 0 10000010 111000000000000000000000
- (b) 0 10000010 111100000000000000000000
- (c) 0 00000011 111000000000000000000000
- (d) 0 00000011 111100000000000000000000
- (e) 1 00000011 111000000000000000000000

Question 10. In which type of datapath does the instruction with the FASTEST execution time determine the cycle time?

- (a) Never
- (b) All datapaths
- (c) In single-cycle datapath only
- (d) In multicycle datapath only
- (e) Depends on the program's CPI

Question 11. How many different numbers can be represented in IEEE 754 single precision floating point representation?

- (a) 65536
- (b) about 1 million
- (c) about 4 billion
- (d) about 2 to the power of 128
- (e) infinite

Question 12. Given a multi-cycle datapath like that discussed in class, which of the following instructions would need the most cycles to complete execution?

- (a) LW (load word)
- (b) SW (store word)
- (c) BEQ (branch if equal)
- (d) ADD (add)
- (e) J (jump)

Question 13. Which of the following is the best measure of performance for a microprocessor running a sequence of instructions?

- (a) MHz
- (b) execution time
- (c) MIPS
- (d) cycles per instruction
- (e) MFLOPS

Question 14. What is the largest number representable in IEEE754 Float Point?

- (a) $1.111111111111111111111111 * 2^{23}$
- (b) $1.111111111111111111111111 * 2^{127}$
- (c) $1.111111111111111111111111 * 2^{128}$
- (d) $1.111111111111111111111111 * 2^{255}$
- (e) infinity

Question 15. In a MIPS I-type instruction, the offset field is 16 bits. What is the range of addresses, relative to the PC, that a branch instruction can jump to?

- (a) 2^{15}
- (b) 2^{16}
- (c) 2^{18}
- (d) 2^{20}
- (e) 2^{32}

Question 16. Under the saving/restoring convention callee-save:

- I. The callee saves registers.
- II. The caller restores registers.
- III. The callee restores registers.
- IV. The caller assumes its registers are unchanged by the call.
- V. The callee assumes its registers are unchanged by the call.

- (a) I, II
- (b) I, III
- (c) I, II, V
- (d) I, III, IV
- (e) I, III, V

Question 17. What instruction does the datapath in Figure 1 most closely correspond to?

- (a) JALR
- (b) LW
- (c) SW
- (d) BEQ
- (e) ADD

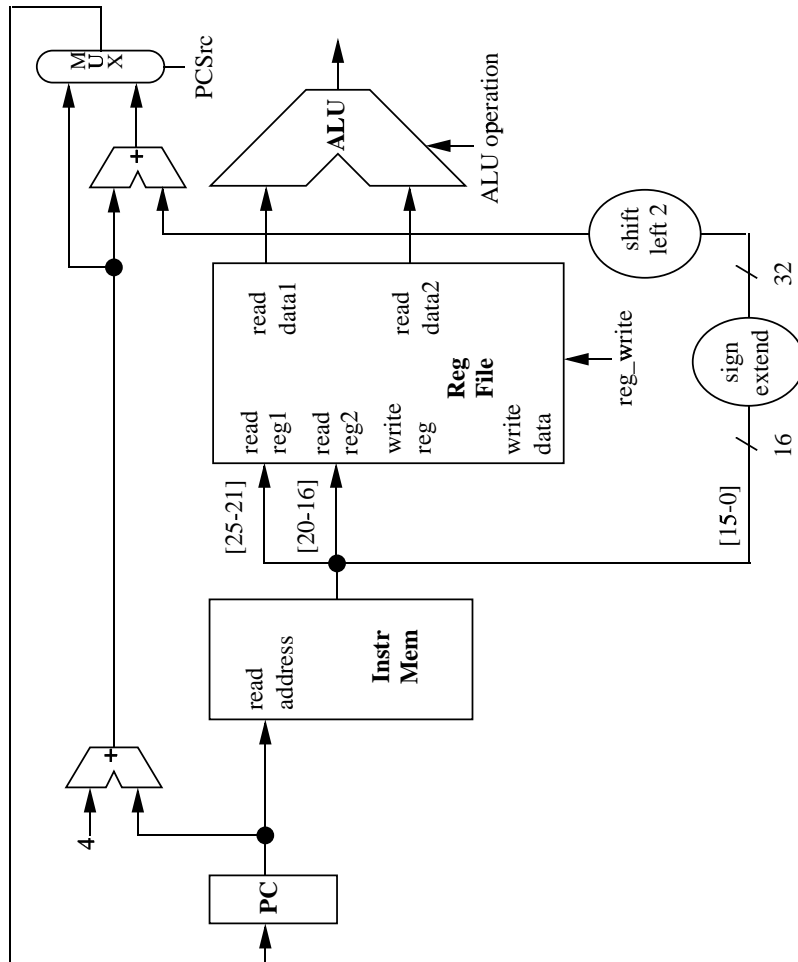


Figure 1: Datapath

Given a machine with the following state (for questions 18–20):

$Reg[0] = 0x0000$	$Mem[03] = 0x0007$	$Mem[8a] = 0x092A$	
$Reg[1] = 0x0004$	$Mem[04] = 0x008B$	$Mem[8b] = 0x008F$	
$Reg[2] = 0x008F$	$Mem[05] = 0x0681$	$Mem[8c] = 0x061B$	
$Reg[3] = 0x008E$	$Mem[06] = 0x7084$	$Mem[8d] = 0x0090$	
$Reg[4] = 0x0005$	$Mem[07] = 0x0005$	$Mem[8e] = 0x0006$	
$Reg[5] = 0x0006$	$Mem[08] = 0x008A$	$Mem[8f] = 0x008A$	
$Reg[6] = 0x008D$	$Mem[09] = 0x008B$	$Mem[90] = 0x0008$	
$Reg[7] = 0x008C$	$Mem[0A] = 0x008A$	$Mem[91] = 0x0718$	$Mem[92] = 0x0681$

Question 18. $M[M[\$1]] + 3$

- (a) 0x0681
- (b) 0x0784
- (c) 0x0092
- (d) 0x0718
- (e) Can't tell from the information provided

Question 19. $M[M[4 + \$5] + 3]$

- (a) 0x0090
- (b) 0x7084
- (c) 0x0008
- (d) 0x0681
- (e) Can't tell from the information provided

Question 20. $M[M[\$4 + 3] + M[M[3]]]$

- (a) 0x092A
- (b) 0x000A
- (c) 0x061B
- (d) 0x008A
- (e) Can't tell from the information provided

Part 2: Multiple Choice (3 points each)

Question 21. Which MIPS instruction type uses bits 31-26 as the opcode, bits 25-21 as operandA, bits 20-16 as operandB and bits 15-0 as an offset?

- (a) O-type
- (b) W-type
- (c) T-type
- (d) I-type
- (e) R-type

Question 22. Which of the following is the CPU time performance measurement equation?

- (a) $CPUtime = CPI * InstructionCount * CycleTime$
- (b) $CPUtime = CycleTime / CPI * 1000000$
- (c) $CPUtime = SpeedUp * InstructionCount * CycleTime / MIPS$
- (d) $CPUtime = InstructionCount * CycleTime / CPI$
- (e) None of the above

Question 23. The MIPS instruction `addi 1 2 10` needs a MINIMUM of how many LC-2K instructions to execute? (Hint: Do NOT count `.fills` as instructions.)

- (a) 1
- (b) 2
- (c) 3
- (d) 4
- (e) Can't be done with LC-2K

Question 24. Which addressing mode is most useful in referencing local variables?

- (a) Direct
- (b) Indirect
- (c) Base + Displacement
- (d) PC-Relative
- (e) Immediate

Question 25. Which of the following can never generate an overflow given two 16-bit numbers A and B ?

- (a) $A + B$ if $A \geq 0$ and $B \geq 0$
- (b) $A - B$ if $A < 0$ and $B \geq 0$
- (c) $A - B$ if $A \geq 0$ and $B < 0$
- (d) $A + B$ if $A < 0$ and $B > 0$
- (e) None of the above

Question 26. One advantage of a multicycle datapath vs. a single-cycle datapath is that the multicycle datapath:

- (a) Uses fewer registers to hold state information
- (b) Has simpler control logic (fewer control signals)
- (c) Uses smaller multiplexors
- (d) Requires just one ALU
- (e) None of the above

Question 27. If a computer, running at 500 MHz, takes 24 microseconds to execute a program with a dynamic instruction count of 750, what is the average CPI for this program?

- (a) 1.5
- (b) 5.0
- (c) $(500 * 750) / 24$
- (d) $(750 * 24) / 500$
- (e) $(500 * 24) / 750$

Question 28. With Base + Displacement Addressing, which of the following notations represents the MIPS instruction `ld 5 2 3`?

- (a) $\text{reg}[5] = \text{mem}[\text{reg}[2] + 3]$
- (b) $\text{reg}[5] = \text{mem}[2] + 3$
- (c) $\text{reg}[5] = \text{mem}[2] + \text{reg}[3]$
- (d) $\text{reg}[5] = \text{reg}[2] + \text{mem}[3]$
- (e) $\text{reg}[5] = \text{mem}[2 + 3]$

Question 29. Machine M1 executes instruction A in 10 cycles and instruction B in 20 cycles. Machine M2 reduces the execution of instruction B to 10 cycles but increases clock cycle time by 10%. For a standard program with 1000 instructions A and 200 instructions B, which machine executes faster?

- (a) M1
- (b) M2
- (c) They both run at the same speed
- (d) Not enough information
- (e) Depends on the order of the instructions in the program

Question 30. What is the correct order of operations (from left to right) to translate a C program into a runnable program?

- (a) compile, link, assemble, load
- (b) assemble, load, link, compile
- (c) load, compile, assemble, link
- (d) link, load, compile, assemble
- (e) compile, assemble, link, load

Question 31. Why do most microprocessors use 2's complement form to represent negative numbers?

- (a) To detect overflow conditions.
- (b) To simplify addition and subtraction.
- (c) To reduce the need for sign extension.
- (d) To save bits on the data bus.
- (e) To confuse EECS 370 students.

Question 32. What is the amount of time that it takes for a carry-lookahead adder to perform an addition, where n is the number of bits?

- (a) $O(n^2)$
- (b) $O(\sqrt{n})$
- (c) $O(\log n)$
- (d) $O(n)$
- (e) $O(n!)$

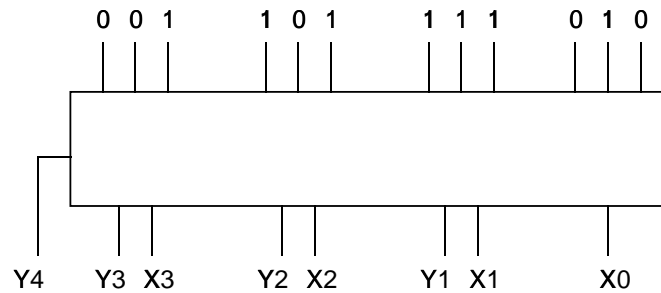


Figure 2: Carry-save structure

Question 33. Consider the carry-save structure in Figure 2. This structure that converts the three 4-bit numbers 0110, 0011, 1110 into two 5-bit numbers $Y_4 Y_3 Y_3 Y_1 0$ and $0 X_3 X_2 X_1 X_0$ with the same sum. What are the bits Y_2 and X_1 ?

- (a) $Y_2 = 0, X_1 = 0$
- (b) $Y_2 = 0, X_1 = 1$
- (c) $Y_2 = 1, X_1 = 0$
- (d) $Y_2 = 1, X_1 = 1$
- (e) None of the above

Question 34. How many Carry-Save Adders does it take to build a 32-bit Wallace Multiplier?

- (a) 8
- (b) 14
- (c) 17
- (d) 24
- (e) 30

Question 35. Consider the multiplication of the binary numbers 1011 and 1011 using a Wallace Multiplier as described in class (the first-level CSA adding 000000, 010110, 001011). What are the two binary numbers at the input of the adder at the last stage of the multiplier?

- (a) 10111010, 11001010
- (b) 10000110, 11110000
- (c) 10101111, 01010101
- (d) 01000001, 00111000
- (e) 01111000, 00000001

Question 36. Consider the carry-lookahead adder in Figure 3. What are the values of X and Y?

Figure 3: Carry-lookahead

- (a) $X = 0, Y = 0$
- (b) $X = 1, Y = 1$
- (c) $X = 0, Y = c_0$
- (d) $X = 1, Y = c_0$
- (e) None of the above

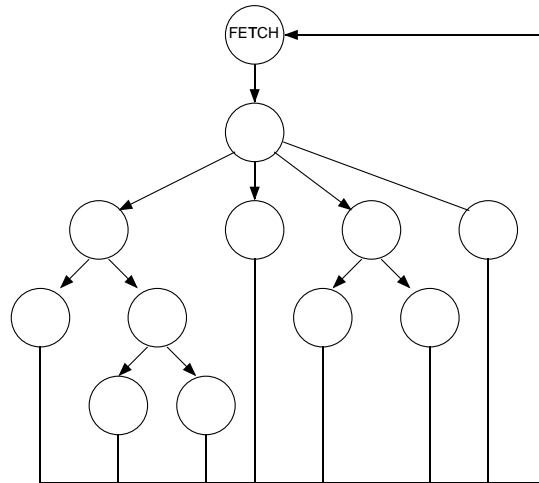


Figure 4: State diagram

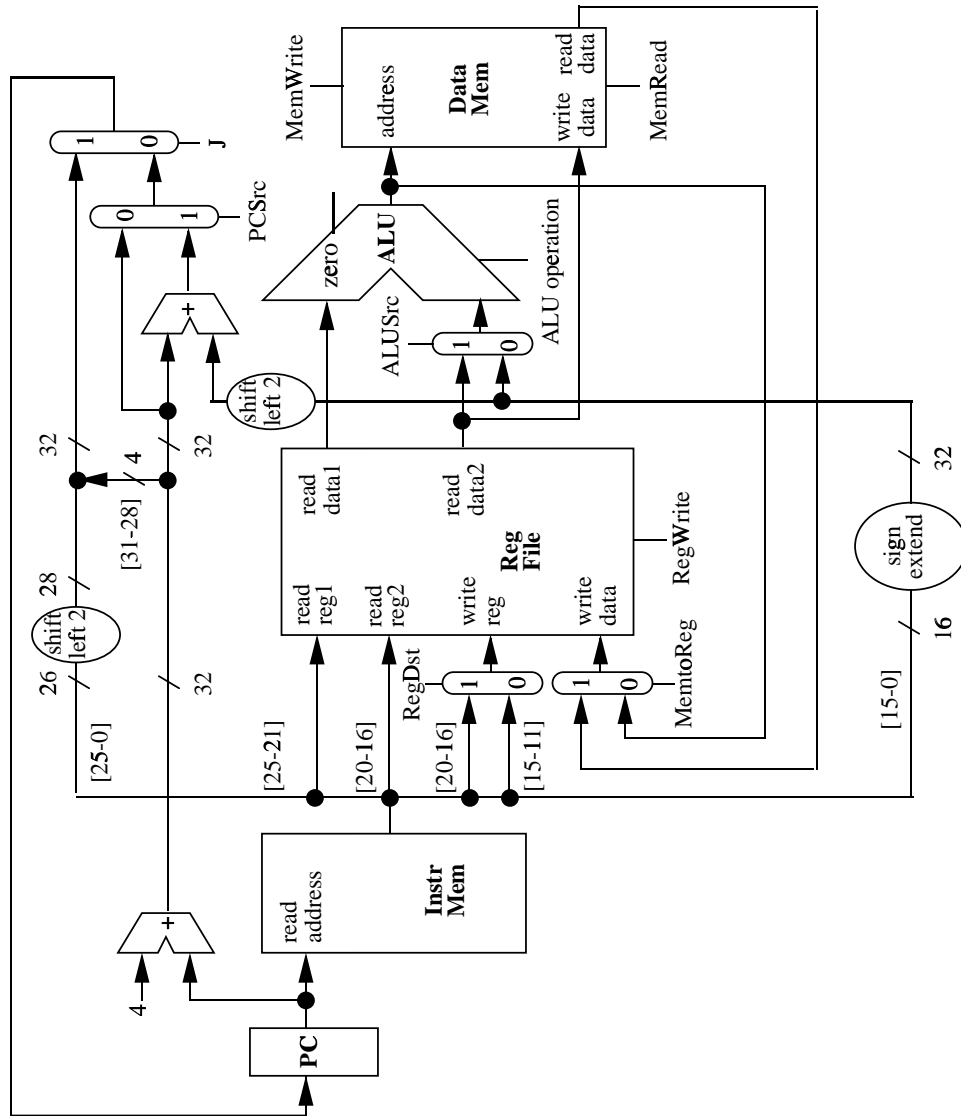
For questions 37 and 38, consider the state diagram in Figure 4 of a multicycle datapath FSM controller. Assume each node corresponds to one cycle in the datapath's execution.

Question 37. How many cycles does the longest instruction take?

- (a) 2
- (b) 3
- (c) 4
- (d) 5
- (e) 6

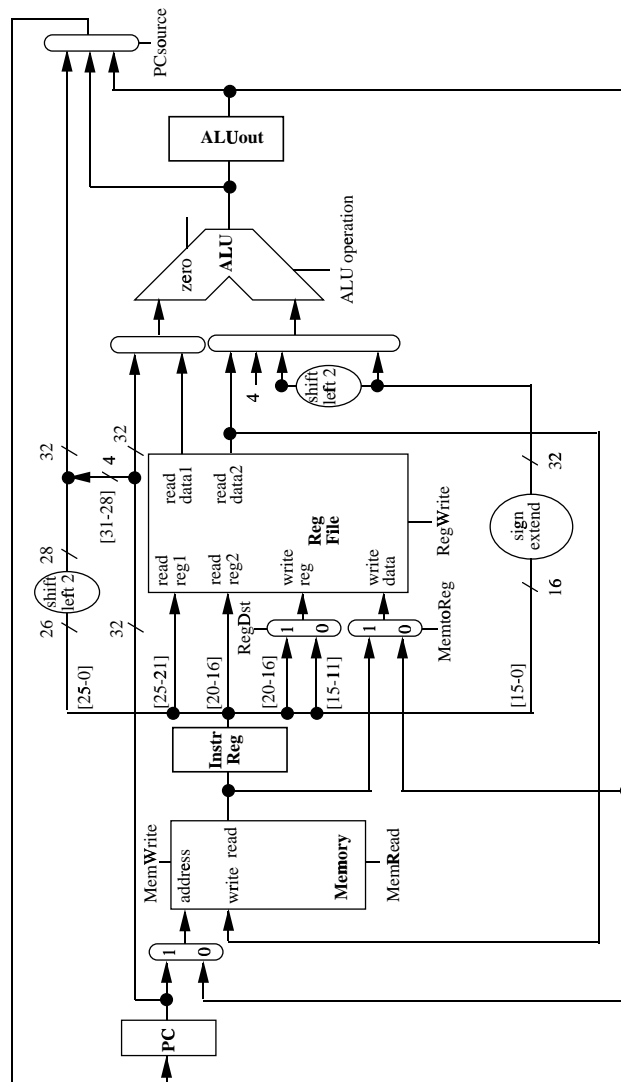
Question 38. In a microprogrammed implementation of this controller, how many dispatch tables would you need?

- (a) 1
- (b) 2
- (c) 3
- (d) 4
- (e) 5



Question 39. Consider the execution of an R-type instruction on the above single-cycle datapath. Among the following signals, pick the one that is safe to set to “don’t care”.

- (a) ALUSrc
- (b) PCSrc
- (c) MemWrite
- (d) MemRead
- (e) MemtoReg



Question 40. Consider the execution of a `sw` instruction on the above multicycle datapath. Among the following signals, pick the one that is safe to set to “don’t care” **throughout** the execution of the instruction.

- (a) MemRead
- (b) MemtoReg
- (c) RegDst
- (d) RegWrite
- (e) MemWrite