Second Midterm Examination

Instructions

1. This is a **closed book/notes** examination.
2. Record your answers on the answer sheet provided.
3. Each multiple choice question has a single correct answer.
4. Each question in Part 1 of the exam is worth 2 points.
5. Each question in Part 2 of the exam is worth 3 points.
6. This examination has 100 points total.

Name:

Student ID:

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1. Part 1: _____ (out of 40 points)
2. Part 2: _____ (out of 60 points)

Total _____ (out of 100 points)

Part 1: Multiple Choice (2 points each)

Question 1. All cache misses can be divided into these basic types:

(a) Component, Conflict, Compulsory

(b) Capacity, Conflict, Compulsory

(c) Conflict, Component, Capacity

(d) Capacity, Compulsory, Compound

(e) Component, Compulsory, Compound

Question 2. Increasing associativity generally reduces which type of cache miss?

(a) Component

(b) Capacity

(c) Conflict

(d) Compulsory

(e) Compound

Question 3. How many bits of the address are needed to index into a 4-way set-associative cache with 256 blocks?

(a) 6

(b) 8

(c) 64

(d) 128

(e) Can't tell from the information provided in the question.

For questions 4–9: Assume a cache with the following attributes:

```
WRITE POLICY:         Write Back
REPLACEMENT POLICY:   LRU
BLOCK SIZE:           16 bytes
CACHE BLOCKS:         8 blocks
CACHE SIZE:           128 bytes
ASSOCIATIVITY:        2-way associative
12-bit byte addressable addresses
```

Moreover, consider the following memory reference trace (assuming all blocks start out invalid):

```
reference 1: Write address 0100 0110 1111

reference 2: Read address  0100 1101 0000

reference 3: Read address  0100 1110 1001

reference 4: Write address 0100 1001 0011

reference 5: Write address 0100 1101 0011

reference 6: Read address  0100 1010 1101

reference 7: Write address 0100 0110 0111

reference 8: Write address 0100 0101 1100
```

Question 4. How many cache hits are there in this trace?

(a) 0

(b) 1

(c) 2

(d) 3

(e) 4 or more

Question 5. What is the tag of the block replaced when reference 8 misses?

(a) 0100 11

(b) 0100 10

(c) 0100 110

(d) 0100 100

(e) reference 8 was a hit in the cache.

Question 6. How many dirty blocks are evicted (don't count any dirty block remaining in the cache at the end of the trace)?

(a) 0

(b) 1

(c) 2

(d) 3

(e) 4 or more.

Question 7. At the end of the trace how many blocks are valid in the cache?

(a) 1

(b) 2

(c) 3

(d) 4

(e) more than 4

Question 8. What is the fewest number of bits required to implement the LRU algorithm in the cache?

(a) 2

(b) 4

(c) 8

(d) 16

(e) 32 or more.

Question 9. Not counting the LRU bits, how many BITS are required to construct the cache (including data, tags, etc.).

(a) 256

(b) 1024

(c) 1088

(d) 1152

(e) 2048

Question 10. What happens to the tag field as cache associativity increases?

(a) tag size increases

(b) tag size decreases

(c) tag bits are shifted left

(d) tag bits are shifted right

(e) tag remains unchanged

Figure 1: 5-stage pipeline.

For questions 11–14: Consider the following loop in MIPS assembly.

```
loop  lw   r3 A(r1)     # a
      lw   r4 B(r1)     # b
      add  r4 r3 r4     # c
      addi r1 r1 1      # d
      add  r2 r1 r1     # e
      add  r2 r2 r2     # f
      sw   r4 C(r2)     # g
      beq  r2 r5 loop   # h
```

Question 11. Assume the loop executes on the 5-stage pipeline shown in Figure 1. This pipeline has no forwarding to the EX stage and does not stall on load hazards. When a register is written/read on the same cycle, the read gets the value of the write. How many `noop` instructions need to be inserted in the original code to ensure its correct execution?

(a) 4

(b) 5

(c) 6

(d) 7

(e) None of the above

For questions 12–14: To reduce the number of `noop`'s required, forwarding is introduced from the EX/MEM and the MEM/WB registers to the EX stage. Assume the loop iterates 1 million times.

Question 12. If the penalty for each execution of the `beq` is 3 cycles, what is the program's CPI?

(a) 1

(b) 9/8

(c) 11/8

(d) 12/8

(e) 13/8

Question 13. If the branch penalty is reduced to 0 cycles, what is the program's CPI?

(a) 7/8

(b) 1

(c) 9/8

(d) 12/8

(e) None of the above

Question 14. Which of the following reorderings of the original code achieves the minimum CPI?

(a) abcefdgh

(b) acbdefgh

(c) abdcefgh

(d) abedcfhg

(e) bacdefgh

Figure 2: 5-stage pipeline with full forwarding and load hazard detection.

For questions 15–18: Consider the following piece of MIPS code.

```
add   r1 r2 r3
lw    r4 0(r1)
addi  r2 r1 1
lw    r5 0(r2)
add   r5 r5 r5
```

All registers are initialized to zero. Memory locations 0 and 1 are initialized to 1. The code executes on the 5-stage pipeline of Figure 2 with full forwarding, stalling at load hazards, and same-cycle write/read capability in the register file. The first instruction enters the pipeline on cycle 1.

Question 15. What are the contents of register `r4` at the end of cycle 6?

(a) 0

(b) 1

(c) 2

(d) 3

(e) Cannot tell from the given information

Question 16. On which cycle is register `r2` updated in the register file?

(a) 3

(b) 4

(c) 5

(d) 6

(e) 7

Question 17. What are the contents of register `r5` at the end of cycle 9?

(a) 0

(b) 1

(c) 2

(d) 3

(e) Cannot tell from the given information

Question 18. What is the total number of cycles taken to execute this code all the way until the completion of the last instruction?

(a) 8

(b) 9

(c) 10

(d) 11

(e) 12

Question 19. Which of the following hazards CANNOT be eliminated with forwarding?

I. load followed by add

II. load followed by load

III. add followed by load

IV. add followed by add

(a) I

(b) I, II

(c) II, III

(d) III, IV

(e) None of the above

Question 20. Among the following pipelines, whose performance suffers the most from poor branch prediction?

(a) 20 stages, branch resolved at stage 10

(b) 20 stages, branch resolved at stage 5

(c) 16 stages, branch resolved at stage 12

(d) 16 stages, branch resolved at stage 7

(e) 5 stages, branch resolved at stage 4

Part 2: Multiple Choice (3 points each)

Question 21. For which of the following reasons does pipelining improves performance over a single-cycle data path?

I. Decreases CPI

II. Decreases cycle time

III. Decreases instruction count

IV. Eliminates data dependencies

(a) I, III

(b) II, IV

(c) II

(d) I

(e) None of the above

Question 22. Branch delay slots are used to

(a) Eliminate data hazards

(b) Eliminate load hazards

(c) Decrease the delay of branches

(d) Decrease cycle time

(e) None of the above

Question 23. What is the CPI of a single-issue pipelined datapath with a 99% Dcache hit rate?

(a) < 1

(b) $= 1$

(c) > 1

(d) (a), (b), or (c) may be correct depending on the program

(e) (a), (b) AND (c) are incorrect!

Question 24. Which of the following generally improves the accuracy of dynamic branch prediction?

I. Increasing the size of the branch prediction buffer

II. Increasing the depth of the pipeline

III. Decreasing cycle time

IV. Using more bits to record the recent history of branches

(a) I, II

(b) I, III

(c) II, III

(d) I, IV

(e) None of the above

Question 25. Which of the following is not allocated to an activation record:

(a) Parameters to a function
(b) Registers saved by caller
(c) Registers saved by callee
(d) Return address
(e) Static local variables

Question 26. When pipelining a CISC instruction that requires multiple references to the data memory, which of the following techniques is required to maintain correct pipeline execution?

(a) Flushing

(b) Stalling

(c) Branch prediction

(d) same-cycle read/write register files

(e) None of the above

Question 27. The following 4 lines of code are to be executed on a superscalar pipeline that can execute up to 2 instructions per cycle.

```
add $2 $1 $1   #a
add $3 $2 $2   #b
add $5 $4 $4   #c
add $6 $5 $5   #d
```

Which of the following reorderings minimizes the number of stalls without altering the function of the original code?

(a) abcd

(b) adbc

(c) acbd

(d) badc

(e) cdab

Question 28. Which of the following techniques can be used to hide memory latencies?

I. Forwarding

II. Stalling

III. Out-of-order execution

IV. Flushing

(a) I

(b) I, III

(c) II, IV

(d) III

(e) None of the above

Question 29. Increasing the depth of pipelining increases performance.

(a) Always true

(b) Sometimes true

(c) Never true

(d) Cannot tell

(e) None of the above

Question 30. Which of the following is NOT a way to resolve a pipeline hazard?

(a) Stall the pipeline

(b) Use branch delay slots

(c) Data forwarding

(d) Data elimination

(e) Branch prediction

Question 31. How many of these can be found in a TLB entry?

I. Virtual page number

II. Physical page number

III. Virtual tag

IV. Cache block

V. Write permission bit

(a) 1

(b) 2

(c) 3

(d) 4

(e) 5

Question 32. Which of the following structures includes a linked-list as a component?

(a) Hierarchical page table

(b) Translation look-aside buffer

(c) Inverted page table

(d) Virtually addressed cache.

(e) None of these use linked-lists.

Question 33. How many blocks are in an inverted page table for a machine with a 32 bit virtual address and 8K byte pages?

(a) 13 entries

(b) 19 entries

(c) 8192 entries

(d) 524,288 entries

(e) Can't determine from the question.

Question 34. Given a 2-level page table with 2K byte pages, requiring 4 bytes per page table entry. What are the sizes (in bytes) of the super page table and the page table for a machine with 32-bit virtual addresses?

(a) 8K bytes and 32M bytes

(b) 2K bytes and 4M bytes

(c) 16K bytes and 8M bytes

(d) 32K bytes and 64M bytes

(e) Can't determine from the question.

Question 35. Which of the following is not a benefit of virtual memory?

(a) Easier memory model for programmer.

(b) Enables larger program to be executed.

(c) Support multi-processing.

(d) Simplifies memory hardware.

(e) Identifies access permission errors in memory use.

Question 36. Given a 500 MHz processor with 16 KB data and 16 KB instruction caches, the cost to access main memory is 100 cycles. Both caches are 2-way set associative. A program running on this processor has a 98% Icache hit rate, and a Dcache hit rate of 95%. On average, 40% of the instructions are loads or stores. Assume that the base CPI for this program running on a machine with an ideal memory system is 1. What is the relative CPI of the program on the machine described above?

(a) 2.0

(b) 3.7

(c) 5.0

(d) 6.3

(e) 7.0

Question 37. The company that makes the processor in question 36 has plans to scale it up to 1 GHz increasing the base CPI to 1.5 and the cost of accessing main memory to 200 cycles. What happens to the performance of the new machine?

(a) The overall CPI increases and the program executing time increases.

(b) The overall CPI decreases and the program executing time increases.

(c) The overall CPI increases and the program executing time decreases.

(d) The overall CPI decreases and the program executing time decreases.

(e) There in not enough information to determine the performance impact of this change.

Question 38. To help mitigate this cost of the increase in cache miss penalty for there new machine (in question 37), a 256 KB unified Level-2 cache will be added. The Level-1 Icache and Dcache will remain at 16 KB each and any L1 misses will be sent to the L2 cache (both instructions and data). The hit rate of the Level-2 cache is 75%, each hit costs 10 cycles, while misses go to memory (now 210 cycles). What is the new CPI for this machine? (Base CPI is still 1.5).

(a) 2.1

(b) 2.7

(c) 3.3

(d) 3.9

(e) 4.6

Question 39. If the Icache is increased to 32 KB for the machine in question 36, its miss rate for this program drops to 1%. If the Dcache is increased to 32 KB, its miss rate for this program drops to 2%. Suppose that there is only enough room to double the size of one of these caches. Which cache should be increased, and what is the most compelling reason for doing so?

(a) Icache, because it would have the lowest hit rate.

(b) Icache, because it accounts for the most references in this workload.

(c) Dcache, because has a more dramatic cut in its hit rate.

(d) Dcache, because it lowers the CPI the most for this workload.

(e) Either choice is fine, since the impact on performance is the same.

Question 40. Which of the following statements is true about write-through and write-back caches of the same configuration:

I Write-through caches require less cache state.

II Write-back caches require less cache state.

III Write-back caches usually generate more traffic with main memory.

IV Write-through caches usually generate more traffic with main memory.

(a) I and III are true.

(b) II and IV are true.

(c) I and IV are true.

(d) II and IV are true.

(e) Only III is true.