

EECS 370 - exam 2

Name:

Uniqname:

Honor Pledge: I have neither given nor received aid on this examination.

Signature:

1. (10 points, 2 points each) Evaluate the following statements about the LC2 datapaths (single-cycle, multi-cycle, pipelined).
 - (a) The pipelined datapath requires less hardware than the single-cycle datapath.
TRUE FALSE
 - (b) The pipelined datapath requires less hardware than the multi-cycle datapath.
TRUE FALSE
 - (c) The pipelined datapath has a lower CPI than the multi-cycle datapath.
TRUE FALSE
 - (d) The pipelined datapath has a lower CPI than the single-cycle datapath.
TRUE FALSE
 - (e) The pipelined datapath has a higher clock rate than the multi-cycle datapath.
TRUE FALSE

2. (5 points) In project 3, we added the WBEND pipeline register as another possible source for data forwarding. If we take this WBEND pipeline register away, what property must the register file have to allow correct program execution without additional stalling?
 - (a) The register file must be able to read and write values to the same register in one cycle.
 - (b) The register file cannot both read and write values to the same register in one clock cycle.
 - (c) The register file cannot both read and write in one clock cycle.

- (d) The register file must read register values before writing register values in a clock cycle.
 - (e) The register file must write register values before reading register values in a clock cycle.
3. (5 points) If we removed all hazard detection logic implemented in project 3, and we inserted **noop** instructions between other adjacent instructions, what is the smallest number of **noop** instructions we need to put between each pair of other instructions to guarantee that all programs will execute correctly?
- (a) 0
 - (b) 1
 - (c) 2
 - (d) 3
 - (e) 4
4. (5 points) If we do not have logic to allow forwarding from the MEMWB or from the WBEND pipeline registers, what is the maximum number of stall cycles necessary for a load hazard?
- (a) 0
 - (b) 1
 - (c) 2
 - (d) 3
 - (e) 4
5. (5 points) For a MIPS like CPU (32 bit address space, byte addressible memory), how many tag bits are needed for a 1 megabyte 4-way set-associative cache with a 32 byte line size?
- (a) 2
 - (b) 9
 - (c) 14
 - (d) 16
 - (e) 24
6. (5 points) What happens to the tag field when the cache associativity goes from 8 to 2?

- (a) Tag size increases by 1 bit
 - (b) Tag size decreases by 1 bit
 - (c) Tag size increases by 2 bits
 - (d) Tag size decreases by 2 bits
 - (e) Tag size is unchanged, but the bits that are used for the tag are changed.
7. (5 points) If we use a write-through policy instead of a write-back policy, do we still need valid and dirty bits?
- (a) Valid: yes, dirty: yes
 - (b) Valid: yes, dirty: no
 - (c) Valid: no, dirty: yes
 - (d) Valid: no, dirty: no
 - (e) None of the above
8. (5 points) Which of the following pipeline modifications may **REDUCE** overall performance?
- (a) Detecting earlier in the pipeline if the branch is taken or not.
 - (b) Predicting that a branch is taken if the last time the branch was executed, it was taken.
 - (c) Allowing data forwarding to both the EX and MEM stages instead of just to the EX stage.
 - (d) Forwarding data using the WB/END register instead of writing registers on the positive clock edge and reading on the negative edge.
 - (e) None of the above.
9. (5 points) Suppose you are given an implementation of the LC-2K3 that is identical to the Project 3 pipeline but uses stalling instead of data forwarding to resolve data dependencies. Given the following LC-2K3 program, which reordering BEST improves performance while giving the same result?
- ```

add 1 1 2
add 2 2 3
add 3 3 4
add 5 5 6
add 6 6 7
lw 7 1 0

```

- (a) add 1 1 2  
 add 5 5 6  
 add 6 6 7  
 lw 7 1 0  
 add 2 2 3  
 add 3 3 4
- (b) add 5 5 6  
 add 6 6 7  
 lw 7 1 0  
 add 1 1 2  
 add 2 2 3  
 add 3 3 4
- (c) add 1 1 2  
 lw 7 1 0  
 add 5 5 6  
 add 2 2 3  
 add 6 6 7  
 add 3 3 4
- (d) add 1 1 2  
 add 5 5 6  
 add 2 2 3  
 add 6 6 7  
 add 3 3 4  
 lw 7 1 0
- (e) add 5 5 6  
 add 1 1 2  
 add 2 2 3  
 add 6 6 7  
 lw 7 1 0  
 add 3 3 4

10. (5 points) Consider three versions of a 5-state pipeline **IF/ID/EX/MEM/WB** with full data forwarding that stalls on branches. Version A resolves branches in the MEM stage and has clock period  $T$ . Version B resolves branches in EX and has clock period  $1.5 \times T$ . Version C resolves branches in ID and has clock period  $1.75 \times T$ . Which version yields the shortest runtime for a program with

25% branch instructions and no load hazards?

- (a) Version A
- (b) Version B
- (c) Version C
- (d) The three versions achieve equal times.
- (e) It depends on the length of the program.

For the next three questions, consider the following MIPS code fragment:

```
lw r1, 0(r2)
addi r1, r1, #1
sw 0(r2), r1
addi r2, r2, #4
sub r4, r3, r2
beqz r4, L1
add r1, r2, r3
```

L1: ...

Assume a 5-stage pipeline **IF/ID/EX/MEM/WB** and a register read and a write can occur in the same clock cycle. Assume that the branch is resolved in **MEM** and all memory references hit in the cache. Let the initial value of **r3** be **r2 + r31**.

11. (5 points) Assume without data forwarding hardware and the branch is handled by flushing the pipeline, how many cycles does this code take to execute?
- (a) 14
  - (b) 15
  - (c) 16
  - (d) 17
  - (e) 18
12. (5 points) Assume with data forwarding hardware and the branch is handled by predicting it as not taken, how many cycles does this code take to execute?
- (a) 8
  - (b) 9

- (c) 10
- (d) 11
- (e) 12

13. (5 points) Assume the branch has a single branch delay slot. Reorder the code to be as fast as possible. What is the minimum number of cycles this code takes to execute?

- (a) 8
- (b) 9
- (c) 10
- (d) 11
- (e) 12

14. (5 points) Suppose that you are given a 16-bit, WORD-addressible memory (1 word = 16 bits). The cache can hold 64 KB of data, is 4-way set associative, and has 128-byte blocks. What are the values of the offset, tag, and index for the address 0xB367? Give your answer in decimal.

15. (5 points) With the following processor configuration, how many lines does the cache have?

- 32-bit memory addresses
- Byte addressable
- 8KB cache, 4-way set associative
- 16 byte cache block size

16. (10 points) You need to resolve a dispute at the LC-2 engineering department. The current design is the pipelined implementation that you should be familiar with from the lectures or programming project 3. Engineer Olivia Optimist wants to add the capability of forwarding from the MEM/WB pipeline register back into the MEM stage. She says this will eliminate a stall in some situations. However, engineer Paul Pessimist says that this forwarding path is not useful. Who is right? If you say Paul, justify why this new forwarding path is never needed. If you say Olivia, give a **very short** example of an instruction sequence that would run faster using this new forwarding path.

17. (10 points) Associative versus direct-mapped caches

Thanks to some clever digital design, the architects of the HiPC computer company (all of who took EECS 270 and EECS 370 while at Michigan) can now build caches with arbitrarily large associativity with very low hardware and delay overheads. Due to chip area considerations, however, they are only allowed to use a cache with **fixed total size for data**. Ben Bitdiddle claims that to guarantee the maximum hit ratio under all possible programs, the cache should be made fully associative. On the other hand, Tricia Hacker argues that increasing associativity may decrease the hit ratio of certain programs when using an LRU replacement policy.

Who is right? If you agree with Ben, provide an argument in support of his position. If you agree with Tricia, provide a program whose performance degrades as associativity increases.