Optrex Corporation DMF 5005NY-LY-AKE Interfacing Guide

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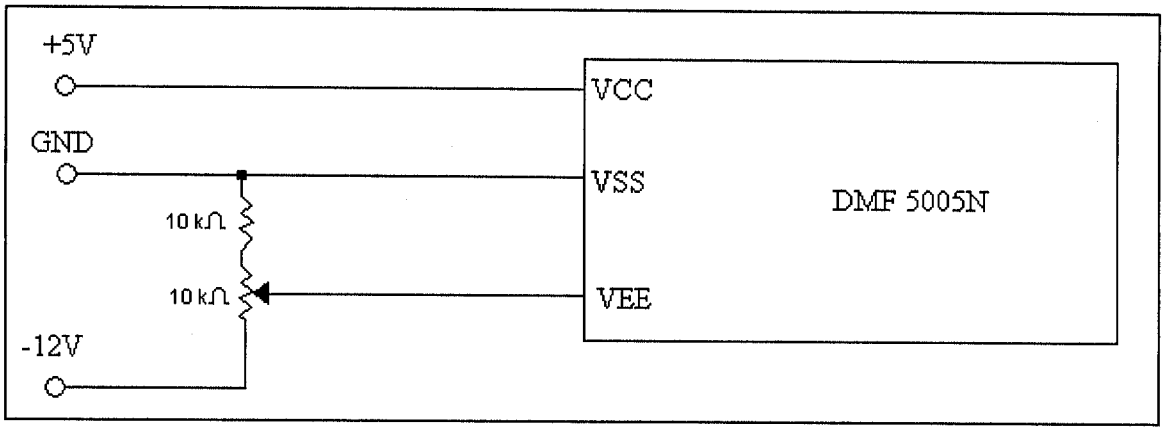
Section 1: Connections

Despite the manual's suggested circuit, the following circuit provided the best results:



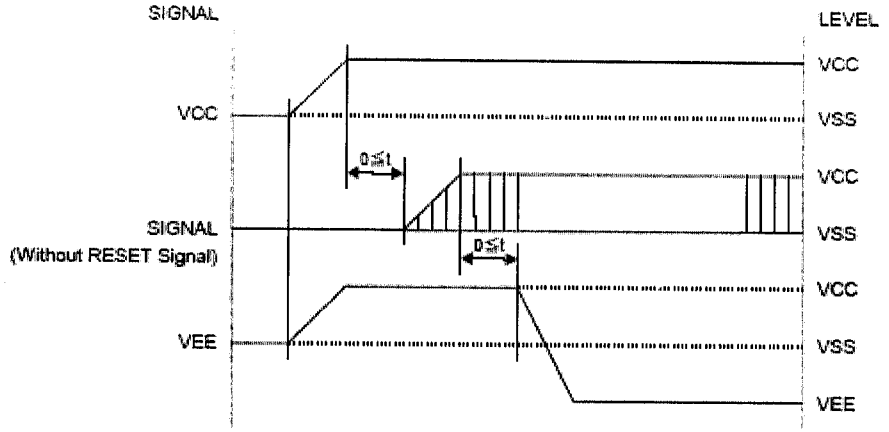
Pin Assignment:

No.	Symbol	Level	Function
1	FG	—	Frame Ground
2	Vss	—	Power Supply (0V, GND)
3	Vcc	—	Power Supply for Logic
4	V_{EE}	—	Power Supply for LCD Drive
5	$\overline{WR}$	H / L	Write Signal L : Active
6	$\overline{RD}$	H / L	Read Signal L : Active
7	$\overline{CE}$	H / L	Chip Enable Signal L : Active
8	C/$\overline{D}$	H / L	Write Mode H : Command Write L : Data Write Read Mode H : Status Read L : Data Read
9	NC	—	Non-connection
10	$\overline{RESET}$	H / L	Reset Signal L : Reset
11	D0	H / L	Display Data
12	D1	H / L	Display Data
13	D2	H / L	Display Data
14	D3	H / L	Display Data
15	D4	H / L	Display Data
16	D5	H / L	Display Data
17	D6	H / L	Display Data
18	D7	H / L	Display Data
19	FS	H / L	Font Switch H : 6×8 dots L : 8×8 dots
20	NC	—	Non-connection

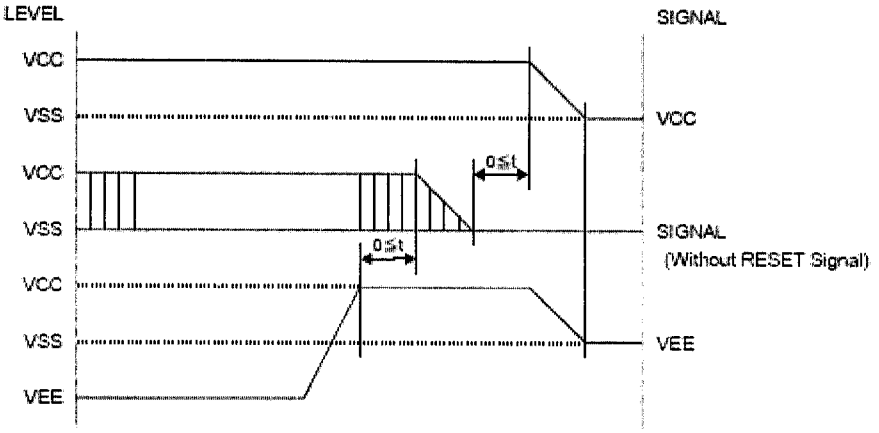
It should be noted that pin 19, FS, must be kept high on the DMF 5005N, or the device will not accept commands or data.

Section 2: Power On/Off/Reset Sequencing

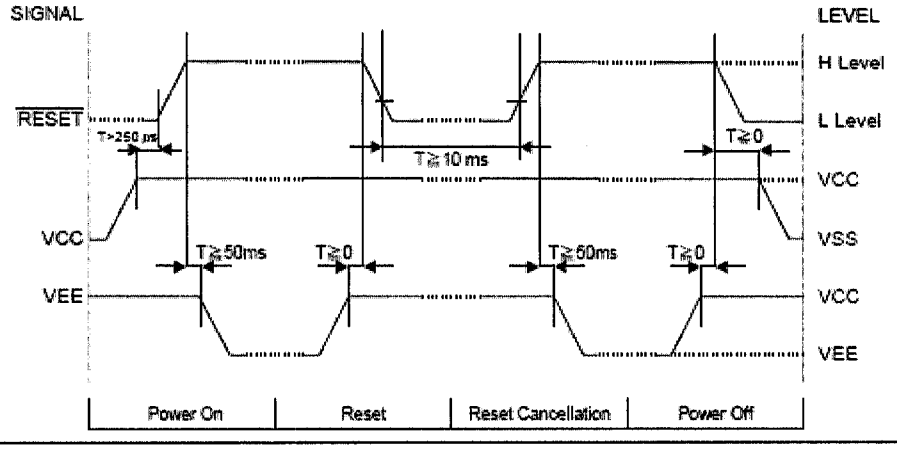
ON Sequence



OFF Sequence



Reset Sequence

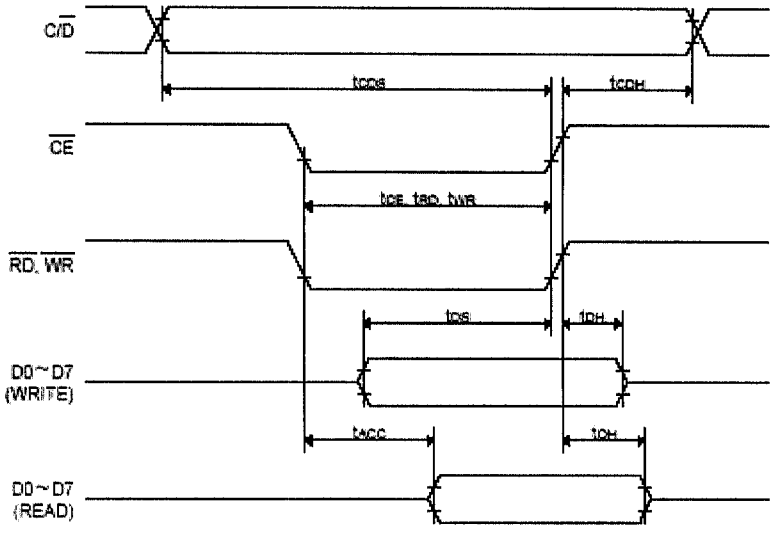


The required time spacing between VCC and VEE engagements is on the order of milliseconds. The simplest solution to ensuring these timing requirements are met is using additional switches on the breadboard that allow for individual control of the 5V and -12V connections. Reset timing similarly requires stable VCC and VEE signals for a time on the order of milliseconds. Reset can be connected to any of the switches on the lab board and is generally used only during the initialization sequence.

Section 3: Signal Timing

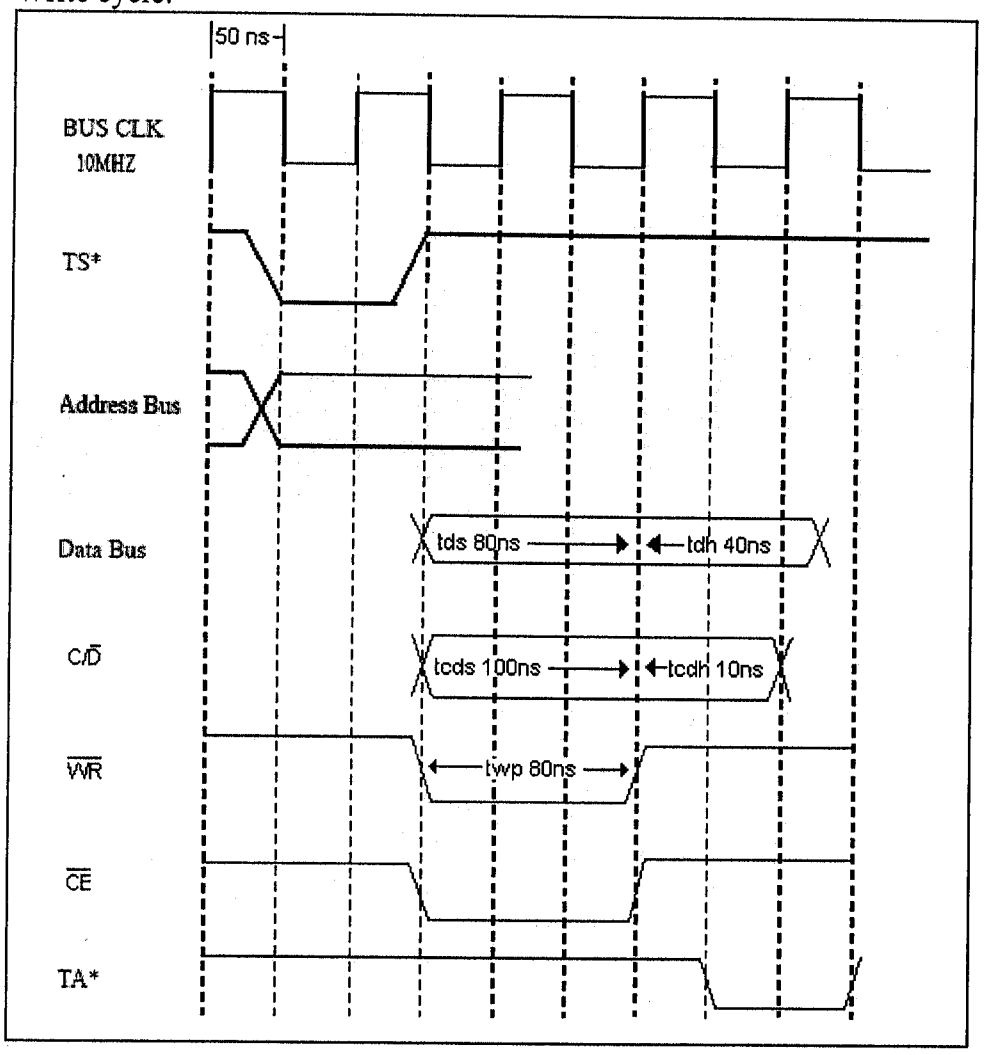
V_{CC}=5.0V±10%

Parameter	Symbol	Min.	Max.	Units
C/$\overline{D}$ Setup Time	t_{CDS}	100	—	ns
C/$\overline{D}$ Hold Time	t_{CDH}	10	—	ns
$\overline{CE}$, $\overline{RD}$, $\overline{WR}$ Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	—	ns
Data Setup Time	t_{DS}	80	—	ns
Data Hold Time	t_{DH}	40	—	ns
Access Time	t_{ACC}	—	150	ns
Output Hold Time	t_{CR}	10	50	ns

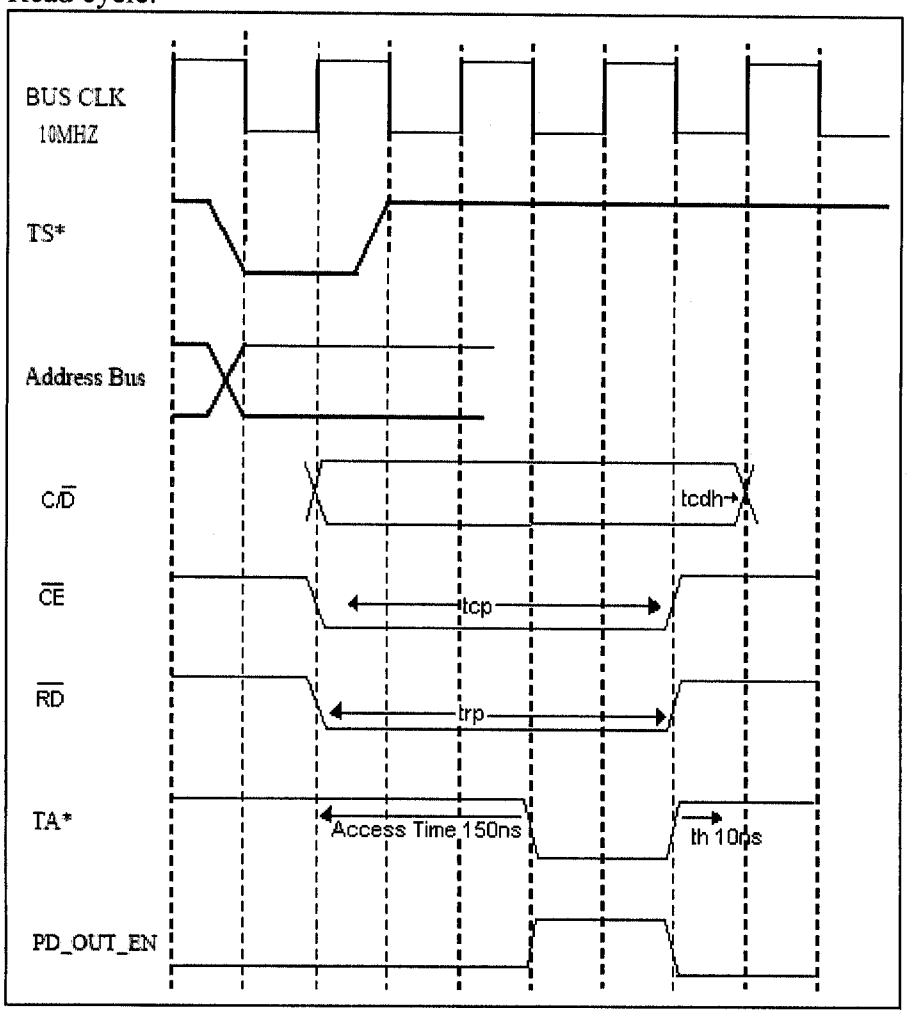


Using the provided timing diagram, the following timing diagrams for a read and a write cycle were developed and tested:

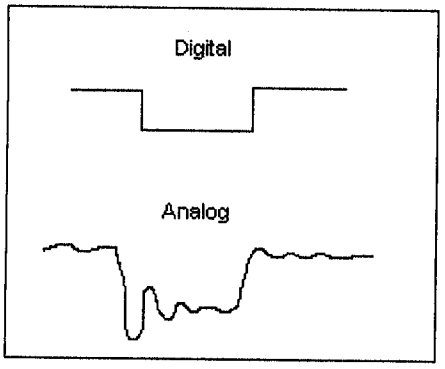
Write cycle:


50 ns
BUS CLK
10MHZ
TS*
Address Bus
Data Bus
tds 80ns
tdh 40ns
C/D
tcds 100ns
tcdh 10ns
WR
twp 80ns
CE
TA*

Read cycle:


BUS CLK
10MHZ
TS*
Address Bus
C/D
tcdh
CE
tcp
RD
trp
TA*
Access Time 150ns
th 10ns
PD_OUT_EN

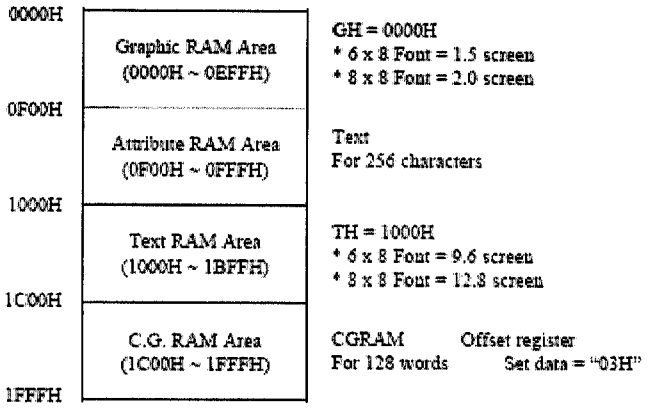
The provided timing diagrams are rather conservative. Writing to the device RAM poses a particular concern for timing. Due to the nature of actual signals:



Special care must be taken to maintain the device's required pulse widths. Any signal that is to be determined as low by the display must be less than 0.8 V. The bounce seen in the analog signal above when it transitions to low can easily exceed this threshold, causing it to be seen as returning high thereby invalidating the current write due to disobeyed signal pulse widths. This appeared to be most of a concern on the WR* signal, especially during writes to RAM. This effect is largely due to the high inductance of running wires from the test points to the LCD controller with relatively small resistance over the same path. Therefore, adding a 100 Ohm resistor in series with the wires running from the test points to the LCD controller will damp the control lines, causing them to look very similar to the expected digital signal. Without the resistors, when the above timing diagrams were created and followed, the display behaved as expected for most 373 lab stations. Adding the resistors for all control and data lines is not only good practice, but will also ensure proper operation across all stations. Finally, ensure that the test points used to write these values produce a suitably high Vcc. One board in particular produced about 2.5V, which caused erratic behavior. Anything around 3.6V or above is ample for proper communication. As with any device in the lab, testing of each signal should be done with an oscilloscope to verify correctness. Testing with the oscilloscope rather than a multi-meter or a logic analyzer, particularly for the timescale that this LCD operates at, will save significant debugging time.

Section 4: Device operation

The device behaves essentially as a small, continuous region of memory. It comes equipped with a small microcontroller that automatically updates the screen with the memory contents. The memory is, however, large enough that the starting point of the display's contents in relation to the memory's contents must be specified by a text/graphic home position pointer.



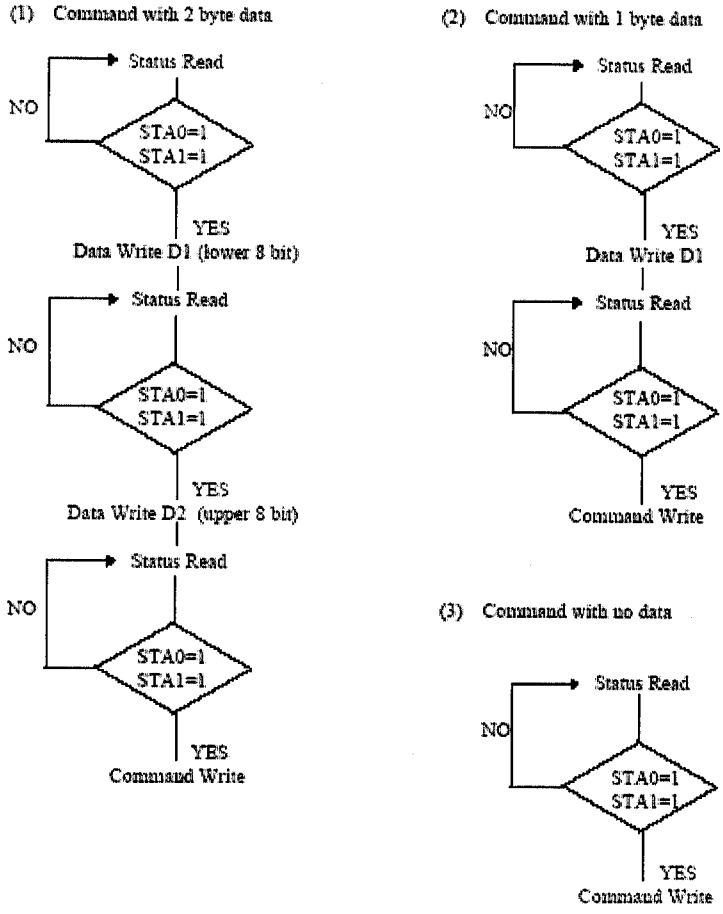
The following suggested initialization sequence gives a good overview of the devices properties:

Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Power on	Power on									
Hard reset (Use reset terminal)	RESET="L" (1mSec minimum after Vcc ≥ 4.75V)									
Mode set	1	1	0	0	0	0	0	0	0	"OR" mode
Control word set Graphic home position set (Graphic home position 0000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 1	0 0 0	Graphic home address command
Number of graphic area set (Graphic 30 x 8 dots)	0 0 1	0 0 0	0 0 1	0 0 0	1 0 0	0 0 0	1 0 0	1 0 1	1 0 1	Number of area Command
Text home position set (Text home position 1000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 1 0	0 0 0	0 0 0	0 0 0	0 0 0	Text home address Command
Number of text area set (Text 30 column)	0 0 1	0 0 0	0 0 1	0 0 0	1 0 0	0 0 0	1 0 0	1 0 0	1 0 1	Number of area Command
(Initialize end) (Data write)										
Address pointer set (Address pointer 0000H)	0 0 1	0 0 0	0 0 0	0 0 1	0 0 0	0 0 0	0 0 1	0 0 0	0 0 0	Graphic home address Command
Data write (Graphic)	0 1	0 1	1 1	0 1	1 0	0 0	1 0	0 0	1 0	Data Command
	0 1	1 1	0 1	1 1	0 0	1 0	0 0	1 0	0 0	Data Command
Address pointer set (Address pointer 1000H)	0 0 1	0 0 0	0 0 0	0 0 1	0 1 0	0 0 0	0 0 1	0 0 0	0 0 0	Text home address Command
Data write (Text) (o)	0 1	0 1	0 1	1 0	0 0	1 0	1 0	1 0	1 0	Data Command
(p)	0 1	0 1	0 1	1 0	1 0	0 0	0 0	0 0	0 0	Data Command
Display Mode Set (Text/Graphic on)	1	1	0	0	1	1	1	0	0	

Note that the number used for graphic and text area set should be 0x28 for both with this particular LCD model. Furthermore, this page reads all correct command codes. The DMF 500 Series Users Manual lists some incorrect codes in the codes section, such as home position set, which it lists as 0x20 rather than the correct 0x40.

Also note that between every single operation with the device, a status check must be performed. Unlike many LCDs, latency is not the only issue with performing a series of commands. The microcontroller contained on this device has an interrupt scheme that requires status checks to be performed in order for the device to accept commands or data. This procedure is outlined below.

The built-in LCD controller, T6963C, is operating asynchronously to the CPU clock. The following procedure is required for data transmission between the module and the CPU.



Data writes to RAM can be performed in many ways with regards to the effect each write has on the address pointer. Leaving the text/graphic home position static, and using the auto-increment data write that moves the address pointer forward by 1 byte each write provides a convenient method of writing a string of text. Using the auto-increment feature with graphics, however, appeared to yield incorrect results, so these operations were done by writing a byte, moving the address pointer forward, then writing the next byte. It is quite possible that this is not necessary; however, not enough testing was done with graphics using this feature. Writing characters simply requires writing the correct byte using the character codes provided in the manual. Concerning this, though, it is important to note that these character codes are not standard ASCII, so any existing conversion algorithms, such as those that convert between ints and strings must be altered to use this particular character set. Graphic writes are performed analogously to character writes. The only difference is that the byte is written to the user-defined graphic area of memory and the eight bits will define pixels as being on or off. Due to characters being six pixels wide on this display, though, means that a write of 0xFF is the same as a write of 0x3F, both turning on six pixels at that particular character location. In order to produce the following picture:

Writes of 0x1E, 0x02, 0x1B, 0x08 would be performed separated by increments of 0x28 to the address pointer between each. 0x28 is the hex equivalent of 40 decimal, which is the width of the display in bytes. The display is 40 pixels or eight characters in height. Therefore, to write a graphic that will fill the entire display requires 1600 byte writes.

Section 5: Additional help

In addition to the common problems listed in the manual,

If the device appears to behave differently each time the same set of commands and data are written to it, or the data that appears on the screen appears only in columns of the same data with that data being only part of the entire data set sent to the device, the signal timing is probably incorrect, particularly the WR signal. Experiment with different pulse widths and start times.

If the characters displayed on the screen begin to flash or display other strange behavior, the text attributes section of memory was probably written over. Writing to this area accidentally may even cause the display mode to change to show the text data even though the display mode command has not been sent.

If strange characters, often Japanese, appear on the screen, the text section likely contains bytes beyond the 128 specified in the manual. Resetting the display does not reset the memory. The memory must be cleared if no characters are desired in a particular location by writing 0x00.

If a solid bar appears across the screen, the reset signal is low, and the device is attempting to reset. Extended reset periods (exceeding 10 seconds) can damage the display.