

EECS 373 Design of Microprocessor-Based Systems

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Lecture 12: Memory and PCBs

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Slides inherited from Mark Brehob.

Outline

- Context and review
- Memory
- PCB design

Context and review

- ADC and DAC operation and error
 - Speed / accuracy / monotonicity trade-offs.
- Prototyping
 - Breadboards.
 - Soldering.
 - Wire wrap.
- Memory
 - Flash
 - Speed, functionality, reliability trade-offs.

Outline

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- PCB design

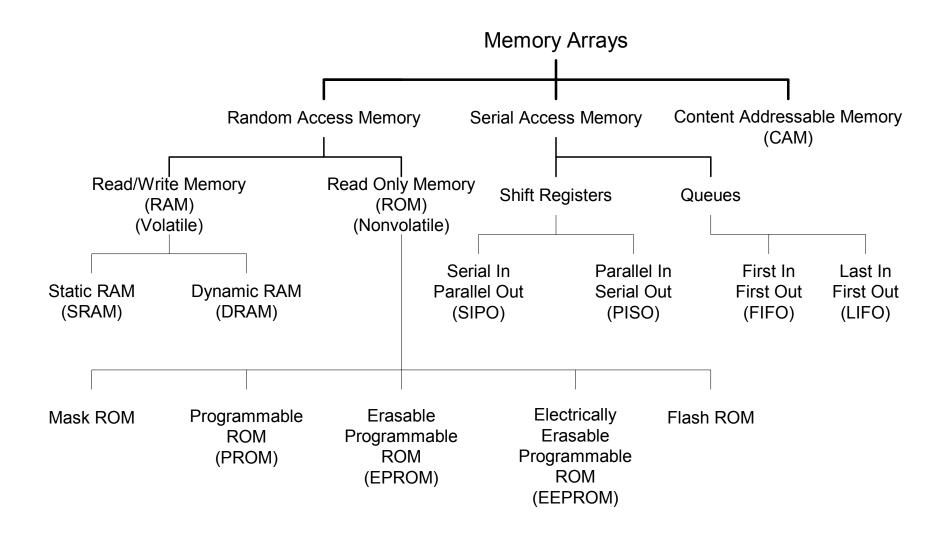
Memory: why?



- You'll be dealing with this a lot in your projects.
- A little review now can save you trouble later.

Memory array types

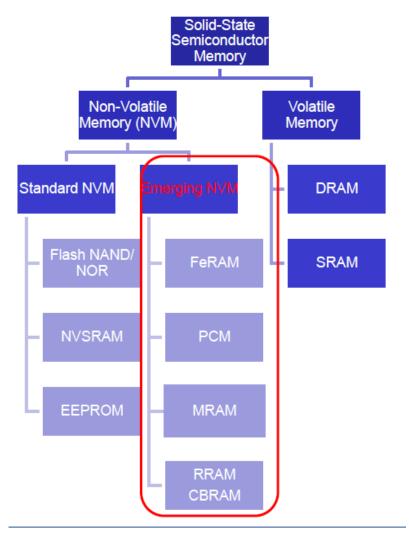






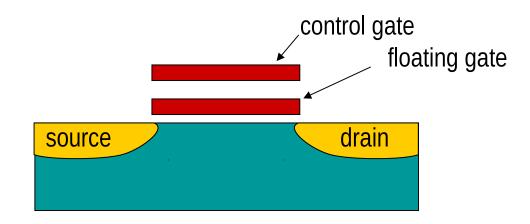
Nonvolatile memory types

- Ferroelectric RAM: polarization changed by electric field. DRAM/flash-like. Electical polarization instead of floating gate. Reading → current pulse on write? 150 ns. 10¹² cycles.
- Phase change memory: amorphous (off) vs. crystalline (on). 5ns to 100 ns write. ns read. 10⁸ cycles.
- Magnetoresistive RAM. ns read.
 Slightly more for write. Many cycles.
- Programmable metallization cell: redox filament. 10s of ns read, write. 10¹⁰ cycles.
- Flash: ns read, ms write.
- EEPROM: ns read, ms write.
- SRAM/DRAM: ns read and write.



Floating gates

- Write: hot-electron injection or Fowler-Nordheim tunneling.
 - High voltage on control gate >> operating voltage
 - Electrons are trapped in the floating gate.
 - Will not discharge for many years.
- Erase? Fowler-Nordheim tunneling.



- Read by seeing whether it acts like a transistor or a wall.
- Tend to self-destruct after 10⁵ write/erase cycles.

Outline

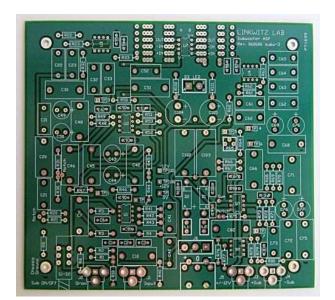
- Context and review
- Memory
- PCB design

PCBs: why?

 Even if you aren't making one for your project, need to understand how they work for debugging / reverse engineering.

Printed circuit board design

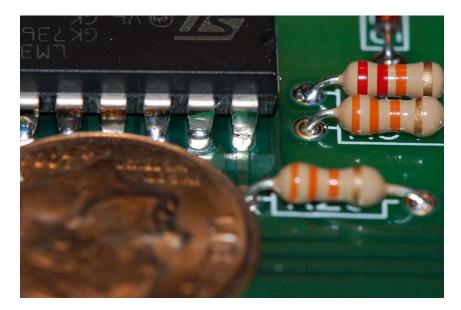
- Physical support.
- Electrical connections.
 - Traces have restricted dimensionality.
 - Very thin, high resistance.
 - Holes/vias and pads.
 - Rework is hard.

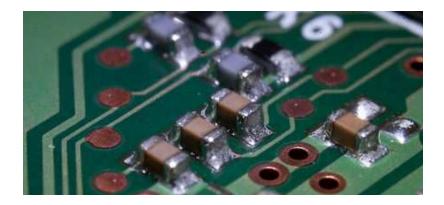




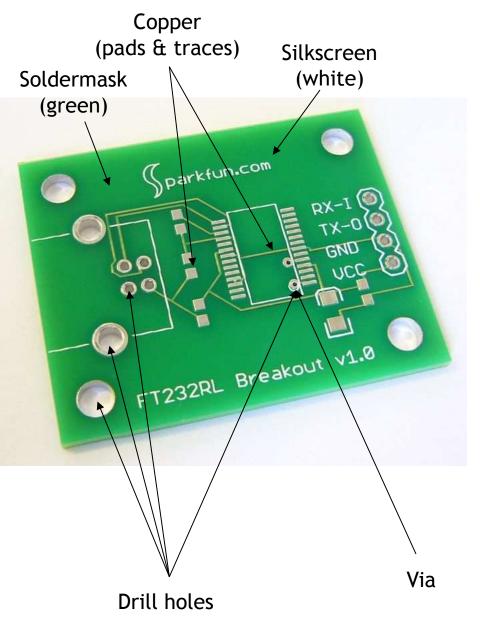
Basic terminology

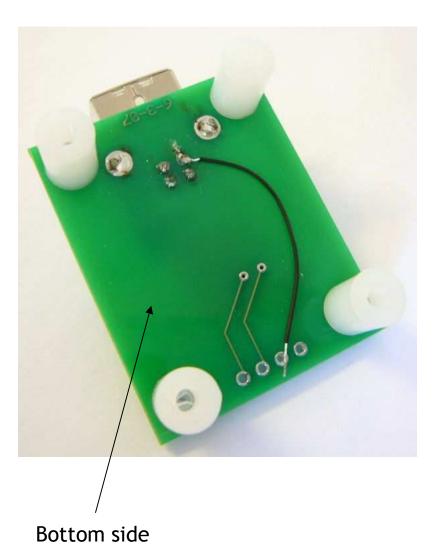
- Interconnects: traces.
- Inside of a given "layer" traces which cross are electrically connected.
- Can have multiple conductive layers by stacking/bonding boards.
- Through-hole: Having holes in the PCB designed to have pins put through the holes.
 - Contrast with surface mount where device goes on top.
- Surface mount.





Parts of a PCB





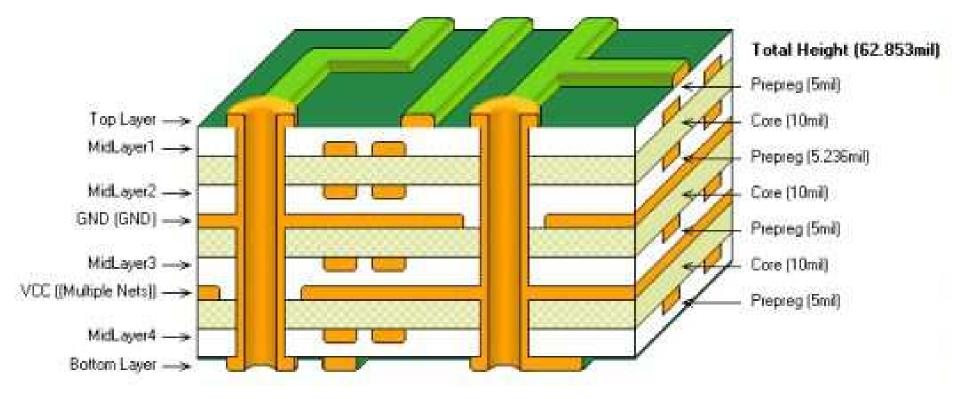
Vias

- Sometimes you need to connect traces on layers.
 - Use a via: a plated through hole
 - Generally smaller than a through hole for a pin.

Clearances

- There will be space between the traces, other traces, and plated holes.
 - You need to meet the requirement of the manufacturer.

The layered construction of a PCB: a six layer board



What do do with layers?

- Mostly orthogonal routing layers.
- Ground planes to increase local power supply capacitance and minimize resistance.
- Power plane for similar reason.
- More layers \rightarrow higher cost.

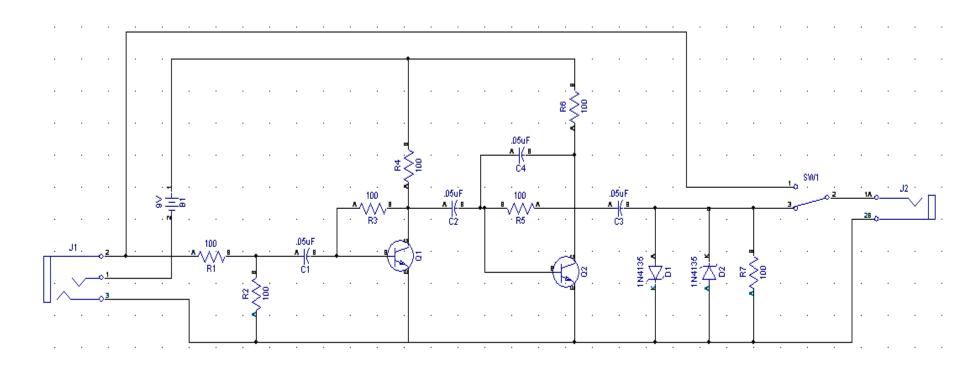
How to design PCB

- 1. Create schematic
- 2. Place parts
- 3. Route interconnect
- 4. Generate files

Step 1: Create schematic

- The first thing you want is something that looks like a textbook circuit diagram. It just shows the devices and how they are connected.
 - Sometimes you will worry about pinouts here (say when working with a microprocessor maybe).
 - But usually you don't.
- No notion of layout belongs here, although the schematic connectivity will influence layout.

Example schematic



Why a schematic?

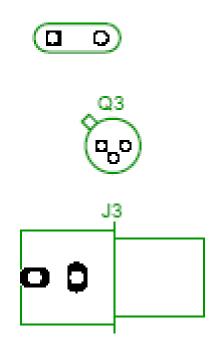
- Communication and formalization are main goals.
 - This is probably what your sketch on paper would look like.
 - You can find and fix bugs more easily here than the PCB layout.

Step 2: Place parts

- You need to place the patterns on the board.
 - You need to not overlap them to that the components can actually fit on the board.
 - You want to leave room for the traces to connect everything.
- This is very much an art form.
 - In fact you will find people who rant about "sloppy" or "unprofessional" placements.
- Some tools will do this for you.
- Sometimes they screw up.

Patterns

- Once you know what it is you want to build, you need to figure out how to lay it out on the board.
 - You need to know how big each piece is, and where the holes need to be placed.
- Each device has a pattern.
 - You will occasionally need to create a pattern.



Step 3: Route interconnect

- A route is a connection between devices.
 It may consist of multiple traces
- There are design rules which include:
 - Minimum trace width
 - Minimum spacing between traces and holes
 - Minimum spacing between holes and holes.
- Rules vary by manufacturer.
- Units vary my manufacturer.

Issues of measure

- PCB designers use odd terminology.
- A "thou" is a thousandth of an inch.
- A "mm" is a millimeter
- A "mil" is a thousandth of an inch.
 - Thou is generally preferred over mil to avoid confusion, but most tools/vendors use mil.

Trace width

- In general most PCB manufactures seem to have trace-width minimums of 6-10 thous.
 Most are willing to go smaller for a price.
- A rule of thumb is to use a 50 thou minimum for power/ground and 25 for everything else.
 - This is to drop the resistance of the traces.
 - In general you are worried about heat dissipation
- There are lots of guidelines for width/power but in general you are looking at:
 - A 10cm trace needs to be 10 thou wide if it will carry 1 amp.
 - 5 amps at 10cm would require 110 thou.

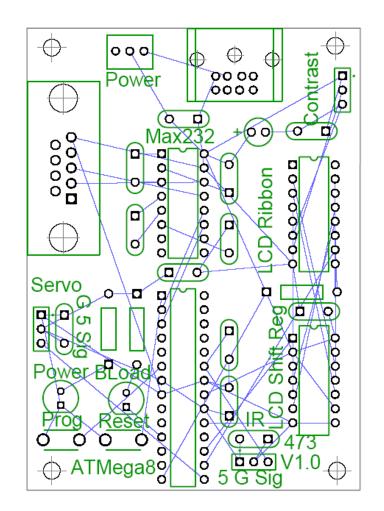
Trace width continued

- The problem with wide traces is that they are hard to route.
 - In particular you might wish to go between pins of a device.
- One solution is to be wide normally and "neck down" when you have to.
 - This is more reasonable than you think.
 - Think resistors in series.



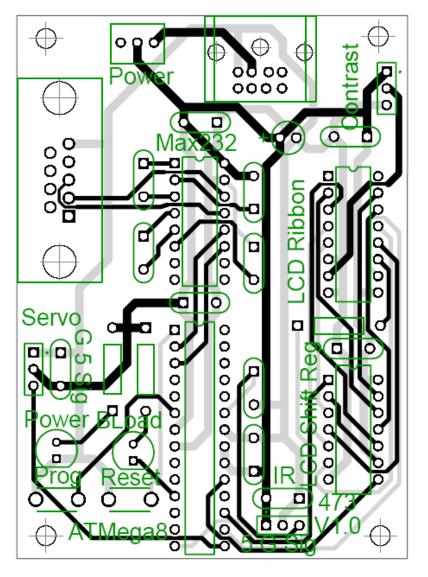
Rat's nest.

- Rat's nest shows device placements and connections but not routing.
 - Automatically generated for you.
 - Sometimes before
 placement, sometimes
 after.
 - Varies by tool.

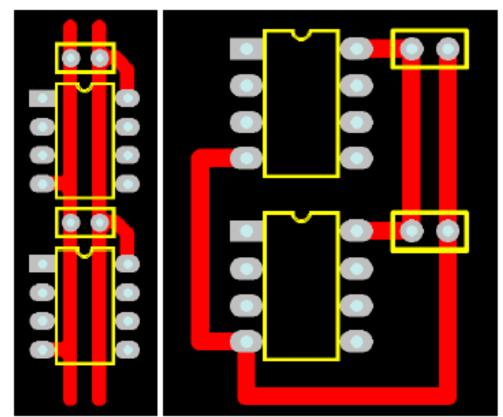


Routing for real

- You can use an autorouter to route your traces
 - Some people hate these as the design will be "ugly".
 - Saves a lot of time.
 - Oddly, not always as good as a person can do.
 - But much faster.
- Still generally need to do some (or all) of the routing by hand
 - Very, very tedious.



Routing quality

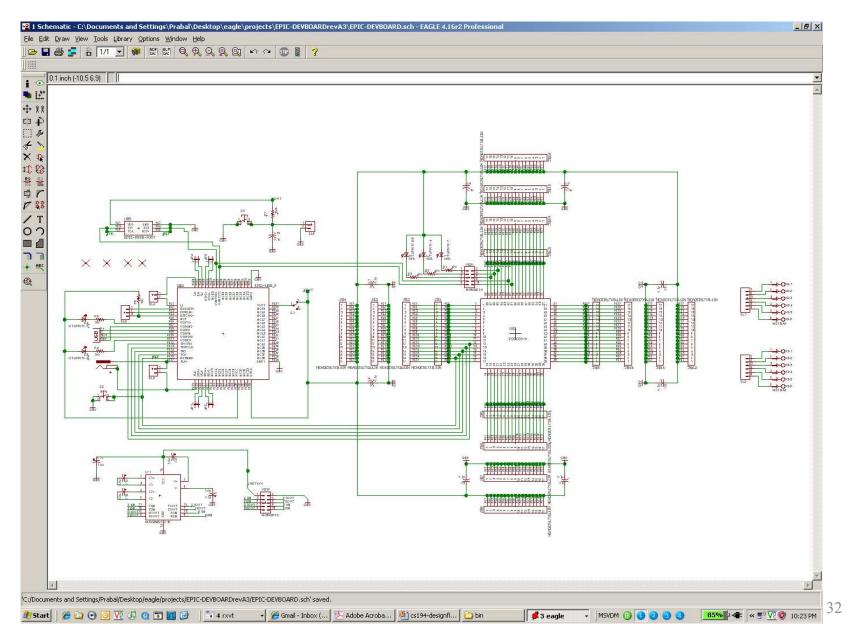


An example of GOOD power routing (Left) and BAD power routing (Right)

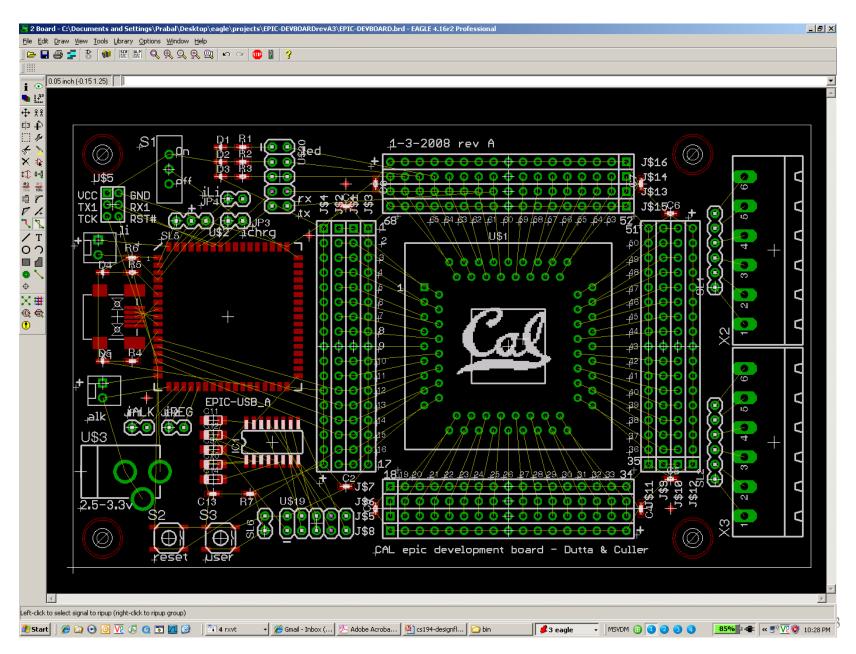
Step 4: Generate files

- Once the design is done, a set of files are generated.
 - Each file describes something different.
 - Copper on a given layer.
 - Silkscreen.
 - Solder mask.
 - Most files are in "Gerber" format.
 - Human-readable (barely) ASCII format.
 - Has commands like *draw* and *fill*.
 - Drill files are a different format called Excellon.
 - Human-readable (barely) ASCII with locations and diameters for the holes.
- Generally you zip all these files up and ship them as a single file to the PCB manufacturer.
 - Often a good idea to include the design file(s) too.

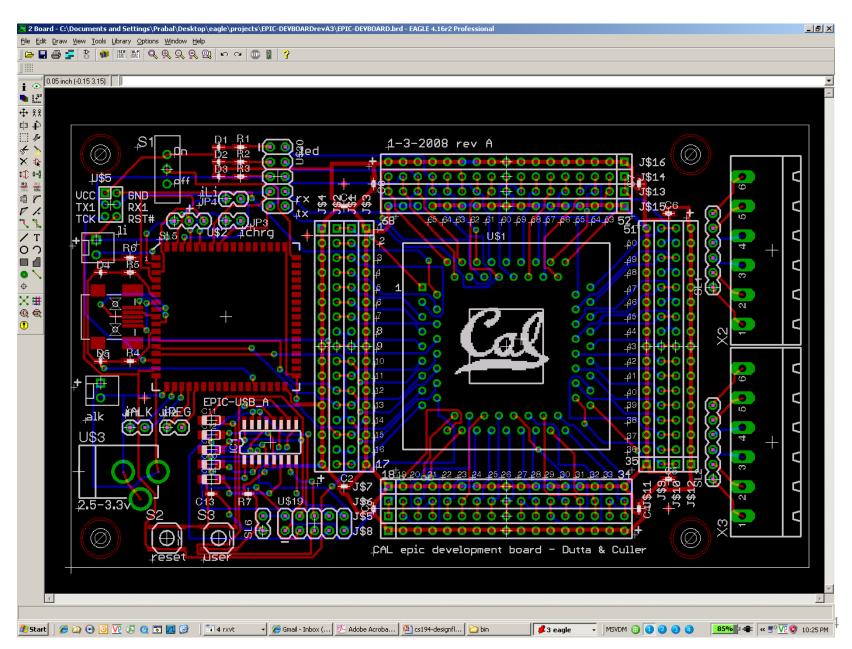
The schematic captures the logical circuit design



Floorplanning captures part locations



The auto-router places tracks on the board, saving time



1 2 4 3 CNI 26 51 UART RXD0 25 50 UART TXD1 24 49 PW0 29 48 PW1 GNI VSNSR CI INT2 INT1 23 22 21 20 47 PW CN3 ECQ-P1H103GZ INT0 46 PW3 : CC CCA : 0.01uF R2 U2A LED3 LED2 LED1 45 PW4 4 19 44 PW5 CFR-25JB-100R 18 43 PW6 S2B-PH-K-S PRPN022PARN 100 MAX9020EKA-T 42 ADC VCC RD WR 41 ADC6 1 15 40 ADC5 ALE 14 39 ADC4 PW7 38 ADC 12 USART1 CLK PROG MOSI 37 ADC2 11 10 INTO 36 ADC1 HSMS-2702 PROG MISO 35 ADC0 34 THERM PWR 3 INT1 SPI SCK 9 USARTI RXD CN3/CN4: mate 33 THRUI B with JST PHR-2 В 32 THRU2 VCC I2C CLK PRPN042PARN housing. 31 THRU 30 RSTN I2C DATA PWM0 PWM1 J1-J3: use Sullins 29 PWM1B 28 VCC SPN02SYBN-RC 2 2 AC+ 4 or equivalent. 27 GNI **R**3 U2B AC-CFR-25JB-100R Π S2B-PH-K-S PRPN022PARN 5 100 DF9-51P-1V(54) ÷ MAX9020EKA-T VCC 27 GND HSMS-2702 ÷ AC+ PWML 28 28 VCC 29 PWM1B 30 RSTN 31 THRU3 32 THRU2 PWM0 4 Note: Polarity of VCC I2C DATA CN3 is opposite polarity of CN4. I2C CLK USARTI TXI 6 33 THRU R4 USARTI RXD 8 SPI SCK 9 IN OUT 34 THERM PWR 35 ADC0 36 ADC1 37 ADC2 C MFR-25FBF-1M00 GND PROG MISO PROG MOSI IM 10 36 ADC1 37 ADC2 38 ADC3 39 ADC4 40 ADC5 41 ADC6 42 AMC6 44 PW6 45 PW4 46 PW3 47 PW2 48 PW1 49 PW0 50 UART 31 UART MAX6018AEUR12-T 11 USARTI CLK 12 PW7 ALE WR 13 14 15 RD LED1 LED2 LED3 CC CCA 16 17 VCC 18 19 20 100 K Title: MOTE-WAKE (2x Large Geophone) INT0 INT1 VDD Author: Sasha Jevtic Revision: 1 22 GND INT2 INT3 VSNSR GND I2C DATA Date: 3/9/2006 Time: 6:52:28 PM 24 I2C CLK SCL SDA MAX5435LEZT-T File: U:\wakeup\hardware\MOTE-WAKE\MOTE-WAKE.SchDoc DF9B-51S-1V(54)

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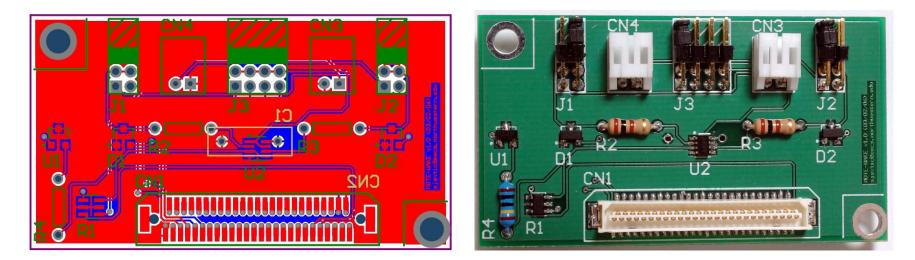
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Another design, all the way to production

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Another simple design, all the way to production



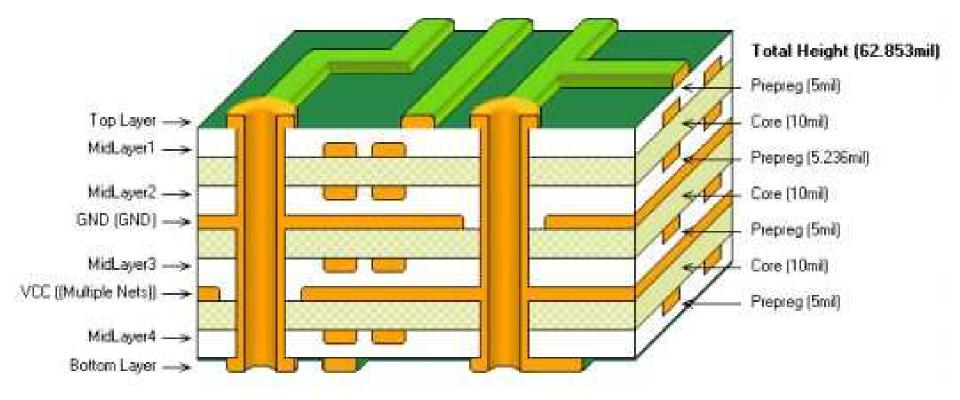
- Simple design that solved a hard problem.
- Deployed at many sites around U.S.

Not a simple design



- Note component density
- Can mount components on each side.
- Relationship between PCB layout, pinouts, and external components important.
 - LED.
 - Battery.
 - Others, e.g., big inductors.
- Form (and board shape) follows function.
- RF subsystem physical design tricky.

The layered construction of a PCB: A six layer board



Doesn't need to be expensive / complex

- Can CAD/CAM mill away solid Cu layer.
- Can use lithography.
 - Photoresist.
 - Mask (can print with laser printer).
 - Projector.
 - Etchant (many are dangerous to breathe and touch).
 - Safe way to dispose of Cu-containing solution.