Interpreting Table 13-3 and 13-2 of the White Book

Table 13-3 of the White Book illustrates the bus contents during byte, ½ word and word write transactions and the associated address and control lines.

Table 13-3. Data Bus Contents for Write Cycles

TRANSFER SIZE	TSIZE [0:1]		INTERNAL ADDRESS		EXTERNAL DATA BUS PATTERN			
			A30	A31	D0–D7	D8–D15	D16–D23	D24–D31
Byte	0	1	0	0	OP0	—	—	—
	0	1	0	1	OP1	OP1	—	—
	0	1	1	0	OP2	—	OP2	—
	0	1	1	1	OP3	OP3	—	OP3
Half-Word	1	0	0	0	OP0	OP1	—	—
	1	0	1	0	OP2	OP3	OP2	OP3
Word	0	0	0	0	OP0	OP1	OP2	OP3

NOTE: — Denotes that a byte is not required during that read cycle.

8-bti data port

16-bit data port

32-bit data port

For example, writing the least significant byte

stb rS, 3(r4)

will place the contents D24-D31 of register rS on D24-D31 of data bus. The register r4 contains a word-aligned address, but the offset of 3 will set A30 and A31 high. In addition the transfer size will be coded as TSIZE[0:1] = 01.

Notice that the processor also places D24-D31 of rS at positions D8-D15 and D0-D7. Why is this? The memory controller is designed to consider the possibility of a 32, 16 and 8 bit data ports. The processor places the data byte in positions for 32, 16 and 8 bit data ports regardless of the data port setting in the memory controller.

Consider the memory contents for a 32-bit memory, 16-bit memory and 8-bit memory for a word write on a word-aligned access.

stb rS, 0(r4)

32 Bit Memory Data Port

A30 A31	Data Bus D0-D7	Data Bus D8-D15	Data Bus D16-D23	Data Bus D24-D31
00	rS(D0-D7)	rS(D8-15)	rS(D16-D23)	rS(D24-D31)

16 Bit Memory Data Port

A30 A31	Data Bus D0-D7	Data Bus D8-D15
00	rS(D0-D7)	rS(D8-15)
10	rS(D16-D23)	rS(D24-D31)

8 Bit Memory Data Port

A30 A31	Data Bus D0-D7
00	rS (D0-D7)
10	rS(D8-D15)
01	rS(D16-D23)
11	rS(D24-D31)

Notice that rS(D24-D31) needs to be in position D24-D31 of the data bus for a 32 bit data port, D8-D15 of the data bus for a 16 bit data port and D0-D7 of the data bus for a 8 bit data port.

In the case of

stb rS, 3(r4)

where r4 is a word aligned address. The memory controller puts the data in all these locations regardless of the port setting in the memory controller to account for any of the three port sizes. You must select the appropriate byte with your control logic.

Keep in mind that the memory controller will always break down an unaligned access into the appropriate combinations of byte and ½ word aligned transactions for a given port size. The memory controller is set up for a 32-bit port. So, your control logic **does not** have to deal with unaligned accesses. If you design your control logic to work according to table 13-3, it will automatically handle unaligned accesses.

Table 13-2 shows the bus contents for memory reads.

Table 13-2. Data Bus Requirements For Read Cycles

TRANSFER SIZE	TSIZE [0:1]		INTERNAL ADDRESS		32-BIT PORT SIZE				16-BIT PORT SIZE		8-BIT PORT SIZE
			A30	A31	D0–D7	D8–D15	D16–D23	D24–D31	D0–D7	D8–D15	D0–D7
Byte	0	1	0	0	OP0	—	—	—	OP0	—	OP0
	0	1	0	1	—	OP1	—	—	—	OP1	OP1
	0	1	1	0	—	—	OP2	—	OP2	—	OP2
	0	1	1	1	—	—	—	OP3	—	OP3	OP3
Half-Word	1	0	0	0	OP0	OP1	—	—	OP0	OP1	OP0
	1	0	1	0	—	—	OP2	OP3	OP2	OP3	OP2
Word	0	0	0	0	OP0	OP1	OP2	OP3	OP0	OP1	OP0

NOTE: — Denotes that a byte is not required during that read cycle.

Notice that the processor selects the appropriate byte for the transaction. So, your logic need only supply then entire word for any transaction. The processor will select the appropriate byte, ½ word or word.