

## Bus Interface Design Problem

For this problem, you need to complete the bus interface to the dipswitches, bar leds and 7 segment leds shown in the High Level schematic. The problem is similar to that of lab 3, except we will use a low power FPGA family that performs somewhat slower than the FPGA used in the lab. Be sure to read the timing specifications carefully.

### Power PC Timing Specifications

TA\* and Data Setup:  $\frac{1}{4}$  clock cycle

TA\* and Data Hold:  $\frac{1}{4}$  clock cycle

### FPGA Timing Specifications

TRI-State Buffer Propagation Delay: negligible

LED Register Data Setup: 2 clock cycles

LED Register Data Hold:  $\frac{1}{4}$  clock cycle

### Memory Map

Switch Location (Word Addressable): 0x3100000

Bar Led Location (Word Addressable): 0x3200000

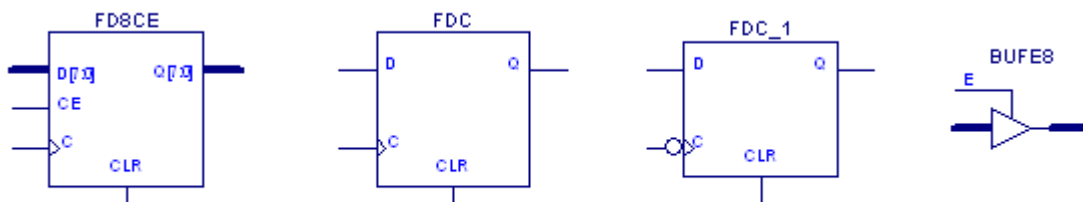
7-Segment Display (Word Addressable): 0x3200000

### Devices Allowed in the Design

You will be asked to complete various parts of the bus interface design. The following components are allowable.

Inverters

AND, NAND, OR, NOR of any size. You may use inverting bubbles on inputs.



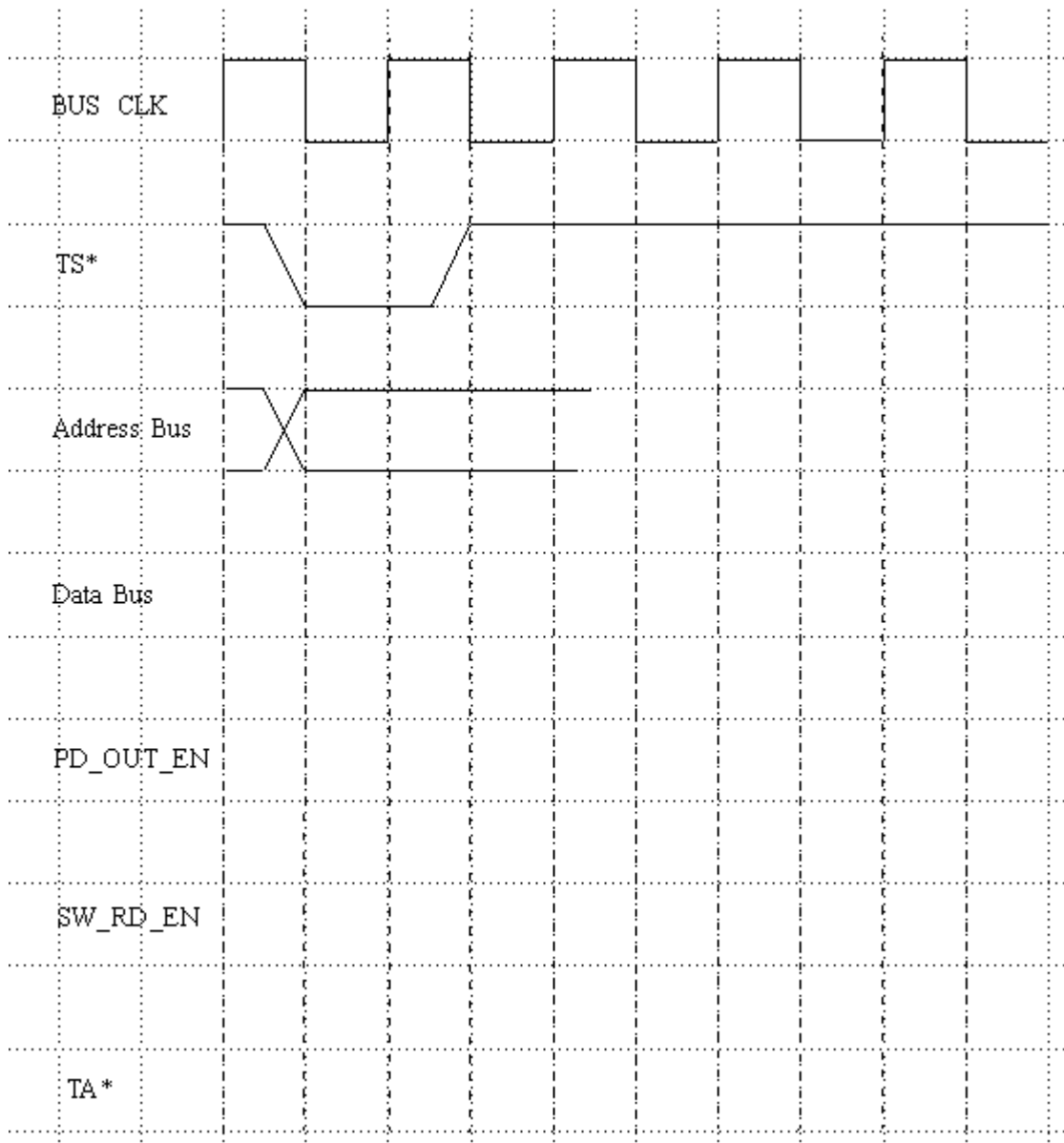
## Timing Study

In lab, we discussed that the design process should start with a timing study. We started by addressing the minimum requirements. We then considered a synchronous solution that would meet the minimums with a safety margin.

### Assignment 1 (%)

Complete the following read cycle timing diagram for a synchronous solution. You should use **no** more WAIT states then necessary.

Show the  $TA^*$ , and processor data setup and hold times your design will **provide**. Illustrate the times as intervals on the timing diagrams.

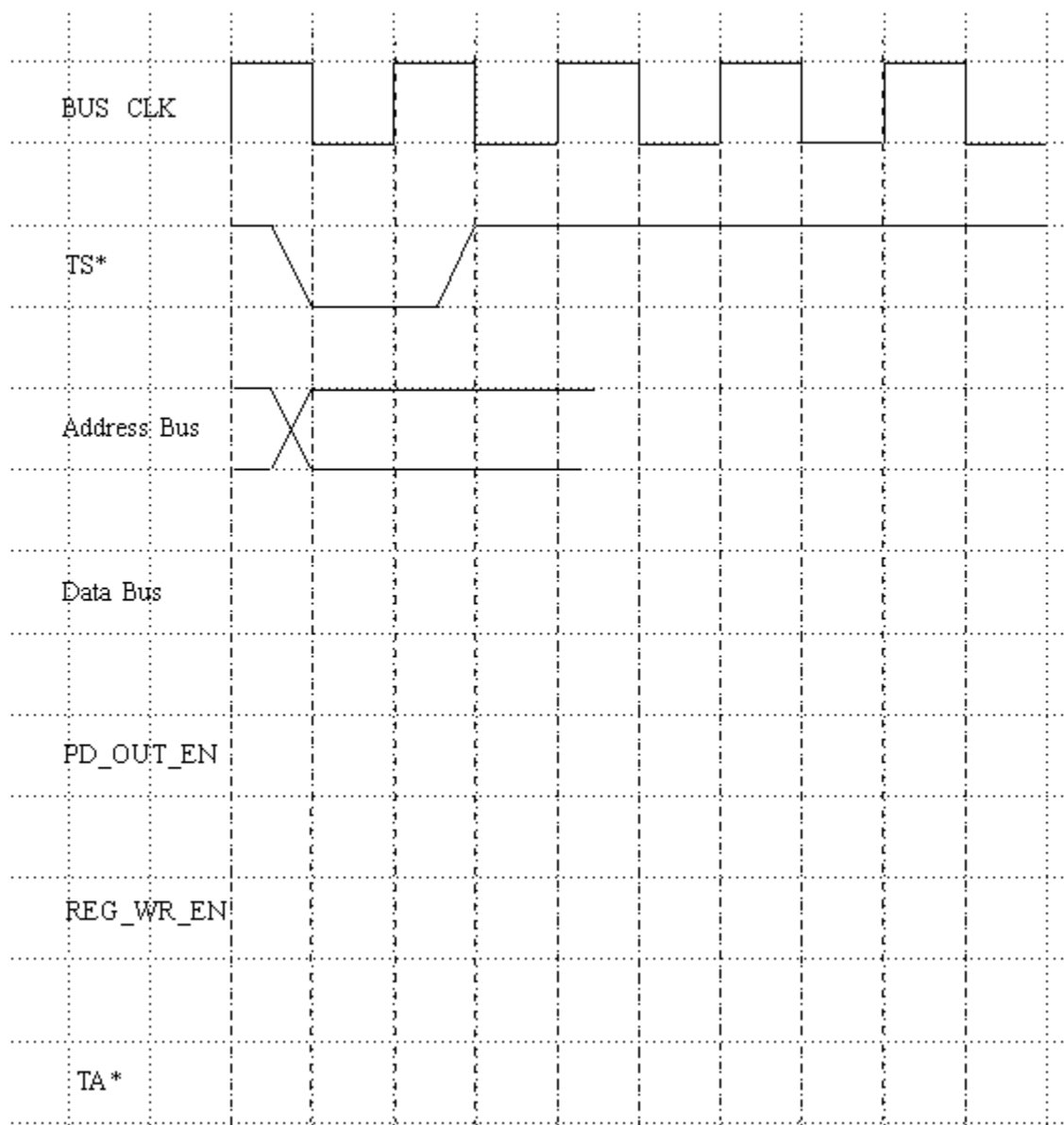


## Assignment 2 (%)

Complete the following write cycle timing diagram for a synchronous solution. You should use **no** more WAIT states then necessary.

Show the LED registers data setup and hold times your design will **provide**. Illustrate the times as intervals on the timing diagrams.

Complete LED registers connections on the High Level schematic. Be sure to show all the connections clearly.



**Assignment 3 (%)**

Provide the logic in schematic form in the space below for the **REG\_WR\_EN** signal in the IO control macro. **You DO NOT have to provide logic for the other control signals.** Clearly label all signals.

#### **Assignment 4 (%)**

In this design, we want to provide a means to read LED registers as well as writing them.

Modify the High Level schematic for the paths and hardware required to implement reading the LED registers. Label all connections clearly. Assume that the BAR led is read on bits 24-31 and the 7-Segment is read on bits 17-23.

#### **Assignment 5(%)**

If the Led registers were upgraded to be byte write addressable:

What input and output control signals do you have to add to the address decoder?

Assuming the address 0x3200000 is decoded as AD32 (active high), provide the **Boolean** expressions for the LED registers byte write control signals. Use \* for AND, | for OR and ~ for inversion.

You **do not** have to provide any modifications to the IO\_Control Macro.

## **Assignment 4 (additional space)**

# HIGH LEVEL SCHEMATIC

