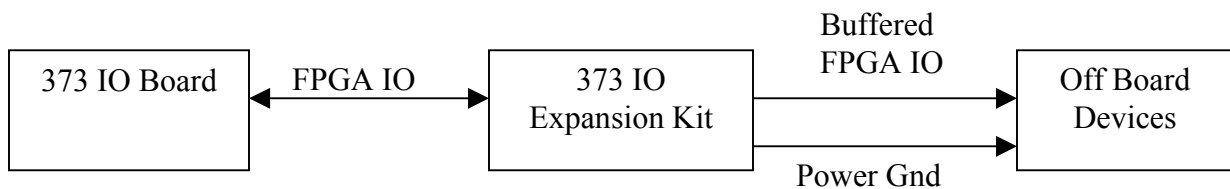


373 IO Expansion Kit

12/22/07

During the project phase of the course, it will be necessary to interface the lab kits to various off kit devices such as displays, sensors and actuators. Forty pins of general-purpose FPGA inputs or outputs (GPIO) are available via the 373 IO board expansion connector.

To facilitate connections and protect the FPGA an IO expansion kit is provided. The kit consists of an interface board integrated into a general-purpose proto-board. Connections to devices are simply made via hookup wire and a general-purpose proto-board alleviating the need to make special purpose connections by soldering or crimping.

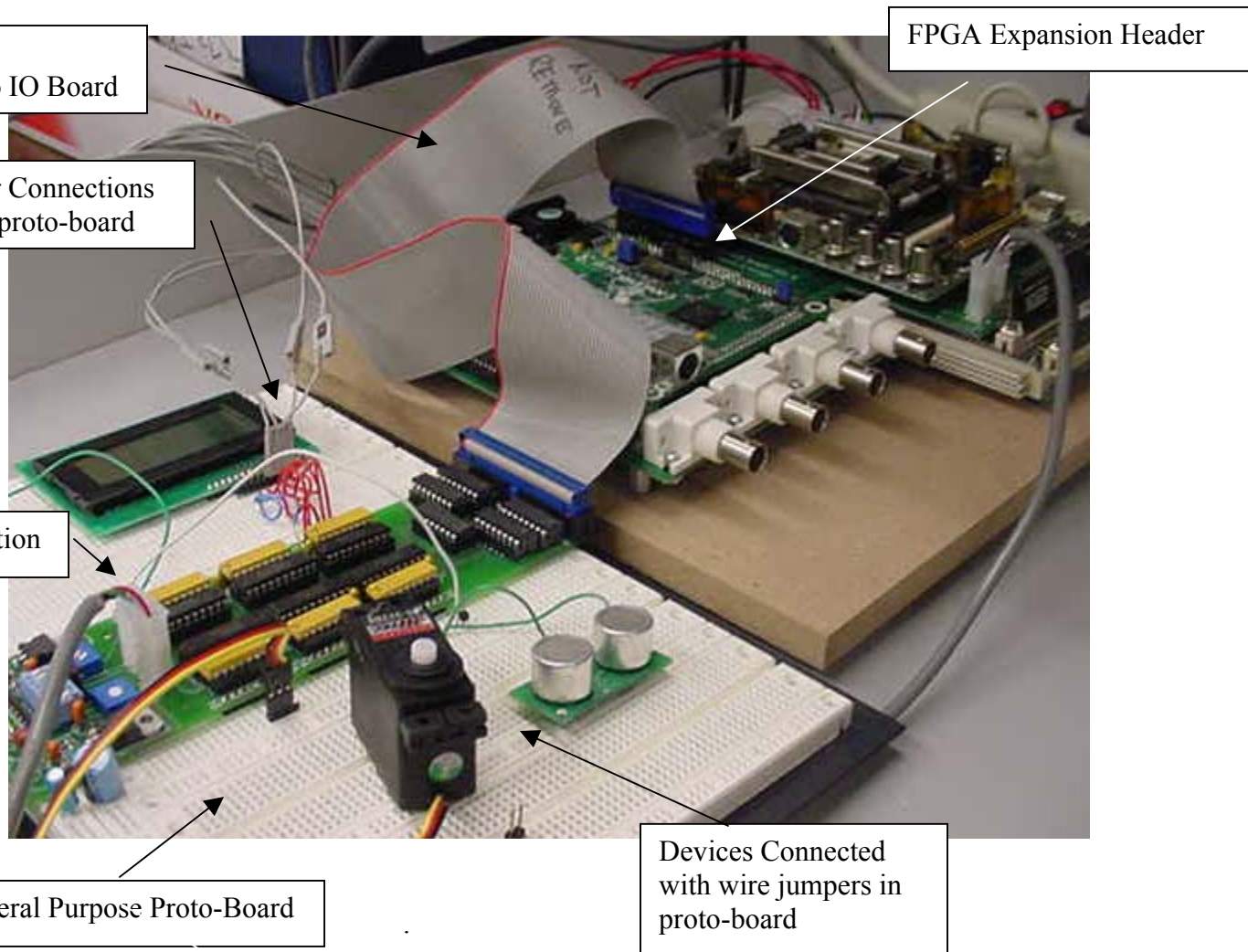


The kit consists of an interface board integrated into a general-purpose proto-board. The kit connects to the 373 IO board via a ribbon cable and power cable. Each project group will be provided an expansion kit for the duration of the project. Keep the kit in your project box with the connections to your devices. You can disconnect the kit by simply removing the ribbon cable and power connections.

Disconnecting the IO Expansion Kit

1. Turn off lab kit power supply.
2. Disconnect the power cable from the IO expansion kit.
3. To remove, push locking tab and lift gently.
4. **Leave the power cable connected to the station kit!!!**
5. Remove the ribbon cable from the expansion kit.
6. To remove, rock it gently and pull upward
7. **Leave the ribbon cable connected to the station kit!!!**

IO Expansion Kit Connected to 373 IO Board

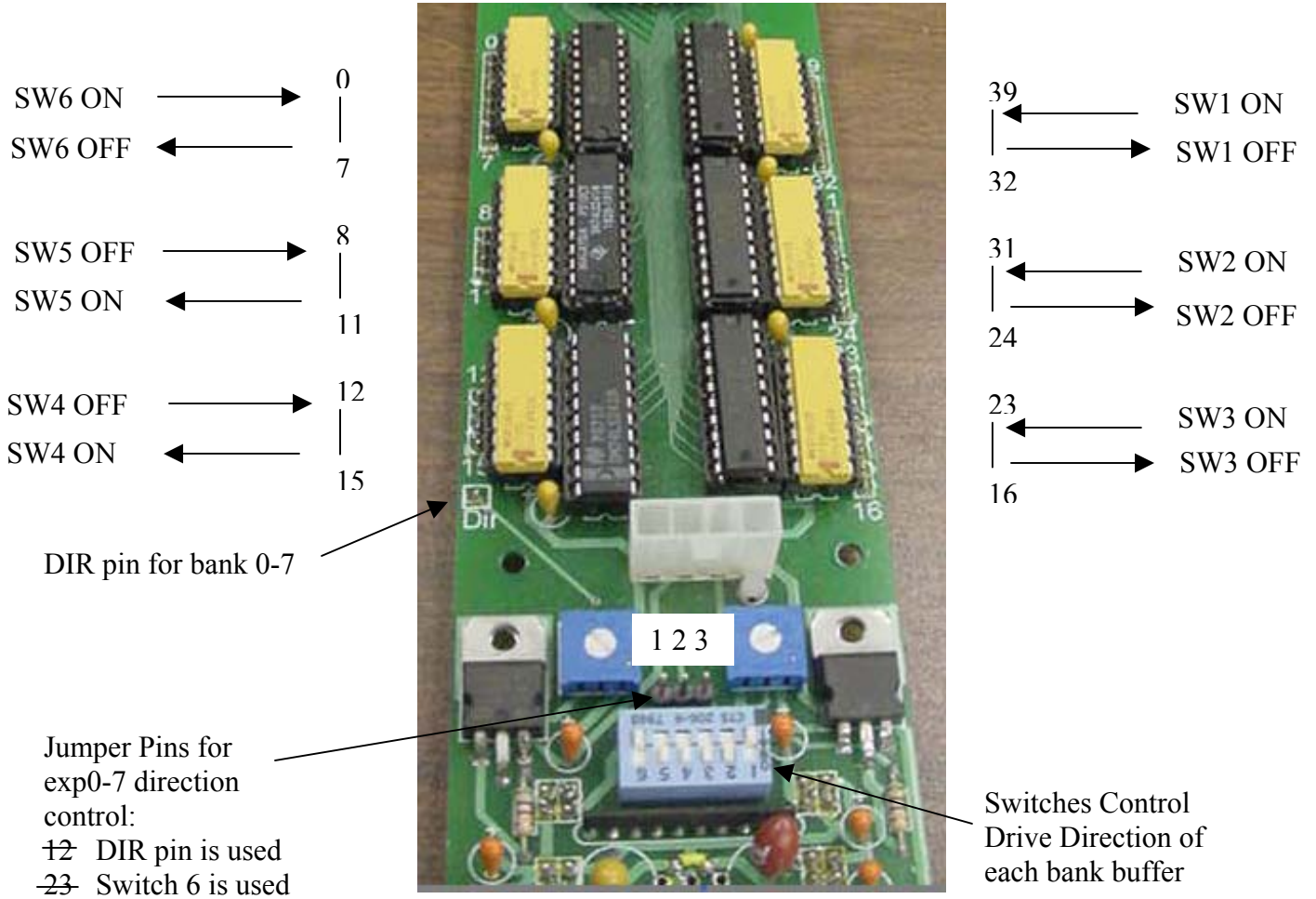


IO Bank Organization

The FPGA GPIO are electrically isolated with 74LS245 (8 bit) and 74LS241 (4 bit) buffers on the expansion card. The buffers protect the FPGA outputs and provide increased voltage and current drive to devices. A control pin determines the drive direction of each 8 or 4-bit buffer. Consequently, expansion board IO is organized into 4, 8-bit and 2, 4-bit banks. List the IO you will need for your project and organize it in banks of 8 or 4 bit inputs or outputs. The banks are organized as shown below:

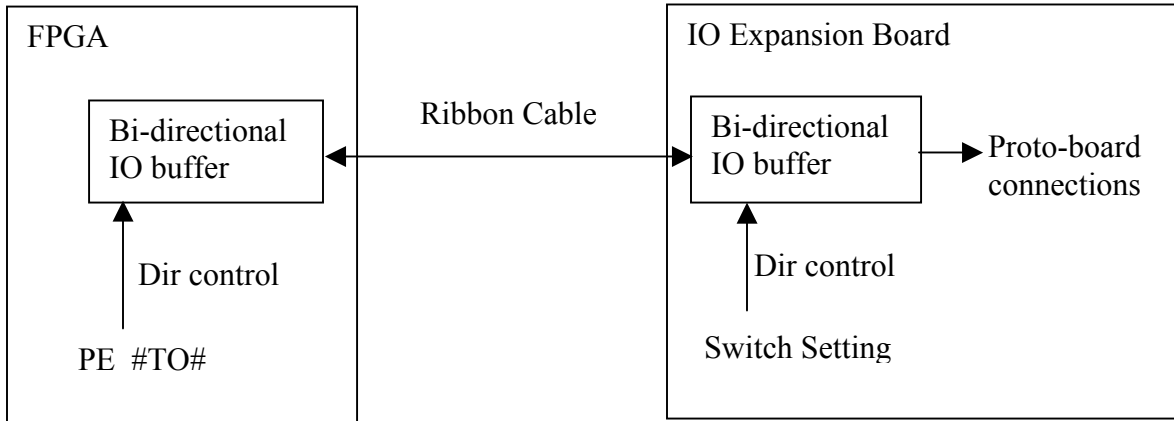
Expansion Kit IO Mapping and Direction Control

The IO expansion kit is organized into 6 banks of 8 and 4 IO expansion pins. They are mapped as follows:



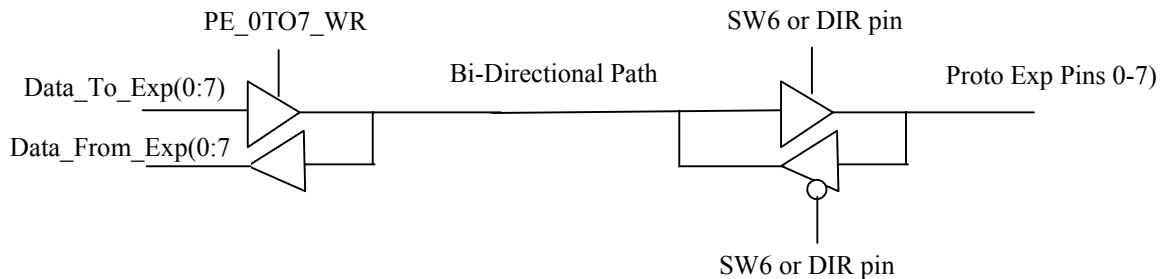
Coordinating FPGA IO Buffers and IO Expansion Board Buffers

The ribbon cable is a bi-directional bus connection between the expansion board and FPGA. To avoid bus contention, the bi-directional drivers must be set correctly on both ends.



For example, to write expansion bank 0-7:

1. PE_0TO7_WR set to logical 1
2. SW6 is set to OFF or DIR is set to logical 1



Bank 0-7 bi-directional buffer is optionally controlled by the DIR signal. The option is selected via the jumper on the IO expansion board near the dipo switches.

All other expansion board bi-directional buffers are only controlled via switches. You must organize your project IO accordingly.

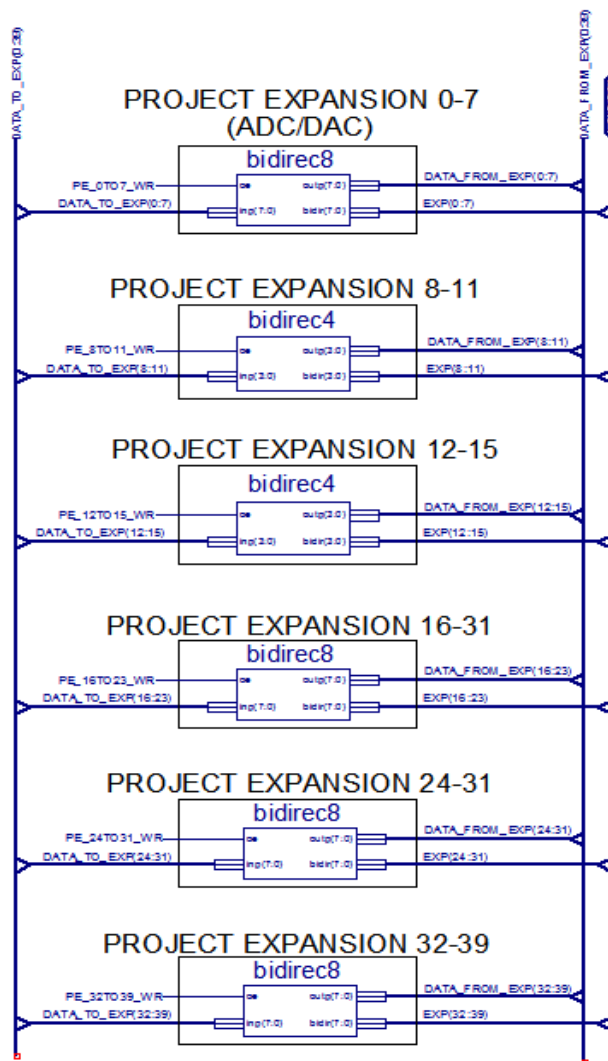
ISE Project Expansion Connections

A special ISE base project is posted with the project materials providing IO connections to the expansion IO and DACs. Of course, connections to the IO used in lab 8 are provided too, but you will see the organization is a bit different.

The expansion IO connections are organized into the respective banks. Since each bank may be either an input or output, the connections are made via bi-directional buffers.

When you open the project, you will notice that the bi-directional buffer path to the ADC is now integrated into the expansion connector since this bank is shared with the ADC and DAC.

When you open the project, you will notice that the TP0-7 ISE connection is no longer provided since it is shared with expansion bank 32-39.



Expansion Board Pin Mapping and Control

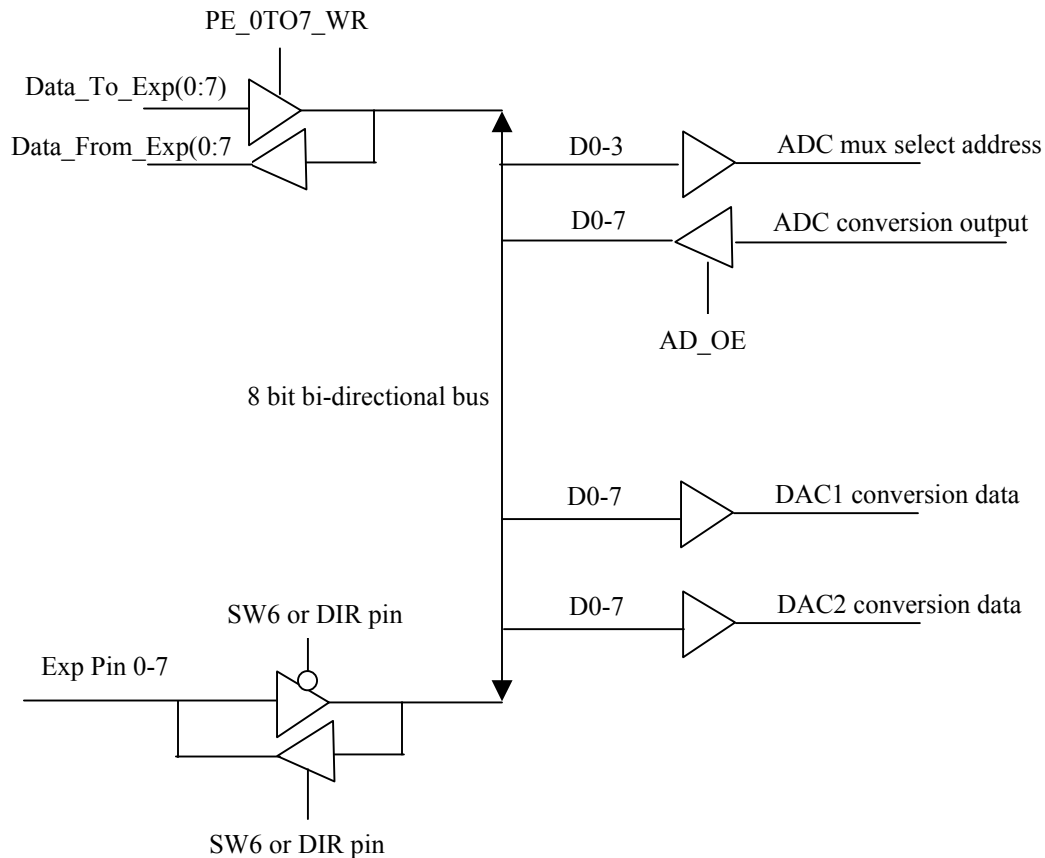
Exp Pin	IO R/W	ISE Expansion Control	Switch Setting	Jumper Setting	DIR pin	Sharred IO
0	R/W	PE_0TO7_WR = DIR		connect 1,2	1=OUT, 0=IN	ADC/DAC DB0
1	R	PE_0TO7_WR = 0	SW6=ON	connect 2,3		ADC/DAC DB1
2	W	PE_0TO7_WR = 1	SW6=OFF	connect 2,3		ADC/DAC DB2
3						ADC/DAC DB3
4						ADC/DAC DB4
5						ADC/DAC DB5
6						ADC/DAC DB6
7						ADC/DAC DB7
8	R	PE_8TO11_WR = 0	SW5=OFF			
9	W	PE_8TO11_WR = 1	SW5=ON			
10						
11						
12	R	PE_12TO15_WR = 0	SW4=OFF			DAC_WR1
13	W	PE_12TO15_WR = 1	SW4=ON			ADC_CLK
14						DAC_WR2
15						suggested for DIR
16	R	PE_16TO23_WR = 0	SW3=ON			
17	W	PE_16TO23_WR = 1	SW3=OFF			
18						
19						
20						
21						
22						
23						
24	R	PE_24TO31_WR = 0	SW2=ON			
25	W	PE_24TO31_WR = 1	SW2=OFF			
26						
27						
28						
29						
30						
31						
32	R	PE_32TO39_WR = 0	SW1=ON			TP7
33	W	PE_32TO39_WR = 1	SW1=OFF			TP6
34						TP5
35						TP4
36						TP3
37						TP2
38						TP1
39						TP0

Note 1: Switch settings are the opposite for 8 and 4 bit buffers.

Note 2: If the ADC or DAC are not used, exp 12-14 may be used for general purpose IO.

Extending the ADC/DAC Device Bus to the Expansion Port 0-7

From lab 8 we know that the ADC/DAC share an 8 bit bi-directional bus. The output of the ADC is read on this bus and the ADC analog mux address and DAC conversion value are written on this bus. This bus can be extended to off board 8 bit devices such as displays thru expansion port 0-7. The complete data path follows:



Care must be taken to avoid bus contention when driving the 8 bit bi-directional bus. That is, only one driver can be activated at a time. For example, to write the ADC mux register:

1. PE_0TO7 must be logical high (ACTIVE)
2. AD_OE must be logical low (INACTIVE)
3. SW $\bar{6}$ must be OFF or DIR must be logical 1 (INACTIVE)

Notice that the expansion port 0:7 on the expansion board must be set to write the expansion pins to avoid driving the 8-bit bi-directional bus when attempting to read or write the ADC or DAC. So, devices attached to the expansion port 0:7 could be affected by these writes. The port is intended for use with devices that require an 8-bit data path such as the LCDs or other devices that have parallel read/write registers. These devices

can be disabled during ADC or DAC accesses by disabling device output enables and/or latch enables. For example, assume that a LCD character display is attached to the expansion port 0:7. Assume it has a data register that is clocked on the rising edge of control signal LATCH_DISPLAY. Then the previous write conditions of the ADC mux register would include:

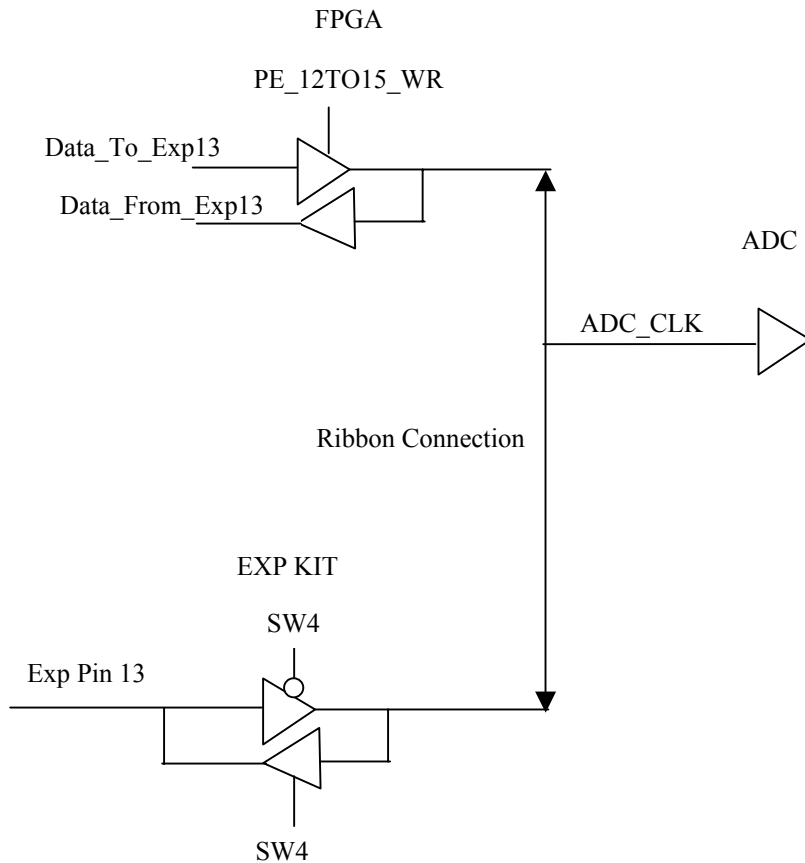
1. PE_0TO7 must be logical high (ACTIVE)
2. AD_OE must be logical low (INACTIVE)
3. SW6 must be OFF or DIR must be logical 1 (INACTIVE)
4. LATCH_DISPLAY must be logical 1 or 0 but not in transition.

Be sure that the control signals associated with external devices attached to the expansion port 0:7 are disabled when using the ADC or DAC.

Device that cannot be disabled when using the ADC or DAC cannot be attached to the expansion port 0:7.

ADC Control Signals

All the ADC control signals are mapped uniquely from the FPGA to the ADC except the conversion clock ADC_CLK. The pin is shared with expansion connection 13. When using the ADC this pin cannot be used as an expansion pin. Furthermore, it is necessary set the expansion board buffer appropriately to avoid driving the ADC_CLK pin from the expansion board. See the following figure:

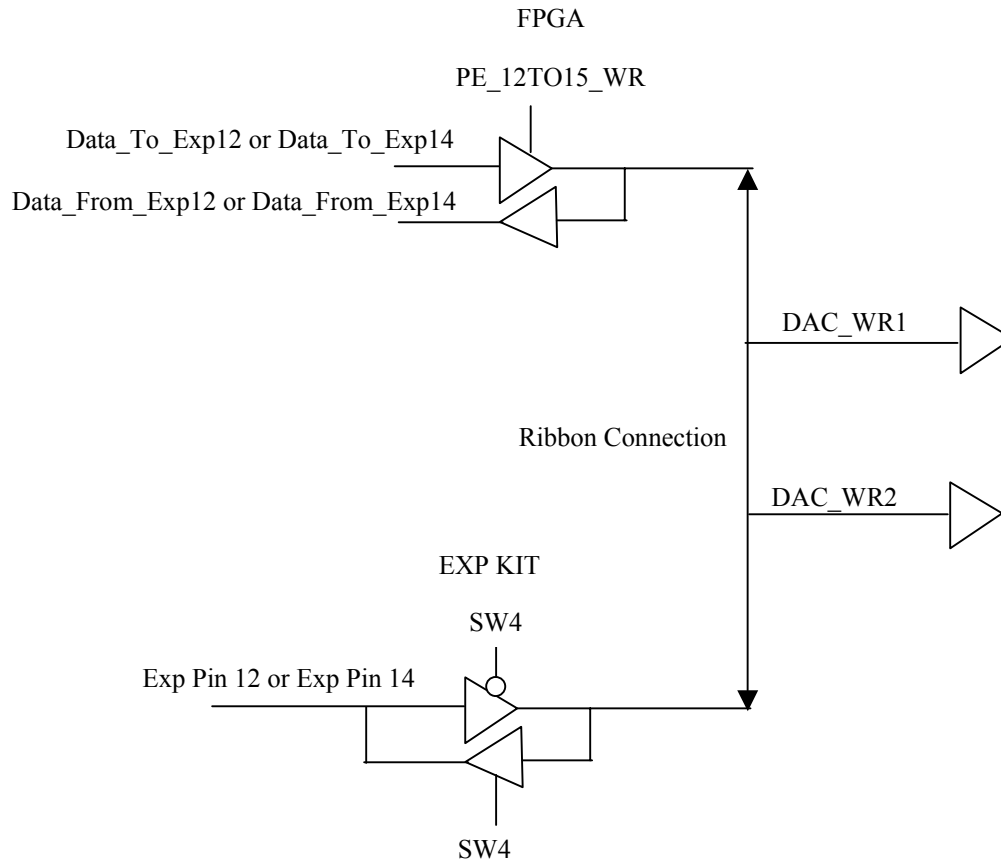


For example, to drive the ADC_CLK:

1. Map `Data_To_Exp13` to a conversion clock source
2. Set `PE_12to14_WR` to logical 1
3. Set `SW4` to ON

DAC Control Signals

The DAC write control signals DAC_WR1 and DAC_WR2 are shared with expansion connections 12 and 14 respectively. When using the DAC, the expansion pins cannot be used. Furthermore, it is necessary set the expansion board buffer appropriately to avoid driving the ADC write controls from the expansion board. See the following figure:

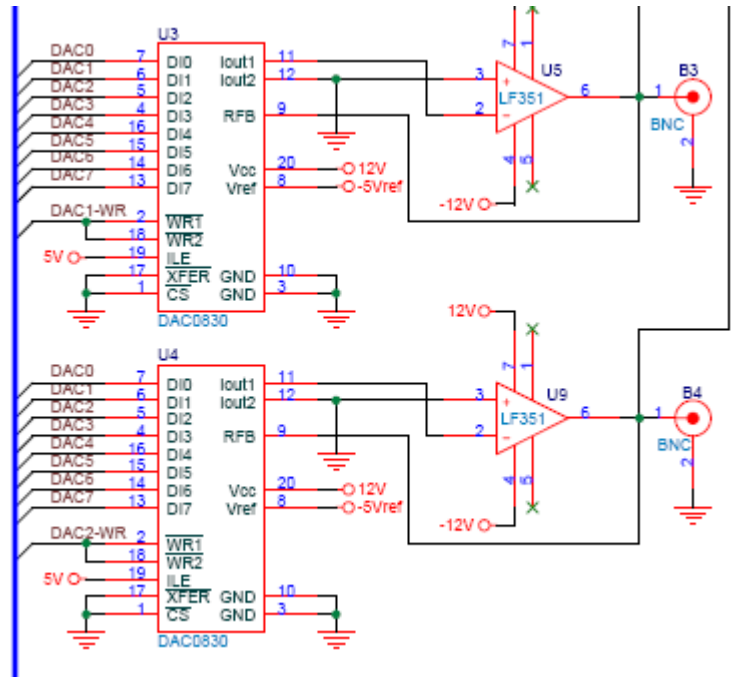


For example, to map the DAC_WR1 signal:

1. Map a DAC write control signal to Data_To_Exp12
2. Set PE_12To15_WR to logical 1
3. Set SW4 to ON

DAC Control Signals cont

When you read the DAC data sheet you will see several other control signals listed. These control signals are not accessible. Instead, they have been “hardwired” on the circuit board to an active state. See the following schematic excerpt:



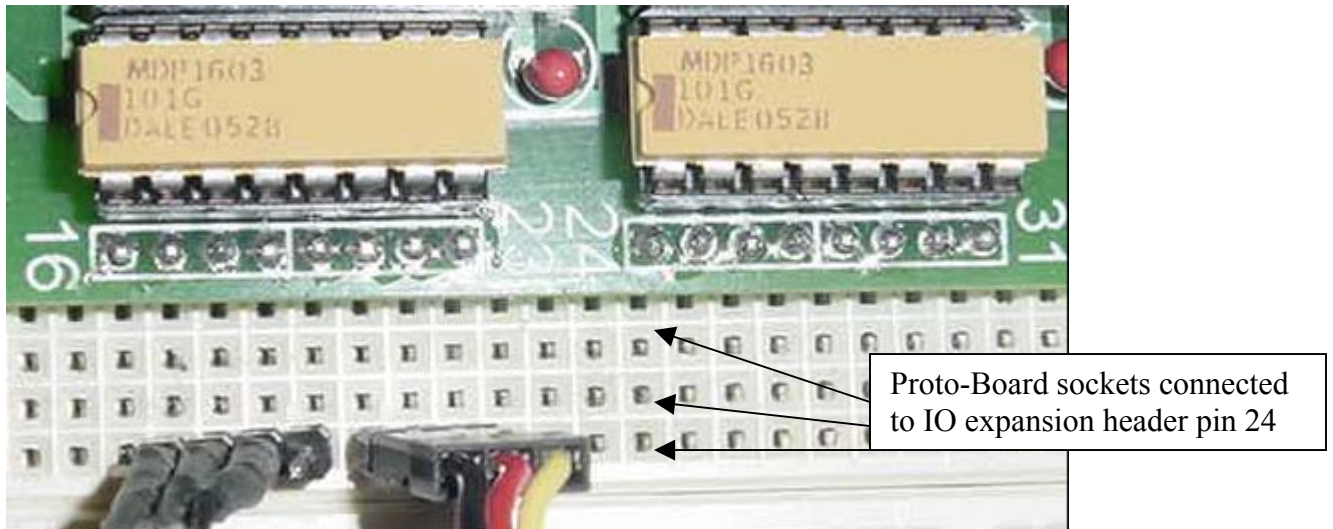
It is only necessary to provide the write control signals to initiate conversions and latch data into the DACs. The DACs will convert the range $0 \rightarrow 0xff$ to $0 \rightarrow 5$ volts. If you need more or less range, an external DC amplifier can be used. Be sure to read the DAC specification for details regarding setup and hold time to latch the DAC input data.

DIR Control Signal

Some devices such as the graphics display require both read and write operations under software control. When extending the 8 bit device bus to these devices via expansion path 0-7, the DIR pin can be used to control expansion board directional buffers instead of SW6. If you are using either the DAC or ADC, it is efficient to use expansion pin 15 to control the DIR since it is necessary to set this bank as a expansion board write bank. Of course, if the ADC or DAC control lines are not being used they can be used to general purpose outputs.

Making Connections to the IO-Expansion Board

The interface board is connected to a general-purpose proto-board via pins under the board providing connections to the FPGA IO. The interface board is labeled with corresponding 373 IO Expansion Header pin numbers. The immediate row of proto-board sockets is connected to the respective expansion header pin. For example,



Expansion Kit Supply Voltages

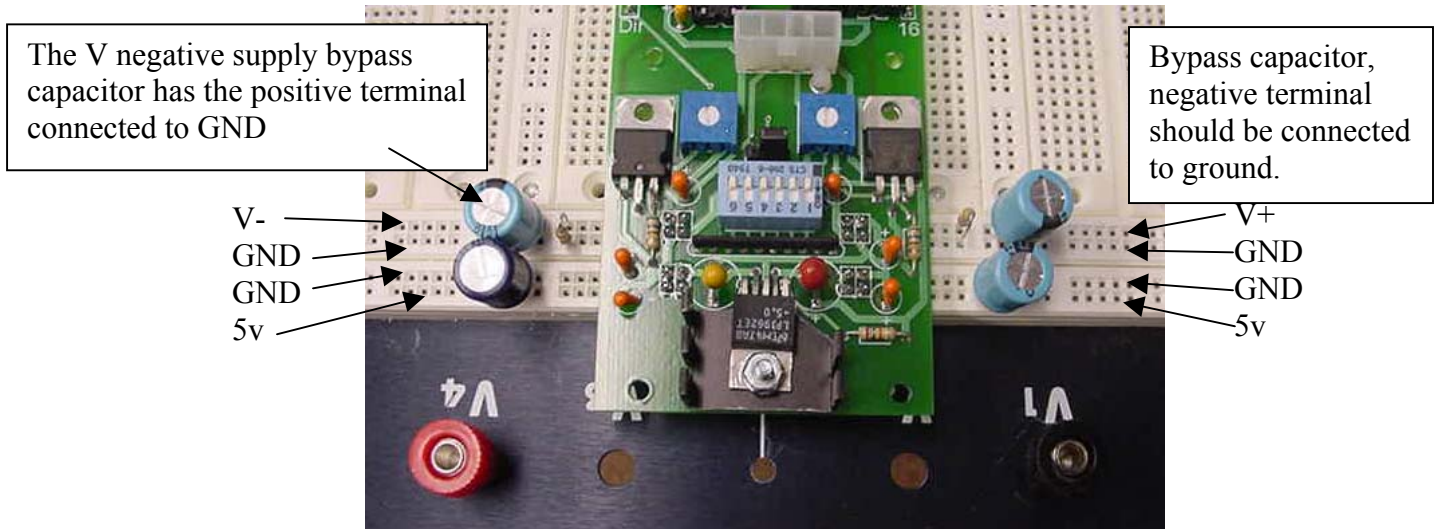
The expansion kit provides 3 supply voltages for signal conditioning circuits and devices. The supplies are for low power devices and signal conditioning circuits. If you need more, a lab supply or alternate will have to be used. Ask your lab instructor if you are not sure. The following table lists the supply limitations.

Voltage	Adjustment	Maximum Current
5+ volt	fixed	0.5 amp
V+ volt	2 \rightarrow 10 volts	0.5 amp
V- volt	-2 \rightarrow -10 volts	0.5 amp

The variable supplies are adjusted by the potentiometers on the interface board with a small screwdriver. Adjust and measure with a meter or your scope for the desired voltage.

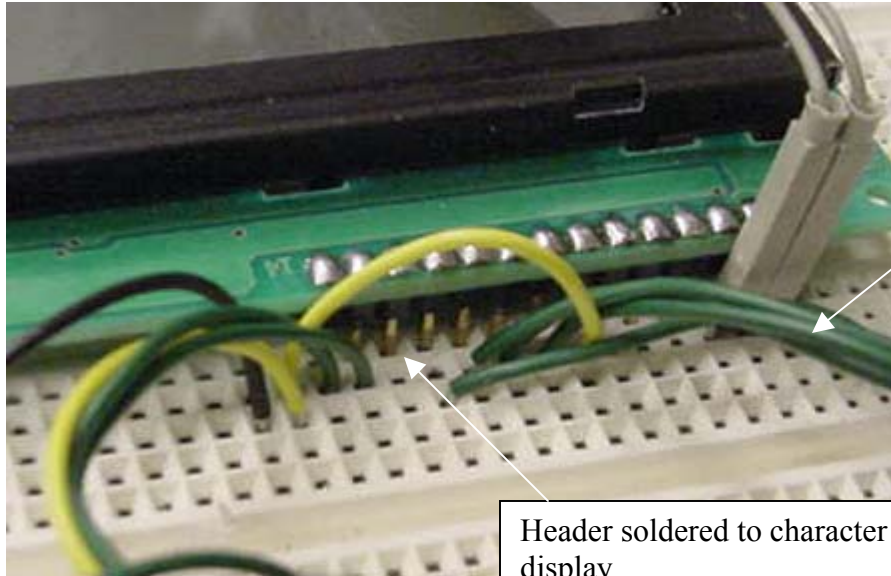


The voltage sources are connected under the interface board to the top rows of the general-purpose proto-board. See below for the mapping. Bypass capacitors should be installed on the power supply rows for supply filtering.



Connecting Devices

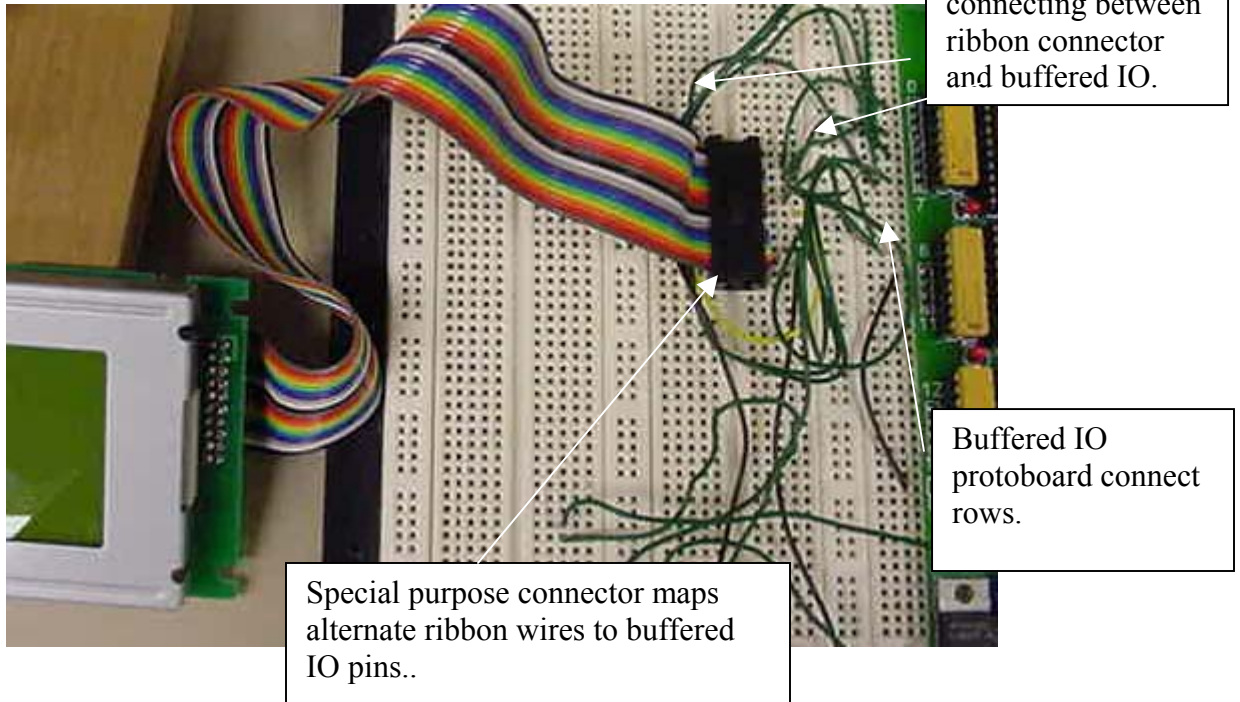
Several standard 373-project devices are equipped with headers (pins) that allow you to plug the board directly into the proto-board. Then it is a simple matter of connecting with hookup wire to achieve the desired mapping between your device and the FPGA IO. The standard character display is one such device.



Hookup wire connecting to interface board

Header soldered to character display

Some devices are not conveniently fitted with single row headers for easy plug in to the proto-board. The standard graphics display is fitted with a dual row header that will not plug into adjacent independent rows on the proto-board. In this case you will have to use a ribbon cable that connects the display header to a connector that accommodates the proto-board layout. Connections can then be made with hookup wire to the interface board.



Project Expansion Board Test Logic

The ISE Expansion Board base project includes logic to perform a basic test of all the expansion port pins. Although the boards are tested between projects, some pins may have been overlooked or during the course of the projects you may have smoked one of the ports. You should try the test to be sure you understand how the expansion board ports work and to check your expansion board. Of course, you can remove the test logic when you develop your project. If you need to test later during project development, simply download the project base project.

The test logic allows you to test each bit of the expansion port EXP0-39 for read/write functionality. The logic maps the slide switches of your kit to each port for write testing and maps the 7segment and bar led displays to each port for read testing. The test logic organizes the expansion banks in pairs so that a bank set up for a write test may be connected to a bank for a read test.

For example, expansion banks exp0-7 and exp31-39 are one such pair. To perform a read/write test for this bank, start by connecting the banks with jumper wires one to one. That is exp0→exp31, exp1→exp32, etc. Then set exp0-7 to write the slide switches to the expansion board and exp31-39 to read the expansion board to the led displays. The display should represent slide switch settings. Alternatively, set exp31-39 to write the slide switches to the expansion board and exp0-7 to read the expansion board to the led displays.

The following table lists all the settings for each bank pair test.

A few notes:

- The expansion board jumper 123 should have jumpers 23 connected for these tests.
- The slide switches are mapped to the displays little endian. Remember the 7 segment displays contain binary to hex encoders. So, for example:
 - SW(7:0) = 0b00000001 → 7 seg display = 1
 - SW(7:0) = 0b00000010 → 7 seg display = 2
 - SW(7:0) = 0b00000100 → 7 seg display = 4
 - SW(7:0) = 0b00001000 → 7 seg display = 8
- To distinguish between a read or write problem, observe the write outputs on the expansion board with the scope, logic analyzer or multimeter. If the write pattern is observed, it is probably a read problem
- If you find a problem, notify the lab instructor and the appropriate components are usually easy to replace.

expansion port mapping (write)	expansion port mapping (read)	exp board bank RD/WR dipswitch	FGPA board pusbuttons	comments
sw(0:7)-->exp(0:7)	exp(31:39)-->7seg(0:7)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP DN *	connect exp proto-board exp(0:7) --> exp(31:39)
sw(0:7)-->exp(31:39)	exp(0:7)-->7seg(0:7)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP * DN	connect exp proto-board exp(0:7) --> exp(31:39)
sw(0:7)-->exp(16:23)	exp(24:31)-->7seg(8:15)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP DN *	connect exp proto-board exp(16:23) --> exp(24:31)
sw(0:7)-->exp(8:15)	exp(16:23)-->7seg(8:15)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP * DN	connect exp proto-board exp(16:23) --> exp(24:31)
sw(0:3)-->exp(8:11)	exp(12:15)-->barleds(0:3)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP DN *	connect exp proto-board exp(8:11) --> exp(12:15)
sw(0:3)-->exp(12:15)	exp(8:11)-->barleds(0:3)	SW 1 2 3 4 5 6 ON * OFF *	PB 0 1 2 3 UP * DN	connect exp proto-board exp(8:11) --> exp(12:15)