7.6 A 1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-Chip Signaling (IIS)

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Decreasing path length is a key to increasing bandwidth and reducing dissipation in chip-to-chip communications. "System in a Package" reduces the chip distance significantly, providing strong motivation to develop a high-speed, low-power interface. Three technologies are reported. These are a three-dimensional integrated circuits (3D-ICs) with high-density vertical interconnections [1], an ac-coupled interconnection between a chip and a multi-chip module substrate [2], and a wireless superconnect (WSC) where two chips are stacked face-to-face and capacitive coupled [3]. Issues in 3D-ICs are yield degradation due to difficulty in screening a known good die and cost increase caused by additions in process complexity. In the second technology, inter-chip distance cannot be shorter than the chip size. WSC solves all these limitations. Chips are tested before assembly by the wireless interface without process addition, and they are placed within microns of each other. Moreover, the non-contact interface removes a highly capacitive ESD protection structure to reduce delay, power, and area. A remaining issue is that WSC cannot be used for connection of more than three chips for which the communication distance is several hundred microns.

In this paper, a multi-drop bus for more than three stacked chips is presented. Figure 7.6.1 illustrates an overview of the proposed Inductive Inter-chip Signaling (IIS). Chips are stacked face up and inductively coupled by metal spiral inductors. Power and clock signals are provided to them by a bonding wire or inductive coupling. Transition of the transmitting data (Txdata) causes a current change in a transmitter inductor (dI_T/dt). It generates small voltage signals in receiver inductors (V_R) which are converted to digital signals as receiving data (Rxdata). V_R is given by $V_R=k\sqrt{L_R L_T}(dI_T/dt) \propto n_R n_T (dI_T/dt)$, where k is a constant determined by distance and feature size of inductors, The parameter n_R (n_T) is number of turns of the receiver (transmitter) inductors.

Advantages of inductive coupling (L-coupling) over capacitive coupling (C-coupling) result from device scaling. As indicated in the above equation, V_R is increased by increasing number of turns of the inductors. Transmission gain is increased by exploiting an increased number of the metal layers, whereas in C-coupling only the topmost metal layer is utilized. Another advantage is accrues when supply voltages are lowered in scaled devices. Transmission power increases in current-mode signaling with L-coupling, while it is limited by supply voltages in voltage-mode signaling with C-coupling. Figure 7.6.2 depicts the simulated magnetic field when three chips are stacked and operated at 1V. In the L-coupling V_R of 65mV is generated at distance of 180μm, while in the C-coupling it is as small as 0.4mV. It is noted that reflection or absorption is much smaller in the L-coupling, since the permeability (μ) is about the same while permittivity (ε) changes in semiconductor devices.

An equivalent circuit of the inductive coupling is analyzed, and the transfer function is derived as depicted in Fig. 7.6.3(a). It is considered that the transmitter (Tx) corresponds to the second-order low pass filter, magnetic coupling to a differentiator, and the receiver (Rx) to the first-order low pass filter. In total, the inductive coupling behaves as a band pass filter. The pass band is designed around the major frequency of Txdata. It is expected that the inductive coupling tolerates noise from LSI circuits if its frequency is lower than the cutoff frequency (typically some hundreds of MHz), but it is protected from ambient noise by magnetic shielding in a package. A simple yet accurate model is developed by using Biot Savart's law to extract L and k from a layout. Calculations using the model agree very accurately agree with simulation using parameters extracted by FDTD (Finite Difference Time Domain) analysis as shown in Fig. 7.6.3(b).

Circuit diagram of a transceiver is depicted in Fig. 7.6.4, and operating waveforms by SPICE simulation are shown in Fig. 7.6.5. The transmitter is implemented by an H-bridge circuit where I_T flows for a period of delay ($T_{transmit}$) by a delay buffer. The shorter $T_{transmit}$, the smaller power dissipation in Tx, but the smaller timing margin to capture V_R. For the purpose of experimental exploration, $T_{transmit}$ is set as wide as 600ps. With accurate timing control using DLL (Delay Locked Loop), $T_{transmit}$ is shortened. In the receiver V_R is detected by a sense-amplifying flip-flop (SA-FF) which is activated by R_{xclk} with appropriate timing and duration. If the rising edge of R_{xclk} is too early or too late, Rx reads erroneously due to noise. The duration time, T_{sense}, should be long enough for detecting small V_R. But if it is too long, Rx operates erroneously because of noise when the same data continues in Non Return to Zero(NRZ) signaling. These timing constraints are investigated by using SPICE simulation and the results are summarized in Fig. 7.6.6 which indicates the timing margin window is wide enough. The simulation takes account of parasitic effects in layout, as well as mismatch in device pairs. The noise in V_R early in the precharge phase in Fig. 7.6.5 is caused by voltage change in the internal nodes of SA-FF in precharging. The noise is sufficiently diminished if the precharge ($T_{precharge}$) period is longer than 340ps.

A test chip was designed and fabricated in a 0.35μm CMOS technology. Chip thickness is 300μm, corresponding to a stack of five chips [4]. Two chips are stacked face up and assembled in a package as shown in the photomicrograph in Fig. 7.6.7. Several different sizes of transceivers are arranged in various pitches to raise the probability of finding transceiver pairs in good alignment. Clock timing and duty ratio are changed by 70ps steps by digital control. A 32b FIFO with Linear Feedback Shift Register (LFSR) is implemented to measure the BER. Timing margin is measured by changing T_{sense} and the difference between the rising edges of R_{xclk} and T_{xclk} (ΔT). The results are plotted in Fig. 7.6.6. Measured results agree very well with the simulation results. Correct operation at T_{sense} of 470ps and $T_{precharge}$ of 340ps corresponds to 1.2Gb/s data rate. Power dissipation at that rate is 43mW in Tx and 2.5mW in Rx.

Acknowledgements:
The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References:
[1] J. Burns et al., "Three-Dimensional Integrated Circuits for Low-Power, High-Bandwidth Systems on a Chip," *ISSCC Dig. Tech. Papers*, pp. 268-269, Feb. 2001.
[2] S. Mick et al., "4Gbps High-Density AC Coupled Interconnection," 2002 CICC, pp. 133-140.
[3] K. Kanda et al., "1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Dig. Tech. Papers*, pp. 186-187, Feb. 2003.
[4] M. Usami et al., "Powder LSI: An Ultra Small RF Identification Chip for Individual Recognition Applications," *ISSCC Dig. Tech. Papers*, pp. 398-399, Feb. 2003.

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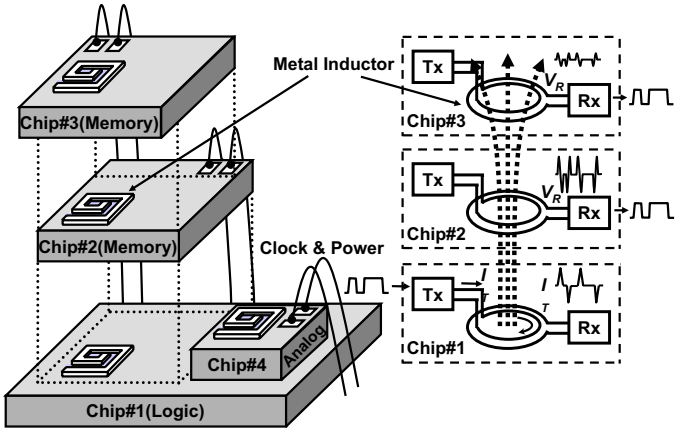


Figure 7.6.1: Inductive Inter-chip Signaling (IIS).

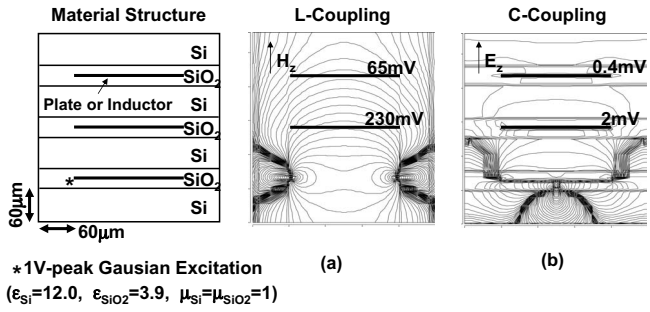
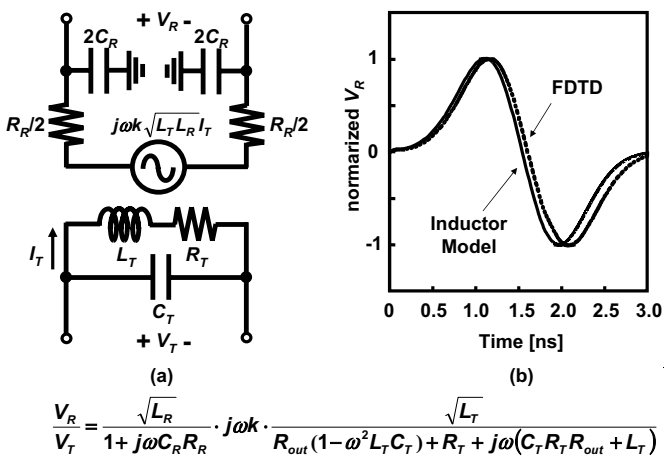


Figure 7.6.2: Electromagnetic field, (a) inductive coupling, (b) capacitive coupling.



$$\frac{V_R}{V_T} = \frac{\sqrt{L_R}}{1 + j\omega C_R R_R} \cdot j\omega k \cdot \frac{\sqrt{L_T}}{R_{out}(1-\omega^2 L_T C_T) + R_T + j\omega(C_T R_T R_{out} + L_T)}$$

Figure 7.6.3: Inductor design, (a) equivalent circuit and transfer function, (b) comparison of proposed inductor model to FDTD analysis.

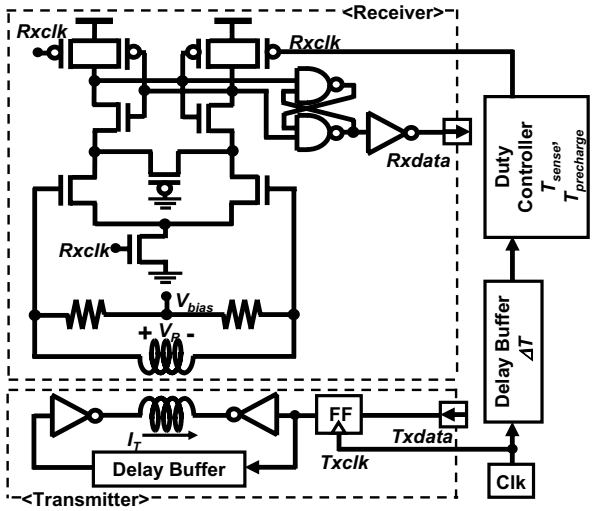


Figure 7.6.4: Transceiver circuit diagram.

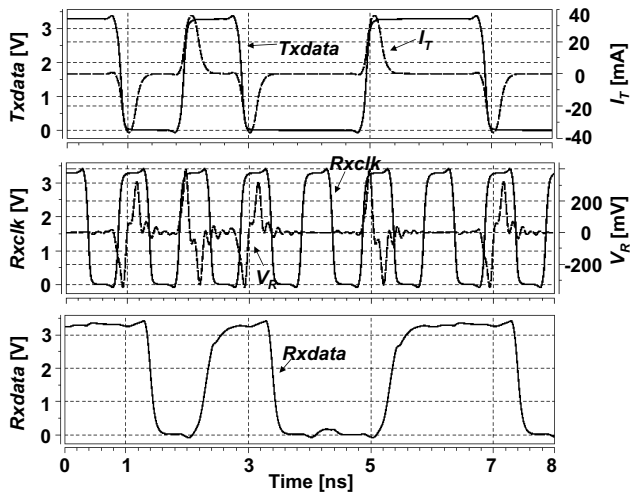


Figure 7.6.5: Operating waveform (SPICE simulation).

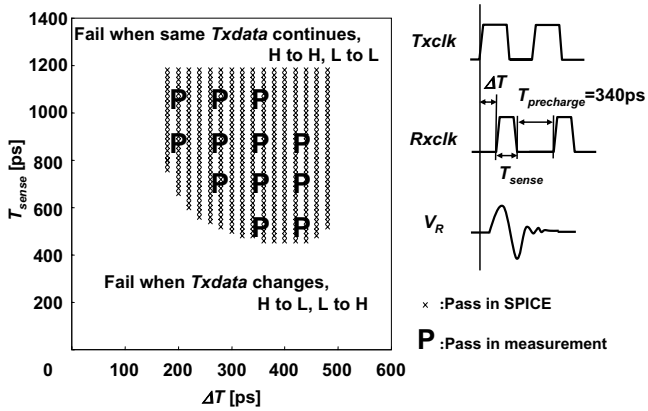


Figure 7.6.6: Receiver timing margin (measured data and SPICE simulation).

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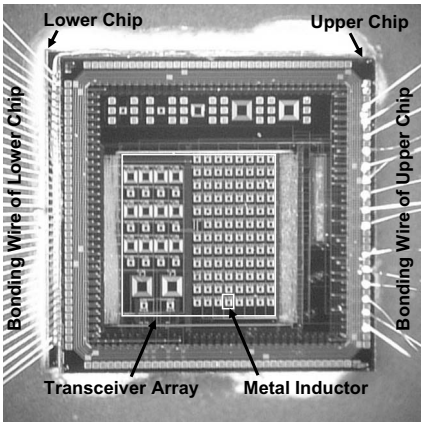

0.35μm CMOS Tech.
Triple Metals
3.3V Power Supply

Chip Thickness 300μm

Area:
Transmitter 90μmX40μm
Receiver 20μmX40μm
Inductor 100μmX100μm

Figure 7.6.7: Microphotograph of stacked test chips.

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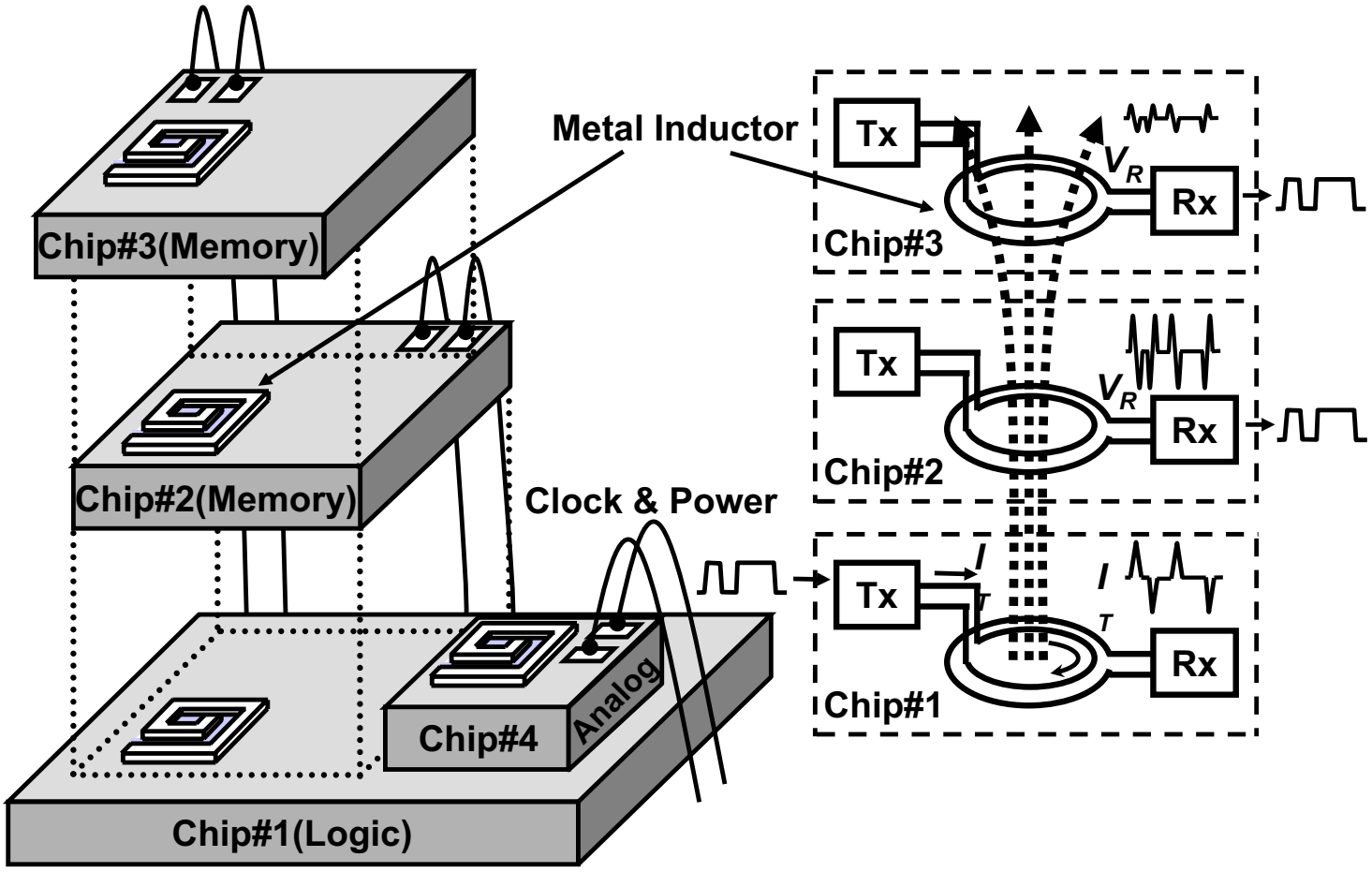

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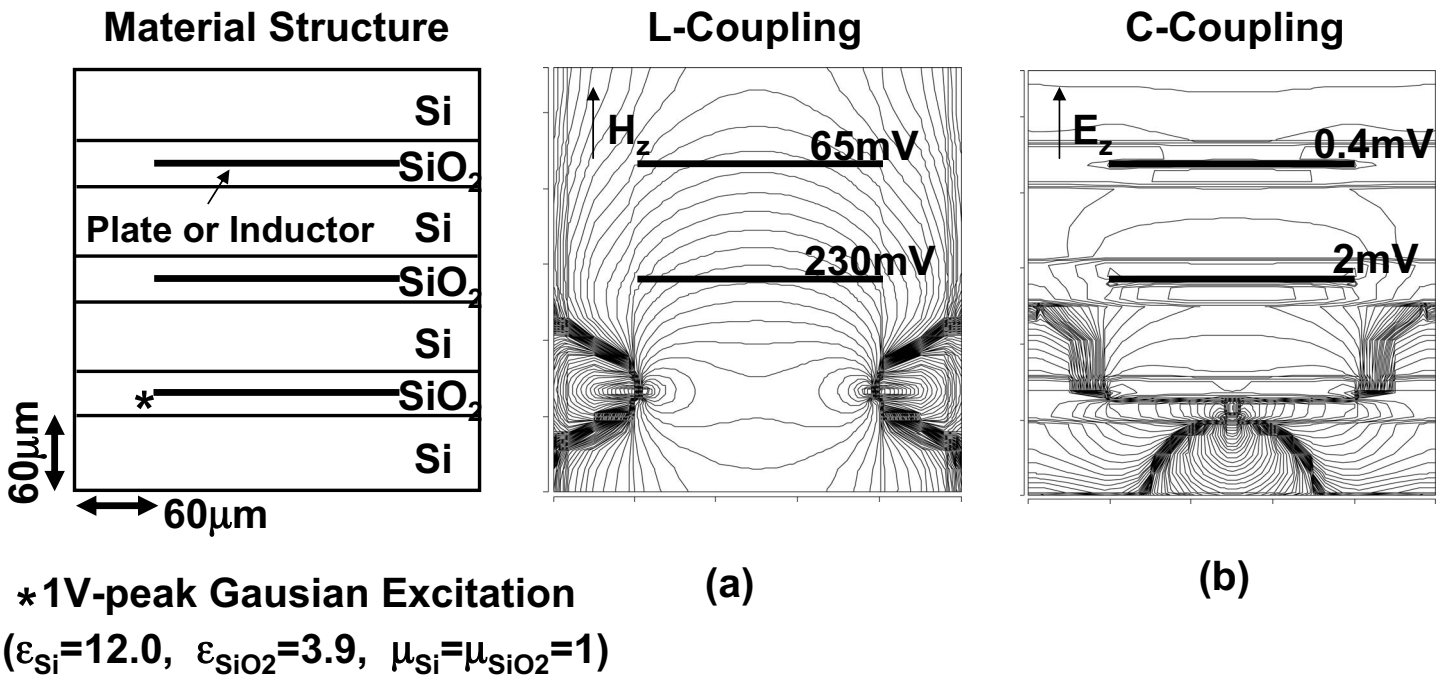

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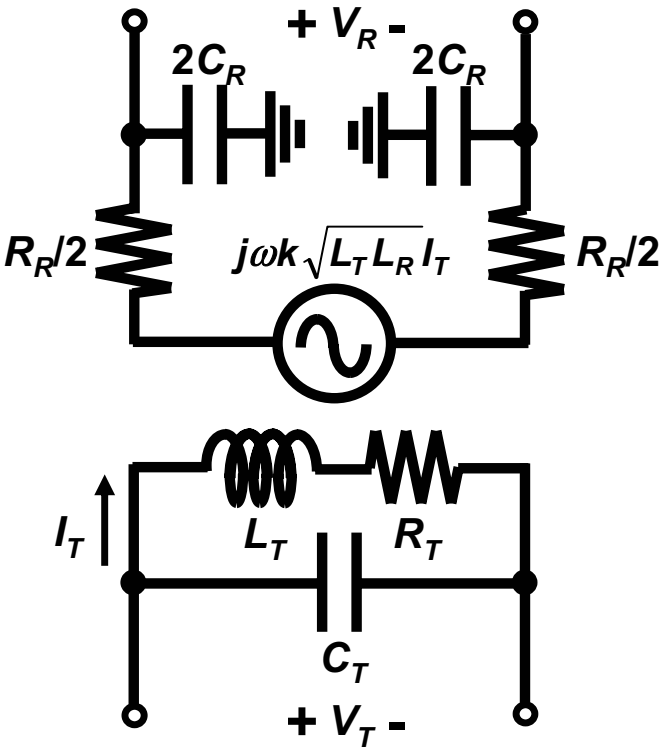
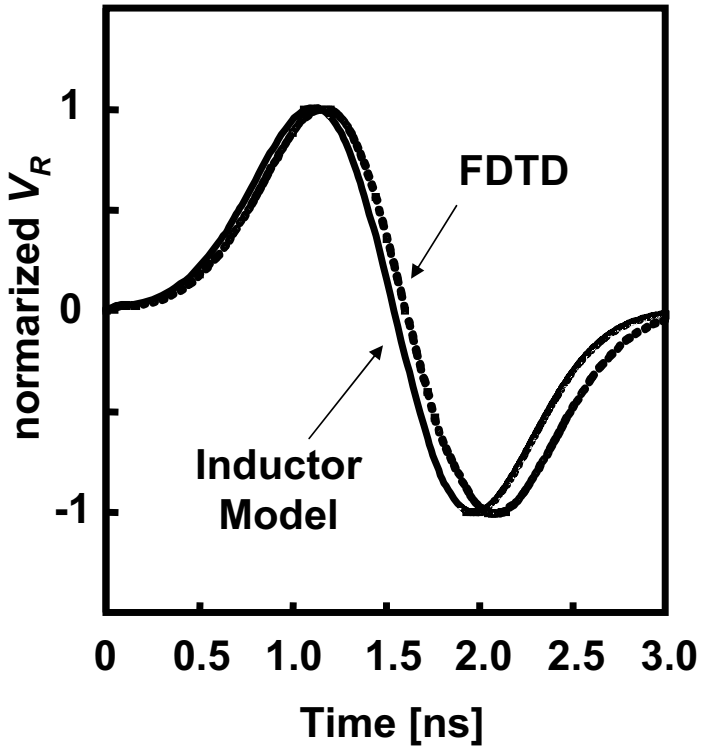


(a)



(b)

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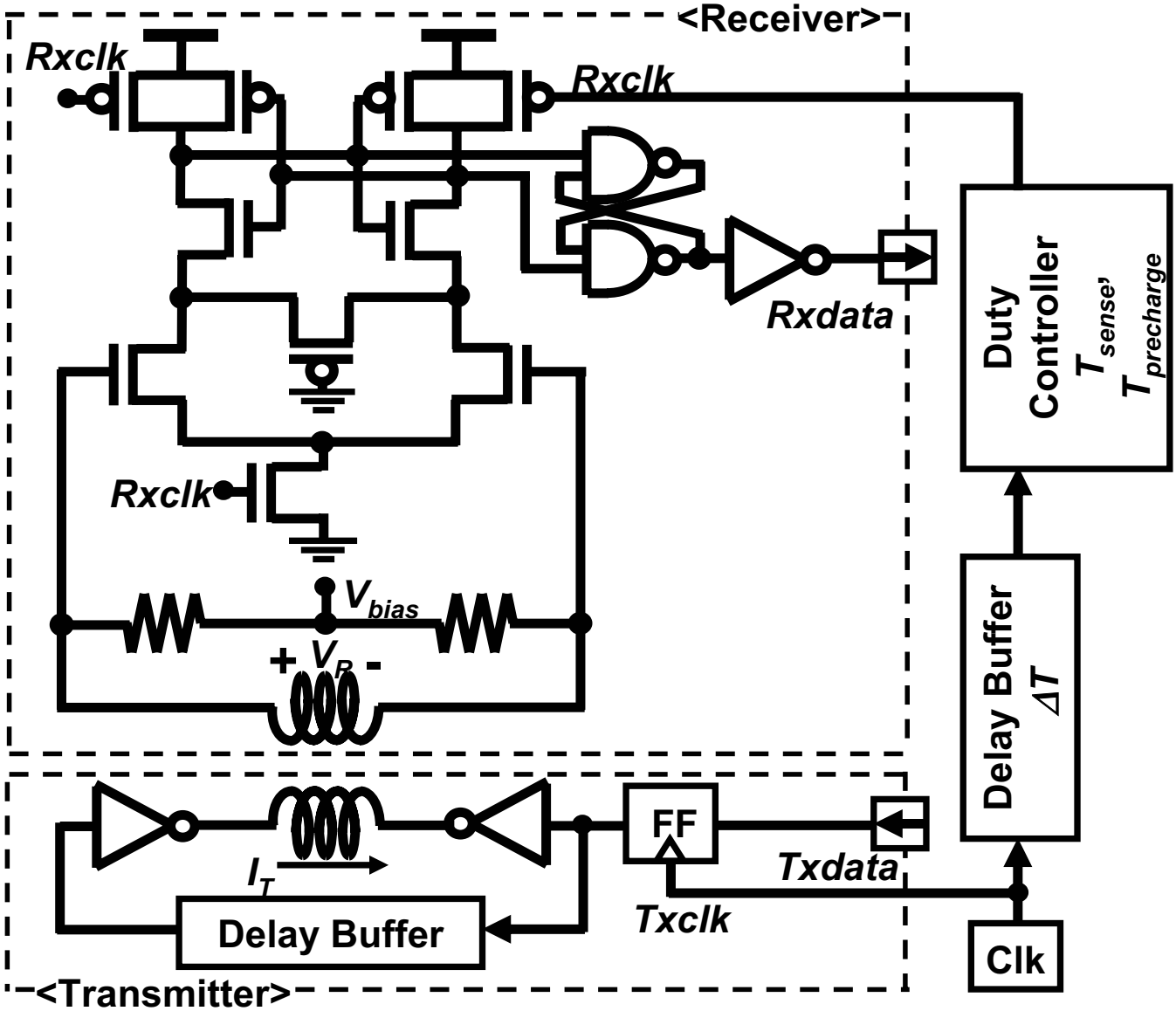

Figure 7.6.4: Transceiver circuit diagram.

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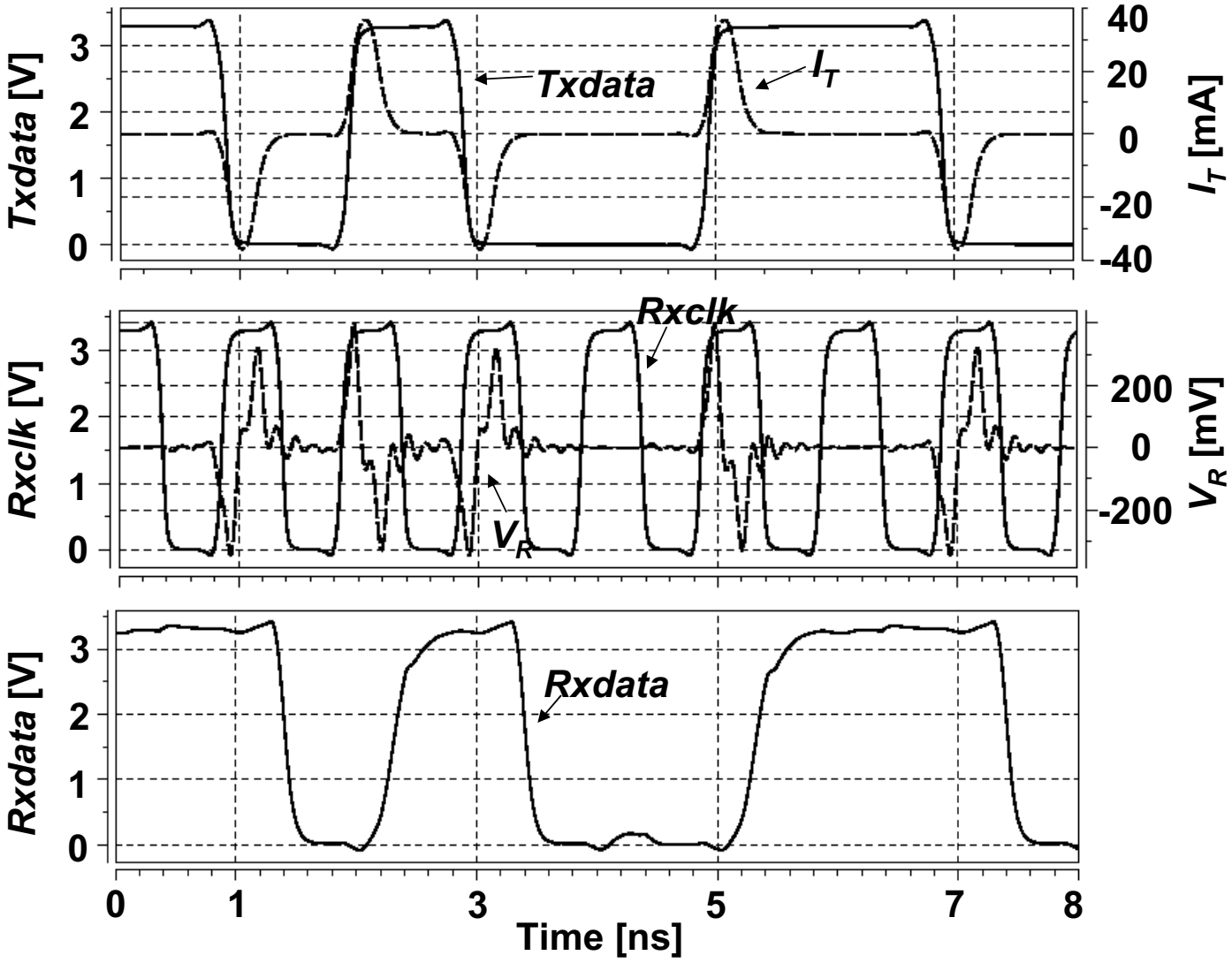

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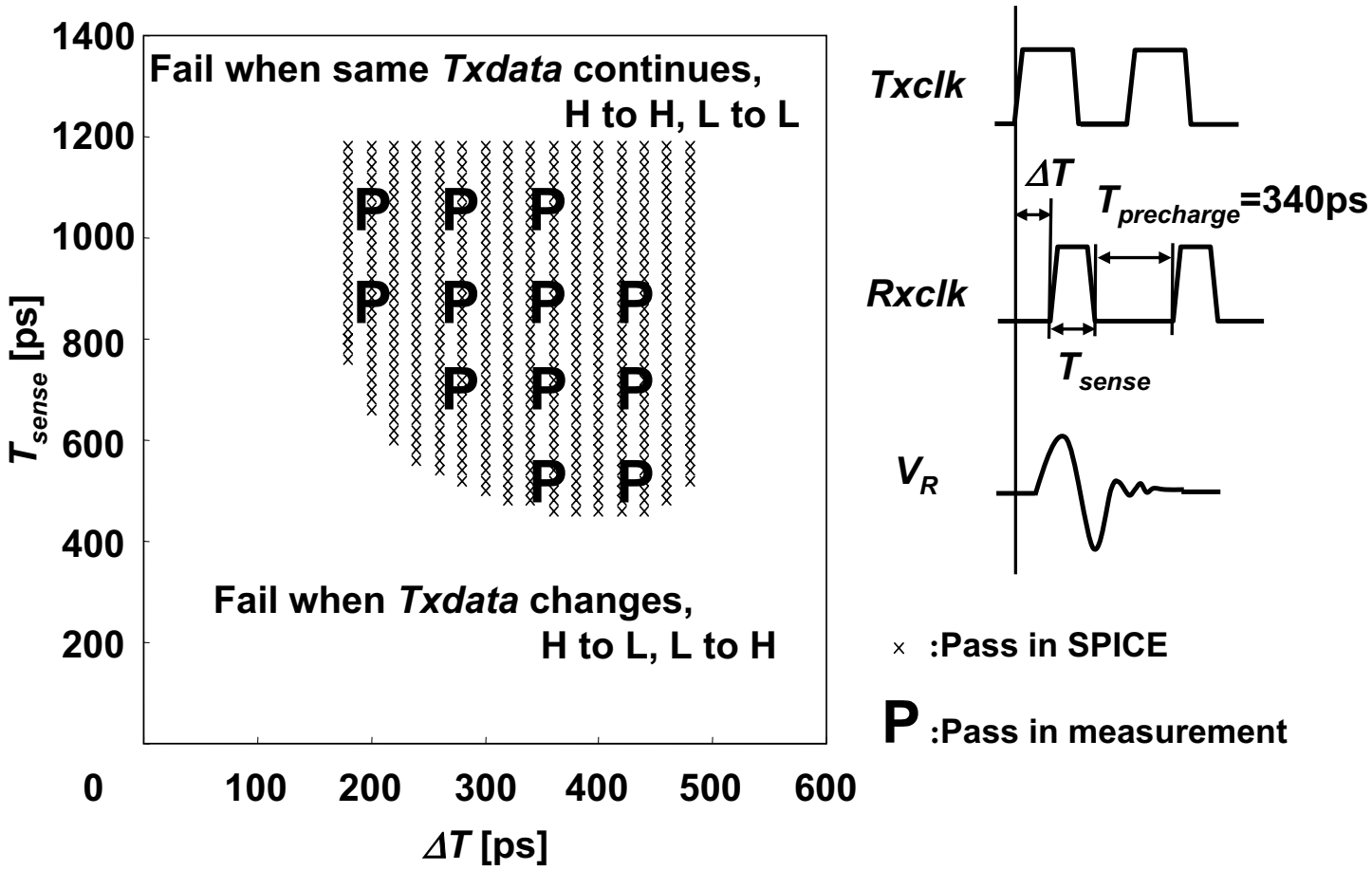

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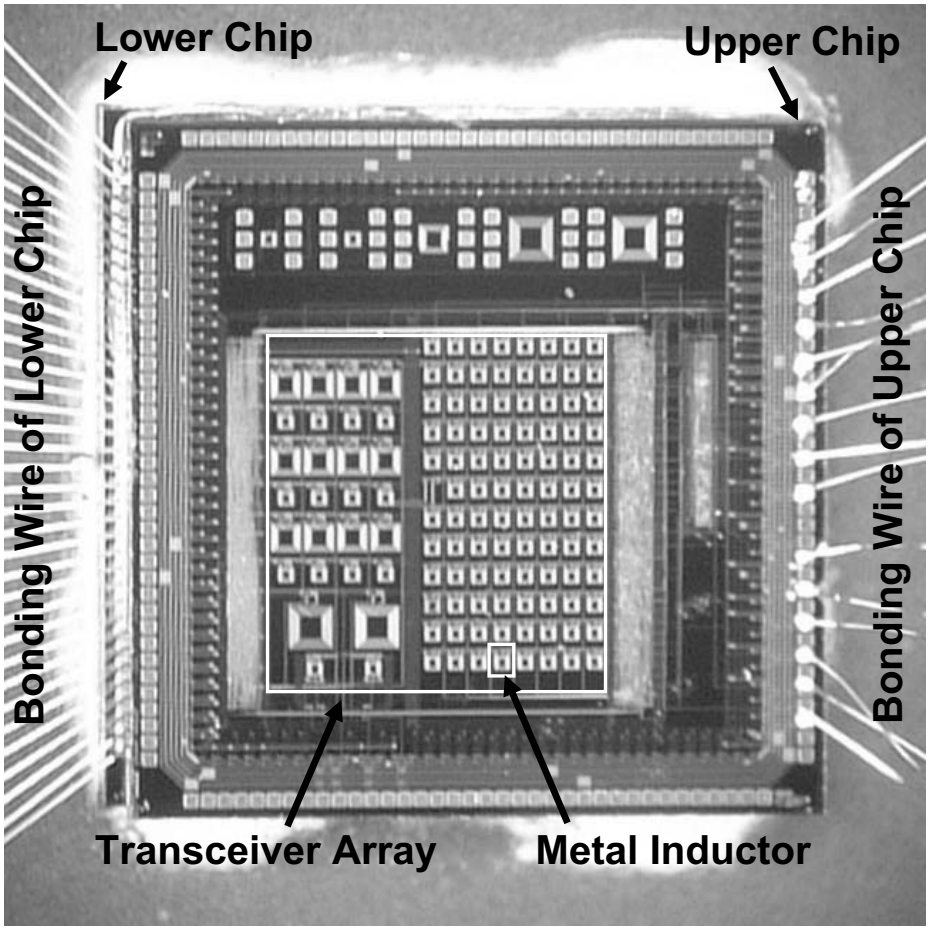

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