A CMOS UWB Transmitter for Intra/Inter-chip Wireless Communication

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***Abstract*-This paper presents a single chip Ultra Wideband (UWB) transmitter which transmits very short duration Gaussian monocycle pulses having wide bandwidth as a signal without a sinusoidal carrier. A new technique based on CMOS technology to generate the monocycle pulse with a target monocycle pulse center frequency of 5 GHz is also presented. The proposed single chip UWB transmitter has been simulated by HSPICE for 0.18 μm CMOS process and results are presented in this paper. Simulation reveals that the proposed transmitter has a wide bandwidth characteristics and can be effectively used for inter/intra chip wireless interconnection.**

I. INTRODUCTION

Steady downscaling of semiconductor device dimensions has been the main stimulus to achieve higher speed and performance of integrated circuits over the past decades. Unfortunately scaling has a reverse effects on the delay associated with the parasitic resistance, capacitance and inductance of conventional wiring. Now the industry is producing logic integrated circuits crammed with over 100 million transistors whose critical dimension is about 0.1 μm. At this level of integration, the main obstacle for achieving higher speed is not the device switching delay, but the delay associated with the interconnects. Again the demand for System On a Chip (SOC) has increased interest in three dimension integrated circuits. The parasitic resistance, capacitance and inductance of conventional wiring will become the primary obstacle for high speed data transmission and for the distribution of high frequency clock signal among different sub-circuits in such a 3-D IC. Recently Intra/Interchip wireless interconnect systems using integrated antenna is proposed to realize high speed data and clock distribution without any parasitics delay [1-3]. Such a interconnect system as shown in Fig. 1 requires transmitter, receiver and antenna. For high data transmission rate and multiple access capability of this wireless interconnection system, it requires wideband characteristics of integrated transmitter, receiver and antenna. According to the channel capacity theorem, data transmission rate or channel capacity grows linearly with channel bandwidth and logarithmically with signal to noise ratio [4]. Thus a UWB system appears to have a great potential for implementation of wireless interconnect system for future ULSI.

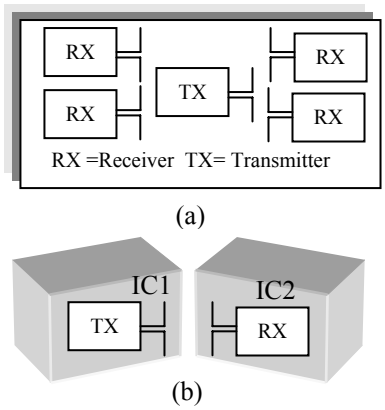

Fig. 1 Wireless interconnect system for future ULSI
(a) Intrachip and (b) Interchip.

In this paper implementation UWB transmitter in a single chip for future intra/interchip wireless interconnection is presented. The well known time hopping spread spectrum technique with pulse position modulation is employed in UWB transmitter. The time hopped or time shifted pulse is then used to generate monocycle pulse for high speed data and clock transmission.

The paper is organized as follows. Section II describes the functional aspects of UWB transmitter. A CMOS UWB transmitter circuit and its HSPICE simulation results are presented in section III. Section IV contains the concluding remarks.

II. UWB TRANSMITTER CONCEPT

The UWB transmitter should transmit very short duration Gaussian monocycle pulses as a signal without a sinusoidal carrier. The functional block diagram of the transmitter to generate the UWB signal is shown in Fig. 2. A time shifted pulse train is generated from the frame clock in accordance with the pseudorandom sequence data which provides multiple access capability. Pulse position modulation (PPM) is used to encode data onto the pulse train. The PPM could transmit a pulse a fraction of the pulse width late (relative to nominal position) to represent a "1" bit and without any late (i.e. at nominal position) to represent "0" bit

At the receiver side the cross correlation technique (a matched filter that consists of mixer followed by an integrator) is to be used to convert each time shifting RF pulse into a baseband signal [5].

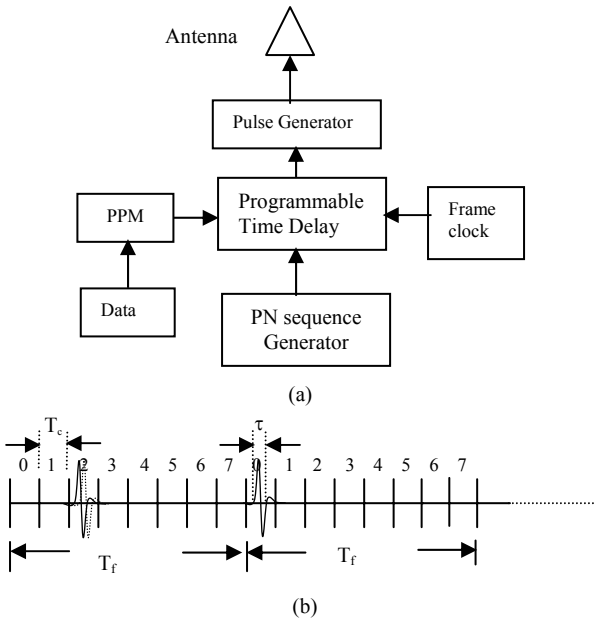

Fig.2 (a) Functional block of UWB transmitter and (b) UWB pulse train.

.A typical time shifting with pulse position modulation UWB signal generated by the k^{th} transmitter (i.e. k^{th} user or k^{th} chip) is given as [6]

$$s^k(t) = \sum w_{tr}(t - jT_f - c_j^{(k)}T_c - \Delta d_{[j/N_s]}^{(k)}) \quad [1]$$

Here $w_{tr}(t)$ represents the transmitted Gaussian monocycle that nominally begins at a time of zero on the transmitter's clock. The jth monocycle generally begins at $jT_f+c_j^{(k)}T_c+\Delta d^{(k)}$. Here T_f is the pulse repetition time which is typically be a hundred to thousand times of the monocycle width [6]. In the present work the pulse width (τ) is considered to be as 0.33ns and pulse repetition time or frame clock is 20ns which is 60 times of the pulse width. These values are taken to avoid the complexity of the circuit design for initial investigation. A frame consists of a number of compartments which is occupied by one of the k^{th} users (i.e. k^{th} chip). In order to avoid the catastrophic collision in multiple accessing due to the possible occupancy of the same compartment at the same instance by the users and to spread the spectrum, each chip is assigned a distinct pulse shift pattern (c_j^k) known as time hopping code. These time hopping code is periodic with a period N_p. The time hopping code provides an additional time shift of $c_j^k T_c$ seconds to each jth pulse of the kth user. Here Tc, the controllable unit time also known as hopping period should satisfy $N_h T_c \le T_f$ to avoid any collision from next pulse. N_h denotes the maximum decimal value of the hopping code. In this work three bit hopping is considered which limits decimal value of N_h from 0 to 7 and thus the number of compartment or slot in a frame is 8. An additional time shifting $\Delta d^k_{j/Ns}$ is provided to encode the data sequence corresponding to the j^{th} pulse of the k^{th} user where $d^k_{j/Ns} \in \{0\ 1\}$. Here Δ represents the modulation factor (i.e. the time interval between bit "1 " and "0") whose optimum value is a fraction of the monocycle duration. N_s represents the number of pulse repetitions per data bit yielding the actual data transmission rate $R_s = 1/N_sT_f$ bit per second.

III. UWB TRANSMITTER CIRCUIT and SIMULATION

The UWB transmitter is implemented by using the current 0.18μm CMOS technology. The circuit schematic of UWB transmitter is shown in Fig. 3. The VCO produces a signal of 800 MHz which is divided by 16 (by using four divide by 2 circuit) to produce a frame clock of 50 MHz (i.e. T_f=20 ns).

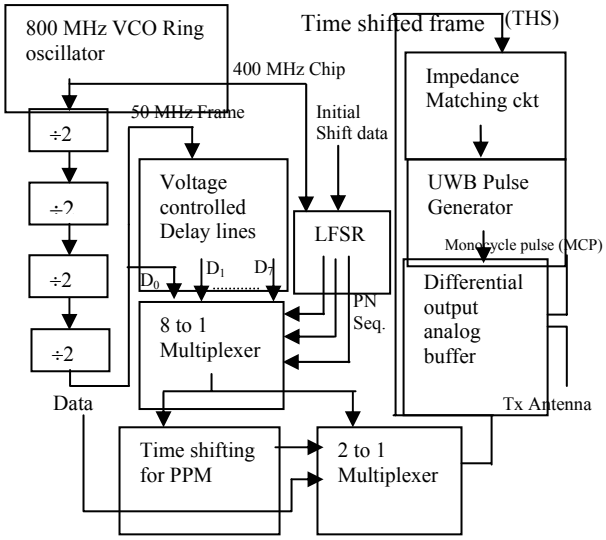

Fig. 3 Circuit Schematic of UWB transmitter.

The simulated VCO output before and after divider is shown in Fig. 4. The frequency stability of the frame clock is an important factor in UWB system. It is found from simulation that the frequency stability with change of V_{dd} and temperature is about 5% in the worst case. The phase noise of the VCO is calculated by the method explained in [7] and is found as –93.6 dbc/Hz for 100KHz offset. The seven time shifted frame is generated from the frame by the precise delay lines. The delay generation circuit is based on the voltage controlled delay line which consists a number of buffer stages connected in series. For the present investigation only eight channel is considered thus the frame is divided into eight slots. Each slot occupies a time of 2.5ns in frame. Thus the delay circuit is tapped at seven points so that a delay of 2.5ns interval with reference to frame clock can be achieved. The simulated output is shown in Fig. 5. Linear feedback shift register which consists of four clocked D-type Flip-Flop along with an exclusive-or logic as feedback is used to generate pseudorandom sequence. The initial shift in data is taken as [1 0 0 0]. This will repeat after the every 15^{th} cycle of the clock frequency of 400 MHz (i.e. T_c=2.5ns).

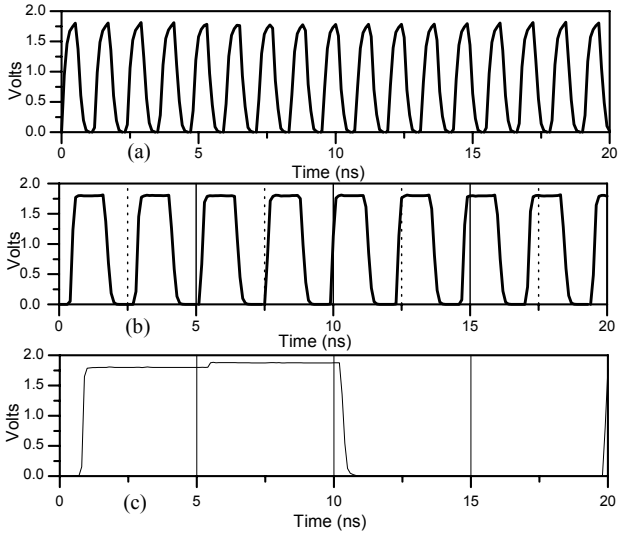

Fig. 4 (a). 800 MHz. VCO output; (b) 400 MHz clock obtained from first divider output and (c) 50 MHz Frame clock.

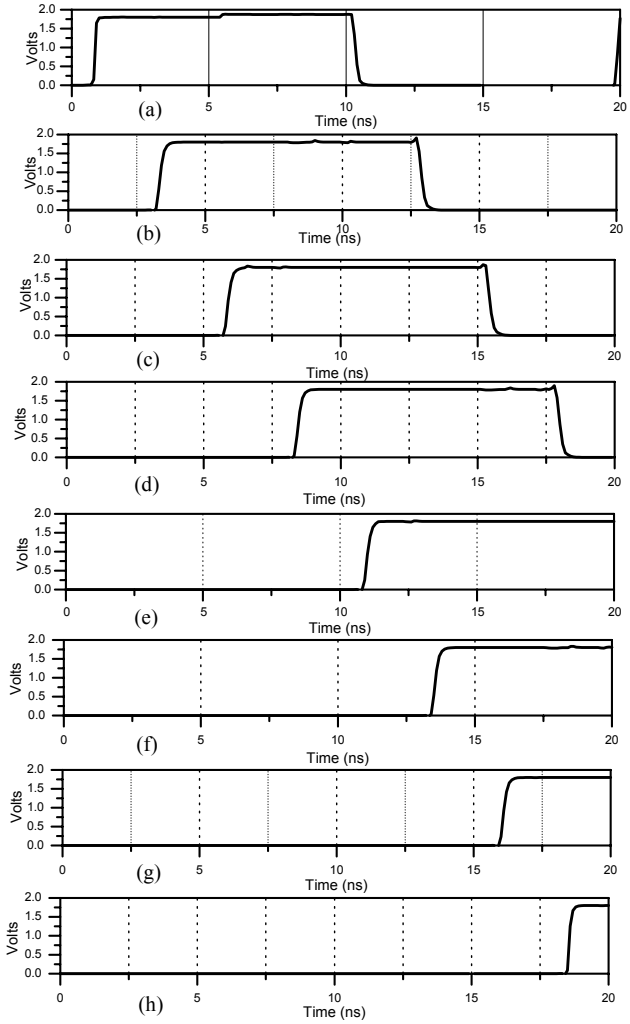

Fig. 5 Time shifted frame: (a) 20ns frame clock; (b) 2.5ns; (c) 5ns ; (d) 7.5ns ; (e) 10ns ; (f) 12.5ns; (g) 15ns and (h) 17.5ns shifted frame.

The simulated result is shown in Fig. 6. It is observed that the generated PN sequence satisfies all its randomness properties such as balance , run and co-relation property.

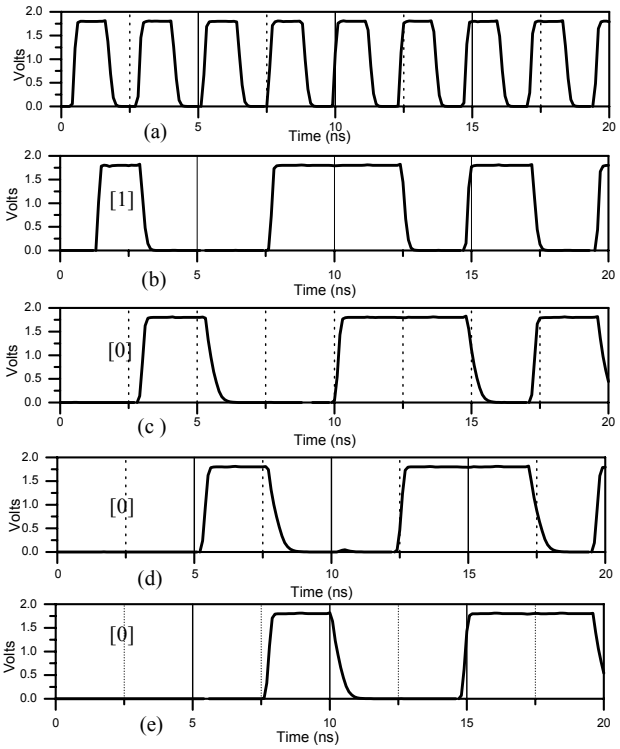

Fig. 6 PN sequence from LFSR with a initial input of [1 0 0 0]: (a) 400 MHz chip clock; (b), (c), (d) and (e) shift register outputs.

An eight to 1 multiplexer circuit is designed using conventional CMOS NAND and NOR gate. The multiplexer selects the time shifted frame clock according to PN sequence with three hopping bit. This is due to the fact that c_j of "(1)," of section II is taken as 0 to 7 because of considering the eight channel in this work. The time shifting due to PPM is done by the fine delay line which provides a delay of approximately the modulation time (Δ=0.05ns). This modulation time is taken because of the minimum delay of the fine delay line. The time shifted pulse is then selected according to data symbol 0 or 1 by using the two to 1 multiplexer and finally the time shifted pulse train due to PN sequence and PPM to encode data is obtained from the output of two to 1 multiplexer. Both eight to 1 and two to 1 multiplexers outputs are shown in Fig. 7. For the present investigation , return to zero (RZ) data signal with a width of 1.25ns is considered. Here data symbol width and PN sequence symbol width is considered to be equal. The Fig. 7(f) shows that the data is placed in the desired compartment at desired position of the frame according to PN sequence and data symbol. The monocycle pulse is then generated from the output of two to 1 multiplexer (time shifted pulse train). The monocycle pulse generator circuit as shown in Fig. 8, produces damped sinusoidal like waveform from the time shifted pulse train.

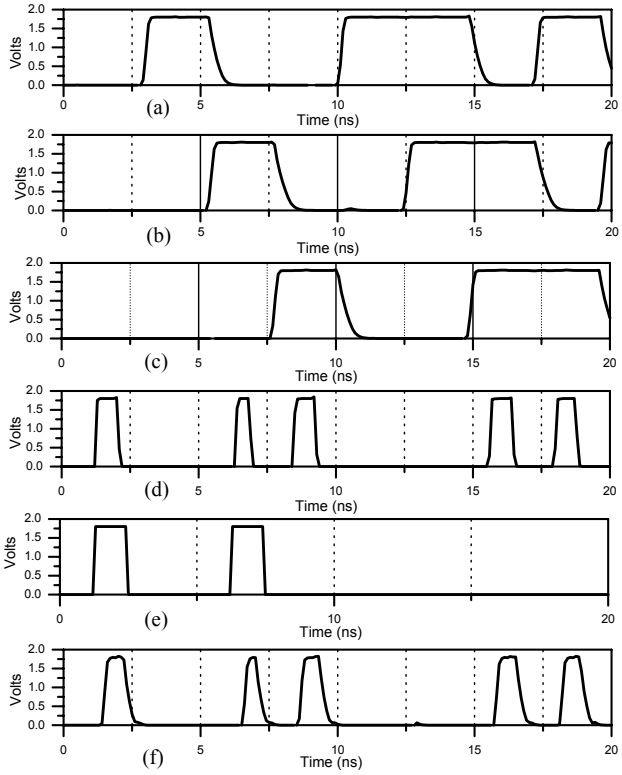

Fig. 7 Time shifted pulse train due to PN sequence and PPM containing data: (a), (b), and (c): hopping bit sequence; (d) 8 to 1 multiplexer output ; (e) RZ data [1 1 0 0 0] and (f) two to 1 multiplexer output.

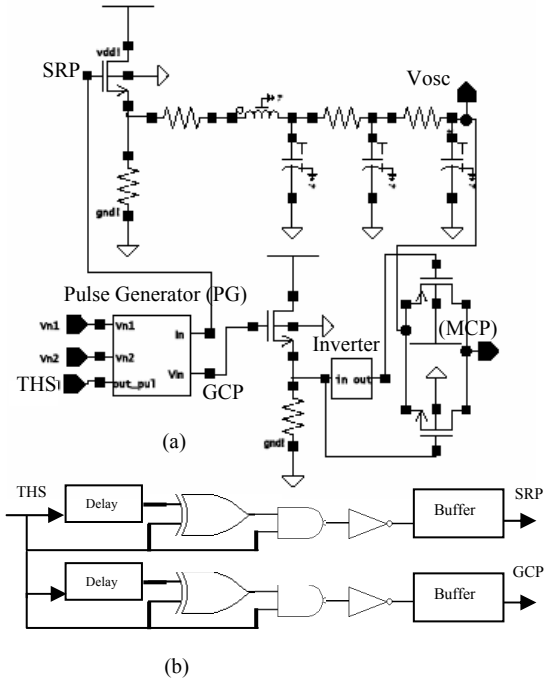

Fig. 8 (a) Monocycle pulse generator and (b) Pulse generator.

A short pulse (SRP) is applied as input of the monocycle pulse generation circuit to produce oscillation. The SRP is generated from the time shifted pulse train through a pulse generator circuit which consists of voltage controlled delay, exclusive-or, NAND and buffer circuit. The frequency of oscillation (*f*) of the damped sinusoid signal can be controlled by varying inductance and capacitance values of RLC network. This signal is then passed through transmission gate which is controlled by the pulse of desired width (1/f) to pass the first cycle of the generated signal at the output. The transmission gate control pulse (GCP) is also generated from the same time shifted pulse using pulse generator circuit shown in Fig 8. The simulated output of the monocycle pulse generation circuit is shown in Fig. 9. The FFT of the generated monocycle pulse is shown in Fig. 10.

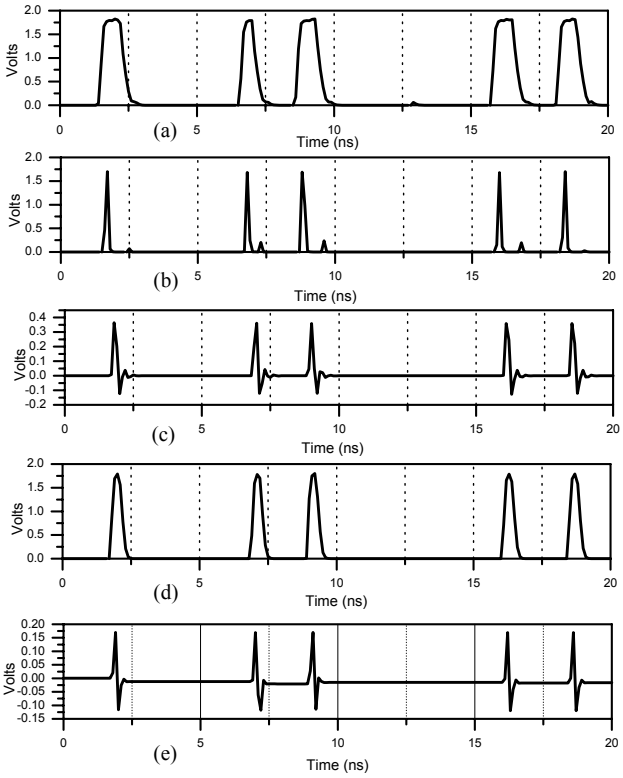

Fig. 9 Monocycle pulse train containing information: (a) time shifted pulse contain data;(THS) (b) short pulse (SRP) for RLC circuit; (c) damped sinusoidal signal (Vosc); (d) gate control pulse (GCP) and (e) Monocycle pulse (MCP) train.

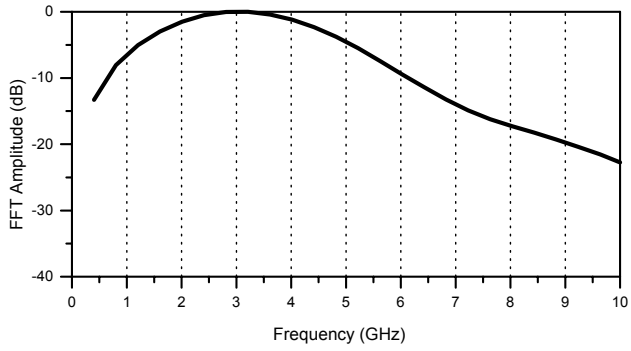

Fig. 10 FFT of monocycle pulse (zoom view is shown).

The FFT shows that the generated monocycle has wide half power bandwidth (BW) of approximately 116% the monocycle pulse center frequency (3GHz). The developed UWB transmitter performance data is given in Table I.

Table I
Transmitter performance data

UWB system	Time hopping Impulse
Carrier Frequency	No carrier
Transmitter Signal bandwidth	3.3 GHz
Data rate	50 Mbps
Single Channel bandwidth	400 MHz
Modulation	Pulse position modulation
Average power consumption	12.5 mW
Architecture	All digital except pulse generator
Technology	TSMC 1.8v, 0.18 µm CMOS mixed signal process
Implementation	Single chip
Circuit Size	0.729 mm^2 (excluding antenna)
Application	Short distance (on chip wireless interconnection for future ULSI)

The proposed UWB transmitter circuit is implemented using TSMC 0.18 µm CMOS mixed signal process. The chip layout is shown in Fig. 11. The chip size is 1078µmX677µm and the operating voltage is 1.8v.

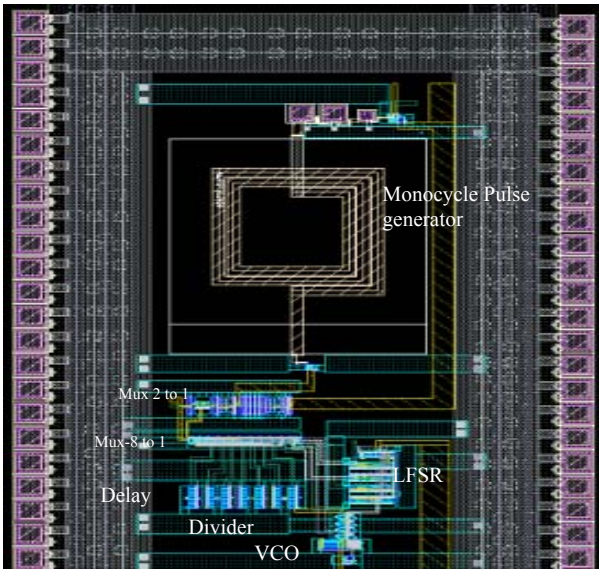

Fig. 11 UWB Transmitter chip layout.

IV. CONCLUSION

All circuit blocks of the UWB transmitter presented in this paper are almost digital architecture except monocycle generation circuit. However monocycle can be generated using the current CMOS technology which has led us to implement the UWB transmitter in a single chip. In the present investigation monocycle center frequency is 3 GHz. This is due to the use of available lowest value of spiral inductor (2.35nH) from the existing TSMC library. The monocycle pulse center frequency can be increased by using low value of inductance and short GCP. Since the monocycle is generated from the time shifted pulse, so it is only necessary to keep constant gate delay with any variation of V_{dd} and substrate voltage.

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