A High-Voltage Temperature Compensated Logarithmic Amplifier Suitable for Integration in a BiCMOS Power Controller IC

William C. Dillard, Jr.
200 Broun Hall
ECE Department
Auburn University, AL, 36849
dillard@eng.auburn.edu

Abstract— **A new logarithmic amplifier suitable for integration in controller IC's for power electronics systems is introduced. The amplifier can be implemented in standard BiCMOS technologies commonly used to manufacture controller IC's but consumes little silicon real estate as compared to commercial log amplifiers, leaving room for primary controller features. Particularly suitable to high voltage measurements at low power, the amplifier includes internal temperature compensation.**

The amplifier is in fabrication using the TSMC 0.35 μm technology node. Simulations results at a single supply of 3.3 V predict true logarithmic performance with only 1.5 mW of quiescent power consumption. The active area of the amplifier (sans I/O pads) is 100 μm x 125 μm.

Keywords-logarithmic amplifier, power controller, power controller, temperature compensation.

I. INTRODUCTION

Simple voltage dividers are commonly used to scale large voltages to signal-level equivalents suitable for signal processing by controller IC's. For applications where a large dynamic range must be monitored, the logarithmic amplifier based on the exponential V-I relationship of the p-n junction, offers signal compression over several decades of voltage [1 – 2]. One solution, shown in Figure 1a, requires two IC's: a commercial logarithmic amplifier and the controller. External resistors and, depending on which commercial log amp is chosen, frequency compensation capacitors may be required to complete the design.

Commercial logarithmic amplifiers IC's rely on several internal amplifiers which, along with the necessary frequency compensation capacitors, consumes large amounts of silicon area [3- 4]. The amplifier output drive must be sufficient for a variety of possible load devices as chosen by the user. Also, for precision, thin resistors are fabricated on the chip and laser trimmed *in situ*, increasing costs. A better solution to design the logarithmic amplifier as portable intellectual property (IP) that is compatible with standard controller IC technology, then integrate the logarithmic amplifier directly into the controller IC, as depicted in Figure 1b.

The advantages of integration are obvious.

- Reduced IC and component count
- Known load (BiCMOS input)
- Better matching between the log amp and the controller devices

To reap these benefits while retaining all controller features, the area consumed by the integrated log amp (ILA) must be significantly reduced as compared to a traditional opamp-based design. A partial list of the ILA's requisite features include:

- Low input bias current
- Low device count
- No frequency compensation capacitance
- Internal temperature compensation
- Transconductance output stage
- Low power consumption

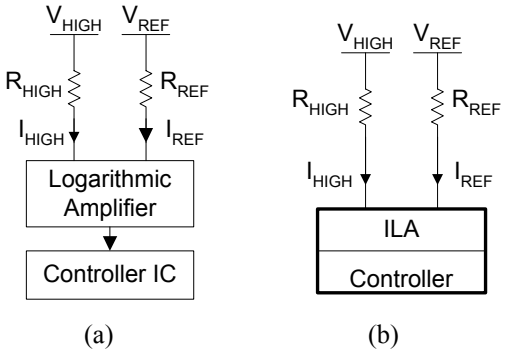


Figure 1. Two approaches to interfacing logarithmic amplifiers to standard controller IC's: (a) the traditional approach using a commercial log amp and (b) an integrated log amp (ILA) implemented directly onto the controller IC.

Fabricated through the RESEARCH branch of the MOSIS Educational Program (MEP).

II. LOGARITMIC AMPLIFIERS - THEORY OF OPERATION

A. First Generation Opamp Topologies

A simplified schematic for a commercial logarithmic amplifier is shown in Figure 2 [3]. The voltage to be monitored, V_{HIGH}, is converted to a current I_{HIGH} and fed into npn transistor Q_1 causing a base-emitter voltage given by

$$V_{BE1} = nV_T \ln\left[\frac{V_{HIGH}}{R_{HIGH} I_S}\right],$$

or, (1)

$$V_{BE1} = \left[nV_T \log(e)\right]\log\left[\frac{V_{HIGH}}{R_{HIGH} I_S}\right].$$

where n is the emission coefficient, V_T is the thermal voltage and I_S is the saturation current of the npn device. Equation (1) assumes that the input bias current of the opamp. I_{BIAS}, is negligible compared to I_{HIGH}. The true collector current is

$$\begin{aligned} I_D &= I_{HIGH} \pm I_{BIAS} \\ &= \left[\frac{V_{HIGH}}{R_{HIGH}}\right]\left[1 \pm \frac{I_{BIAS} R_{HIGH}}{V_{HIGH}}\right]. \end{aligned} \quad (2)$$

If R_{HIGH} is chosen large to minimize power consumption, error can occur when V_{HIGH} is small. Therefore input bias currents should be kept as low as possible.

While the activity described in (1) performs the log operation, there are two temperature dependences, the thermal voltage and the saturation current, which must be compensated.

$$V_T = kT/q \approx 25\text{mV at } 300\text{K}$$

and (3)

$$I_S = BAT^3 \exp\left[\frac{-E_G}{kT}\right]$$

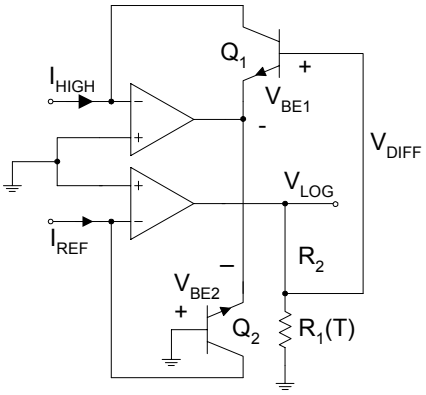


Figure 2. A simple logarithmic amplifier based on two opamps and the exponenential I-V relationship of the bipolar transistor operating in the forward active region.

where B is a temperature independent material constant, A is the emitter area of the npn transistor and E_G is the bandgap of silicon. Although the strong temperature dependence in I_S is weaken by the log operation in (1), it still must be eliminated. A similar circuit produces a second base-emitter voltage

$$V_{BE2} = \left[nV_T \log(e)\right]\log\left[\frac{V_{REF}}{R_{REF} I_S}\right]. \quad (4)$$

Subtracting these voltages eliminates the saturation currents, leaving only the temperature dependence of V_T. This signal appears at node V_{DIFF}.

$$\begin{aligned} V_{DIFF} &= V_{BE1} - V_{BE2} \\ &= \left[nV_T \log(e)\right]\log\left[\frac{V_{HIGH} R_{REF}}{V_{REF} R_{HIGH}}\right] \end{aligned} \quad (5)$$

The resistors and V_{REF} can be chosen to reference V_{HIGH} to V_{REF}. The output voltage is then

$$V_{LOG} = \left[\frac{R_1 + R_2}{R_1}\right]\left[nV_T \log(e)\right]\log\left[\frac{V_{HIGH}}{V_{REF}}\right]. \quad (6)$$

Making R_1 proportional to absolute temperature (PTAT) provides a degree of temperature compensation. This becomes completely effective only as R_2/R_1 approaches infinity. Output drive is provided by the output stage of the second opamp. External frequency compensation capacitors may also be required [5 – 6].

B. The Progressive Compression Topology

An alternative logarithmic amplifier topology for high frequency applications is the progressive compression scheme depicted in Figure 3 [4]. Cascaded amplifier stages with limited gain are successively driven into saturation as the input voltage increases, emulating the signal compression of the log function. As a result, no diodes are required. The overall accuracy of the amplifier is strongly dependent on the number of cascaded stages and each stage must be uniquely designed to enter saturation at the appropriate input voltage level. The principle weaknesses of the compression scheme are the large number of transistors (more than 100 typically) and the need for frequency compensation – particularly at low signal levels where all amplifier stages are operating at maximum gain.

A variation on the progressive compression topology that is applicable to signal strength detection and IF amplification in communication equipment is the rectifying scheme shown in Figure 4 [5,6]. Limiting amplifiers are employed as described in Figure 3. The input to each stage is rectified and the resulting signals are summed to produce the logarithmic output.

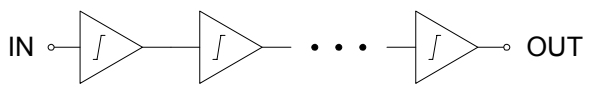


Figure 3. A cascade of limiting amplifier can mimic the logarithm transfer function. Stages saturate sequentially as the input increases compressing the gain. Each stage is tuned independently for the requisite small-signal gain and large signal saturation point.

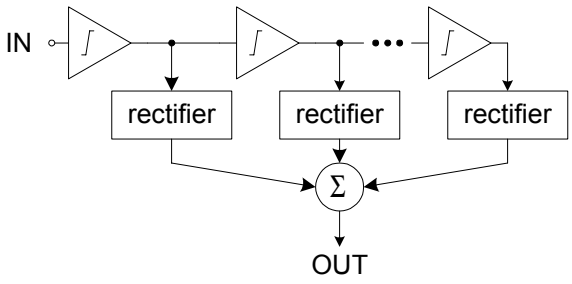


Figure 4. High frequency communications blocks such as signal strength detectors and IF amplifiers can be created by adding rectifiers to the progressive compression scheme in Figure 3.

III. The ILA Circuit – Theory of Operation

A conceptual diagram of the proposed integrated logarithmic amplifier is shown in Figure 5. It is comprised of two main blocks – a difference block, which outputs a logarithmic current, and a temperature compensator block that acts as a load resistance to convert the log current to voltage.

A. Difference Block

In the difference block, shown in detail in Figure 6, voltages V_{HIGH} and V_{REF} are input effectively as currents through resistors R_{HIGH} and R_{REF}. Diodes D_1 and D_2 convert these currents to voltages V_{D1} and V_{D2}, performing the logarithm operation described in (1). Rather than subtracting the diode voltages with opamps as shown in Figure 2, transistors M_1 – M_4 first convert the diode voltages ***linearly*** back to currents. The unique arrangement of transistors M_2 and M_1 forces M_1 to operate in the linear region. As a result, I_{D1} is linearly related to V_{D1} without the use of opamps. (A similar argument can be made for M_3-M_4 and their effect on I_{D2} and V_{D2}.)

Simulations results in Figure 7 verify this linear relationship for temperatures between 25°C and 100°C. Note that the temperature dependence of the drain current is significant with I_{DS} decreasing as temperature increases due to the channel mobility degradation at higher temperatures.

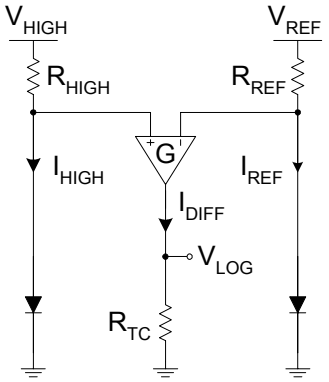


Figure 5. A conceptual diagram of the ILA shows the transconductance difference block and the temperature compensator, R_{TC}.

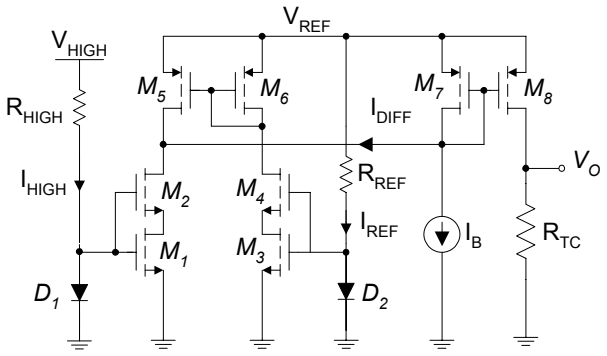


Figure 6. The difference block effectively subtracts diode voltages as described in eq (2). Rather than relying on feedback to linearize opamps, transistors M_1 and M_3 operated exclusively in their linear regions be design.

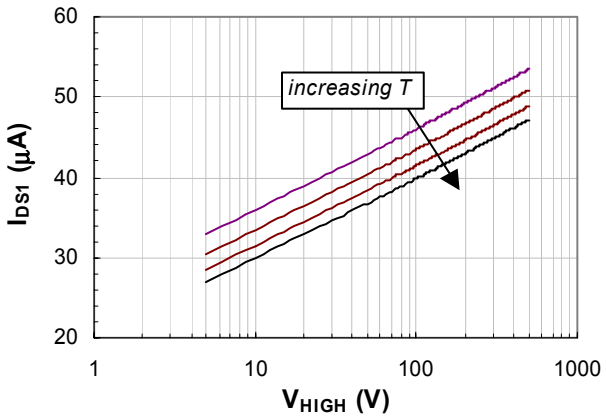


Figure 7. The ability of M_2 to force M_1 into its linear region is seen here. Note that I_{DS1} is logarithmically related to V_{HIGH} across the range 5 to 500 V. Stepping the temperature from 25°C to 100°C in 25°C increments shows the significance of the temperature dependence.

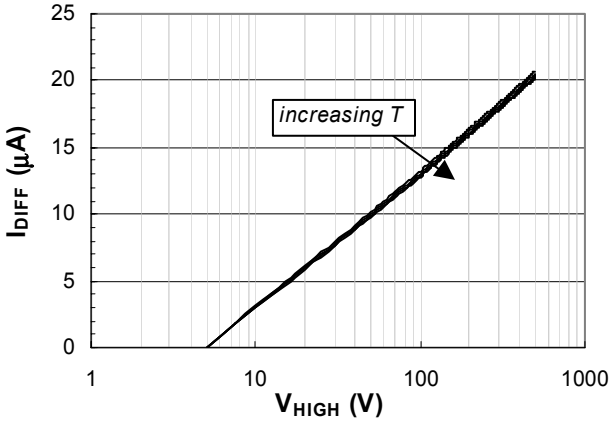


Figure 8. The M_5-M_6 current mirror subtracts the drain currents in M_1 and M_2 to produce I_{DIFF}, cancelling most of the terms in eq. (7). For the same 25°C to 100°C temperature stepping used in Figure 4, the subtracting has dramatically lowered the temperature sensitivty.

$$I_{D1} = K_{N1}[V_{GS1} - V_{TH1} - (V_{DS1}/2)]V_{DS1}$$
$$\approx K_{N1}\left\{V_T \log(e)\log\left[\frac{V_{HIGH}}{R_{HIGH} I_S}\right] - V_{TH1} - \frac{V_{DS1}}{2}\right\}V_{DS1} \quad (7)$$

Transistors M_5 and M_6 form a current mirror that subtracts I_{HIGH} from I_{REF} to yield I_{DIFF}. This subtraction cancels most of the terms in (7), producing the proper logarithmic relationship while reducing the temperature dependence. When I_{DIFF} approaches zero, the accuracy of the difference block is degraded. This is mitigated by the current source I_B, which biases the current mirror M_7-M_8 at 20 µA. The simulation results in Figure 8 validate the log relationship between I_{DIFF} and V_{HIGH} with much lower temperature sensitivity.

Since the difference in diode voltages has been converted to currents, the ILA is classified as a current-mode amplifier and traditional analog current mode techniques are available. For example, gain can be added by adjusting the W/L ratio of M_8 with respect to that of M_7.

B. Temperature Compensation Block

There are two major temperature dependencies in (7) –the transconductance parameter K_N and the thermal voltage, V_T. (Actually it is the carrier mobility implicit in K_N that has a T^n dependence where n ≈ 1.5.) To produce a temperature compensated output voltage proportional to log(V_{HIGH}), a resistance must be produced that is inversely proportional to both K_N and temperature. Such a resistance is shown in Figure 9 where transistor M_9 operates in its linear region.

The floating proportional-to-absolute-temperature (PTAT) voltage source produces a voltage

$$V_{PTAT} = V_1 + \beta T \quad (8)$$

where V_1 is designed to offset V_{TH}. The parameter β compensates the slight temperature dependence in Figure 8. Resistors R_3 and R_4 form a voltage divider such that the gate voltage and drain current for M_9 are

$$V_G = V_{PTAT} + \frac{V_{LOG}}{2} \approx V_{TH} + \beta T + \frac{V_{LOG}}{2} \quad (9)$$

and

$$I_D = K_{N9}\left\{V_G - V_{TH} - \frac{V_{LOG}}{2}\right\}V_{LOG} \approx K_{N9}(\beta T)V_{LOG} \quad (10)$$

The resulting equivalent resistance is

$$R_{TC} = \frac{\partial V_{LOG}}{\partial I_D}\frac{1}{K_{N9}\beta T} \quad (11)$$

Figure 10a shows the schematic for the PTAT generator. A PTAT current source formed by transistors M_{10} – M_{13}, diodes D_3 – D_4 and R_{PTAT}, produces the current

$$I_{PTAT} = \frac{V_T}{R_{PTAT}} \quad (12)$$

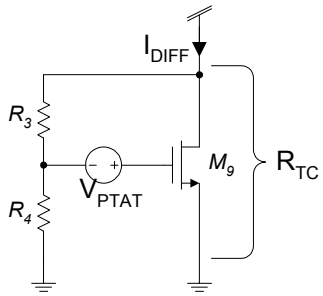
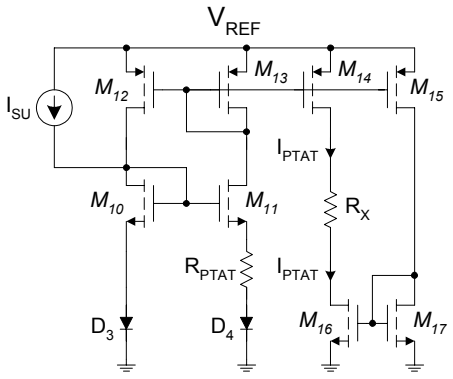
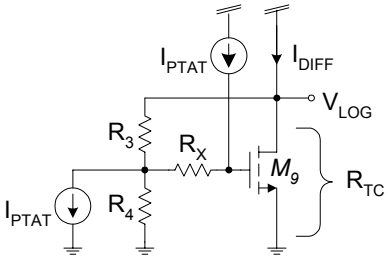


Figure 9. The temperature compensator block utilizes a voltage divider to improve the linear performance of M_9. A PTAT voltage source modulates the equivalent resistance, R_{TC}, and compensates for the temperature dependences in Figure 8.



(a)



(b)

Figure 10. The PTAT current source (a) produces V_{PTAT} as expressed in eq. (8) across resistor R_X as a floating voltage. Used in conjuction with the R_3-R_4 divider (b) the gate voltage in eq. (9) is generated.

(The current source, I_{SU}, is a startup current of 10 µA that is required to avoid the stable operating point of I_{PTAT} = 0.) Transistors M_{14}-M_{17} form a source-sink current mirror. I_{PTAT} is sourced into resistor R_X by M_{14} and sunk from it by M_{16} to create a floating PTAT voltage. Figure 10b shows how the PTAT circuitry is inserted into the R_3-R_4 divider. Figure 11 shows that the PTAT current source output is indeed proportional to temperature over the range 25°C to 100°C. Several parameters including I_{SU}, W/L, and R_X can be used to tailor V_{G9} as needed.

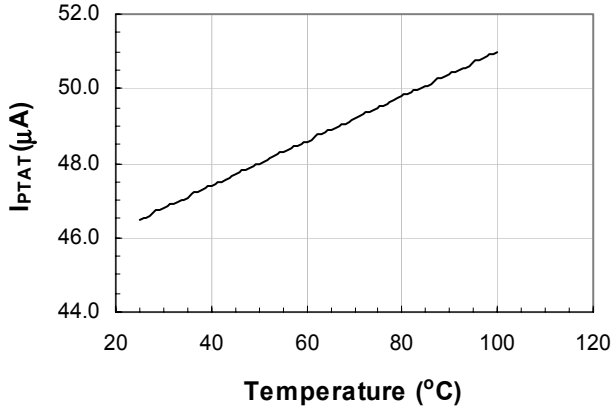


Figure 11. The output of the PTAT current source is very linear with temperature (0.060 μA/°C). Characteristics of I_{PTAT} such as intercept and slope can be controlled through the startup current source and the W/L ratios of the transistors.

Combining the two blocks, the final output voltage is generated.

$$V_{LOG} = I_{DIFF} R_{TC} = \frac{K_{N1} K_{N8} V_T \log(e)}{K_{N7} K_{N9} \beta T} \log\left[\frac{V_{HIGH} R_{REF}}{V_{REF} R_{HIGH}}\right] \quad (12)$$

If the external resistors are equal, the output voltage becomes

$$V_{LOG} = \frac{(W/L)_1}{(W/L)_9} \frac{(W/L)_8}{(W/L)_7} \frac{k \log(e)}{q\beta} \log\left[\frac{V_{HIGH}}{V_{REF}}\right] = A \log\left[\frac{V_{HIGH}}{V_{REF}}\right] \quad (13)$$

and V_{HIGH} is normalized to V_{REF}. (Alternatively, the external resistor ratio can be selected to normalize V_{HIGH} to unity.) The gain, A, can be adjusted through the W/L ratios and β.

The load seen by the ILA will a BiCMOS input that requires low currents. If V_{LOG} in (13) has enough signal swing, there is no need for a high gain output stage at all. This is a significant costs and area savings as compared to the commercial logarithmic amplifier. Since β in (13) provides temperature compensation, it is left to the W/L ratios to ensure adequate signal swing. Simulations for the entire amplifier across the two-decade input range of 5 to 500 V and the temperature range 0 to 100°C are shown in Figures 12 and 13. The percent errors are calculated against the least squares fit to the data. As expected, operating at lower voltages results in higher percent errors of 3 to 4 %. However, between 20 V and 500 V, the anticipated error is less than 1%.

C. Frequency Response

Reviewing the Difference and Temperature Compensation blocks in Figures 6 and 10, we find that there are no high impedance nodes in the entire amplifier. At each node, except the output node, the maximum impedance is only $1/g_m$. At the output node, the equivalent resistance is

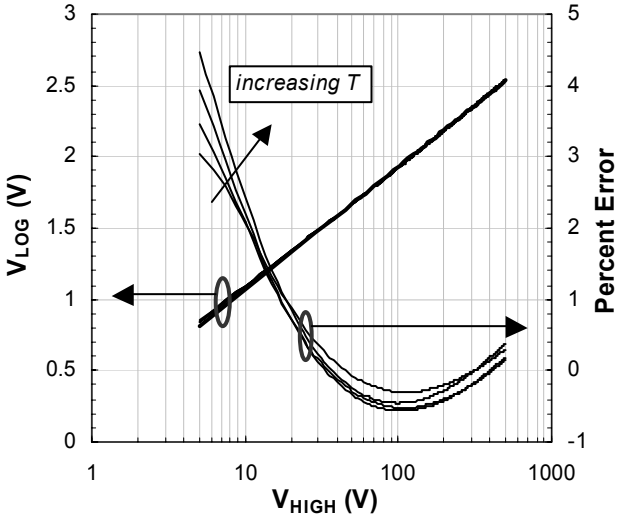


Figure 12. Simulation results show the effectiveness of the temperature compensator block in canceling most temperature effects. The percent error is calculated using a least squares fit to the data.

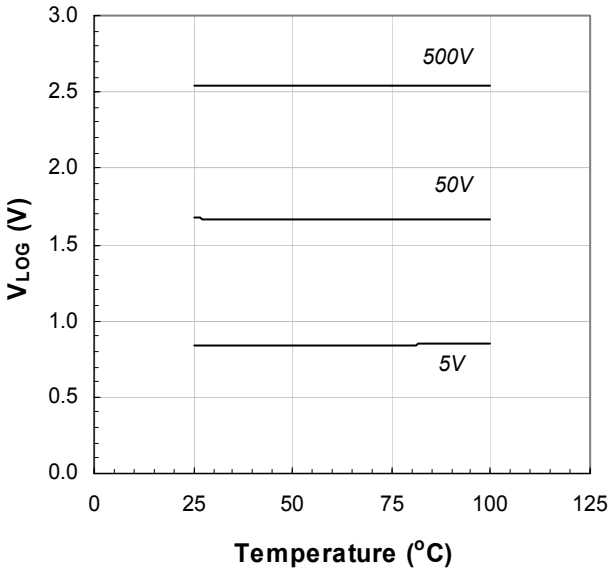


Figure 13. Simulations for the output voltage versus temperature at three different values of V_{HIGH} show the insensitivity to temperature across the input voltage span.

$$R_{OUT} = R_{TC} \,//\, r_{o8} \approx R_{TC} . \quad (14)$$

Choosing bias currents to set R_{TC} much less than $1/g_m$, the frequency response is dominated by the output capacitance – the BiCMOS input capacitance of the downstream circuitry.

As all other poles are at high frequencies, the amplifier behaves as a single pole amplifier being self-compensated by C_{OUT} and is inherently stable.

$$f_{3dB} = \frac{1}{2\pi R_{OUT} C_{OUT}} \quad (13)$$

IV. IMPLEMENTATION

The optimum technology for the ILA is a standard BiCMOS technology. Diodes would be fabricated as diode connected bipolar transistors and a variety of diffusions would be available for resistors. As the entire ILA is analog, submicron geometries are not critical. In fact, at very small gate lengths, the channel length modulation can significantly degrade the analog performance of CMOS devices.

At present the ILA and a collection of test structures are being implemented in the TSMS 0.35 μm CMOS process through the MOSIS fabrication service [7]. Diodes are implemented in the source-drain/well diffusions. Also, well diffusions are used for integrated resistors. Upon receipt the final product, the design will be tested across the temperature range 25°C to 100°C.

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