A Micropower Logarithmic A/D With Offset and Temperature Compensation

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***Abstract*—Logarithmic circuits are useful in many applications that require nonlinear signal compression, such as in speech recognition front-ends (SRFEs) and cochlear implants or bionic ears (BEs). A logarithmic current-input analog-to-digital converter (A/D) with temperature compensation and automatic offset calibration is presented in this paper. It employs a diode to compute the logarithm, a wide linear range transconductor to perform voltage-to-current conversion, and a dual-slope autozeroing topology with 60 dB of dynamic range for sampling the envelope of speech signals. The temperature dependence of the logarithm inherent in a diode implementation is automatically cancelled in our circuit topology. Experimental results from a 1.5-μm 3-V BiCMOS process show that the converter achieves a temperature stability lower than 150 ppm/°C from 12 °C to 42 °C, and consumes only 3 μW of power when sampling at 300 Hz. At this level of power consumption, we show that the design is thermal-noise limited to 8 bits of precision. This level of precision is more than adequate for deaf patients and for speech recognition front-ends. The power consumption is almost two orders of magnitude lower than state-of-the-art DSP implementations, and the use of a local feedback topology achieves a 2.5-bit improvement over conventional dual-slope designs.**

***Index Terms*—Analog-to-digital converter, bionic ear, cochlear implant, dual slope, logarithmic map, speech-recognition front-end.**

I. Introduction

BIONIC EARS (BEs) or cochlear implants have been implanted in more than 60 000 people worldwide, according to an estimate by the FDA [1]. BEs use a surgically implanted array of electrodes to stimulate the auditory nerve, which restores a measure of hearing to the deaf. The BE must therefore function as a surrogate middle and inner ear, performing the same chain of signal transduction from sound waves to electrical impulses as in the biological cochlea. Fig. 1 shows the signal-processing chain of a typical BE, with further details described in [2]–[6].

In the current generation of BEs, logarithmic compression of the signal is performed just prior to nervous stimulation. Such compression is useful because theory and experiments suggest that acoustic amplitudes are log-compressed into electrical amplitudes by the cochlea [7]–[9]. More simply, there is a linear relationship between sound intensity in dB sound pressure level (SPL) and electrical stimulation intensity in microamperes. Hence, a circuit that performs logarithmic compression is useful in BE processors.

Logarithmic compression is also inherent to cepstral speech recognition, since a logarithmic function allows the excitation signal in speech to be subtracted from the effect of filtering by the vocal tract [10]. Many speech-recognition front-ends (SRFEs) are therefore designed to produce output bits which represent log-spectral magnitudes of a microphone input signal [11]. Consequently, a low-power logarithmic analog-to-digital converter (A/D) is also very useful in portable SRFEs.

The BEs and SRFEs of today mostly employ an A/D, followed by a DSP to perform all the necessary signal processing. However, a DSP is costly in power when compared with analog processing schemes, such as those proposed in [12]–[14]. We have shown that large power savings can be realized for a fully implanted BE or portable SRFE [6], [15]. The logarithmic A/D is the final building block circuit in an analog BEs signal processing chain. It converts the current input from an envelope detector such as that described in [5] and [16] into a digital output code. In this paper, we present a logarithmic A/D (logmap) that exploits subthreshold CMOS technology to compute a logarithm in almost one hundredth the power of DSP implementations. Like the digital implementation, our analog implementation is robust and insensitive to temperature and component mismatches.

In the literature on logarithmic A/Ds, we find designs that have been proposed to handle the ultrawide dynamic range inherent in optical sensors [17], [18] and mention the limitations in overall accuracy due to temperature coefficients in the phototransducer [18]. A logarithmic A/D for high-fidelity (Hi-Fi) audio applications has also been designed to meet the requirements of low-power portable electronics [19]. Finally, high-performance systems with sampling rates in the megahertz range have been built for radio and communications applications [20], [21]. The logmap we present is tailored to meet the low-power, highly parallel, and low sampling rate requirement of speech-envelope processors like BEs and SRFEs.

This paper is organized as follows. Section II lists the logmap specifications. Section III explains our choice of a dual-slope A/D topology. Section IV describes the dual-slope operation and the advantages it confers. Section V shows how the temperature dependence in a diode's V–I curve is cancelled. Section VI examines global feedback offset correction, which is the most common method of offset correction used in dual-slope converters. Section VII shows how we can do better by using multistage local feedback for offset correction. Section VIII shows our experimental results. Section IX discusses tradeoffs between speed, precision, and power that can be made

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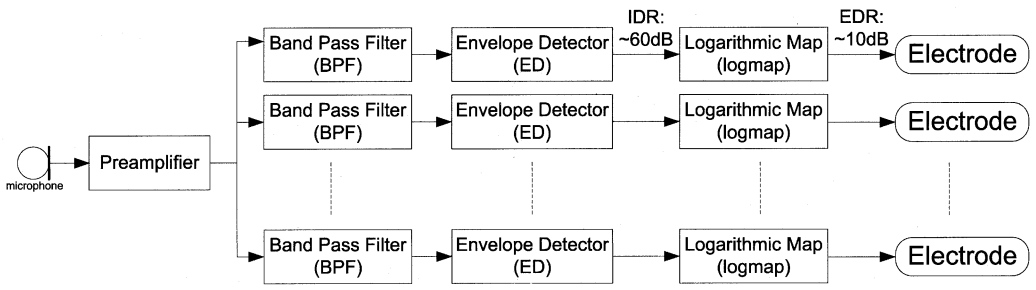

Fig. 1. Typical signal processing chain in a bionic ear.

in our converter. Finally, Section X concludes with a summary of the features in this design.

II. System Requirements and Specifications

A. Dynamic Range

The logmap should have an input dynamic range of at least 60 dB in order to handle the range within which most of normal speech will lie. This also allows the logmap to accommodate the internal dynamic range (IDR) of typical BEs, which is around 60 dB, as denoted in Fig. 1.

B. Appropriateness of an A/D for an Analog BE Processor

The IDR of a BE must be fit onto the limited electrical dynamic range (EDR) of a deaf patient's auditory nerve fibers, which may range from 10–20 dB [7], [9]. However, the threshold of sensation may vary by an additional 40 dB between patients or even between electrodes (for example, the minimum detectable electrode current may vary from 2 to 200 μA) [9]. Hence, the absolute level of output current may have to vary by as much as 60 dB, which is impractical to generate directly from subthreshold analog currents. Current BEs already make use of a digital-to-analog converter (D/A) to construct stimulation waveforms in the electrodes. Hence, it makes sense for a fully analog BE processor (as described in [6]) to generate output bits that can interface to a back-end D/A stimulator. The D/A stimulator may then be programmed to perform the requisite offset and scaling for each electrode.

C. Precision

Normal-hearing listeners can detect about 200 discriminable intensity steps within their dynamic range, while implant patients can only discriminate between 8–50 intensity steps [22]. Thus, a precision of 8 bits should be sufficient for SRFEs, while a 6-bit precision should suffice for BEs. While we present an 8-bit design in this paper, precision can be traded off for a quadratic increase in sampling rate at the same level of analog power. This relationship is derived from the precision of the A/D being limited by thermal noise.

D. Input Bandwidth and Stimulation Rate

The logmap is designed to take in a current-mode input from an envelope detector such as that described in [5] and [16]. It must also have a bandwidth of at least 300 Hz to handle the envelope variation in speech. Current cochlear implants implement intentional low-pass cutoffs between 35 and 300 Hz, since the envelope of speech is believed to vary slowly, no faster than a few 100 Hz [2]. However, to be compatible with higher stimulation rates up to 2 kHz or higher (where some implant patients have been shown to do better), we have designed for an input bandwidth of up to 5 kHz. For this 300-Hz converter, higher stimulation rates at the same level of precision require a linear increase in both analog and digital power. Higher stimulation rates at constant power may be attained by lowering precision.

E. Power

It takes a DSP about 1 MIP to compute a logarithm. So even with state-of-the-art DSPs like Texas Instrument's micropower C55x series, a logarithm will require about 250 μW to compute [23]. We shall show that this converter consumes only 1 μW in the analog section and 2 μW for the digital control. The enormous saving in power is, therefore, the primary motivation behind this design.

F. Power Supply Rejection

As with any analog circuit, there is a concern that power supply noise will adversely affect performance. As our A/D must perform in noisy environments, we need to guarantee some minimum level of power supply rejection.

G. Temperature Stability

Although a fully implanted BE may have a well-regulated external temperature, there may be internal temperature gradients set up in the device by neighboring high-power circuits. Furthermore, a subthreshold circuit can be sensitive to even small temperature variations, because subthreshold currents vary exponentially with temperature [24]. As we can expect fully implanted BEs and portable SRFEs to be exposed to changing thermal environments, it is important for the logmap to have some built-in immunity to temperature fluctuations.

III. Choice of A/D Architecture

A dual-slope integrator was chosen to perform the logarithmic A/D conversion, for two main reasons: First, both BEs and SRFEs break down the input spectrum into 8–32 channels. A complete BE processor or SRFE will, therefore, require 8–32 logmaps to be operating in parallel. The use of an integrating A/D topology allows a single clocking waveform and counter to be shared between the logmaps to implement quantization. As the clocking waveform is the highest frequency signal on chip, the ability to amortize its cost in terms of power and area

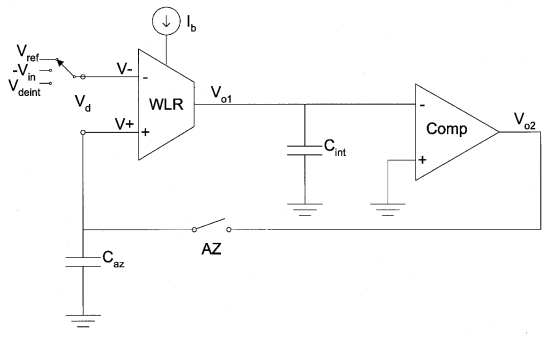

Fig. 2. Circuit implementation of a basic dual-slope converter.

is a tremendous advantage for highly parallel systems like BEs and SRFEs.

Second, the sensitive temperature dependence of subthreshold bias currents is automatically cancelled in a dual-slope topology. If we guarantee that the charging current and discharging current in the topology are derived from a single bias current, any temperature dependence in that bias current gets divided out in the conversion. A dual-slope A/D topology has inherent immunity to component drift because component values such as capacitance serve as intermediate variables that cancel out in the final answer. This is advantageous in BEs and SRFEs, which are intended for long-term usage, and need to preserve their accuracy over long periods of time. We show that our experimentally measured precision is limited only by thermal noise, which is fundamental and unavoidable. The precision of D/As such as in successive approximation topologies, or capacitor matching such as in pipelined topologies, does not matter in dual-slope topologies. Although matching problems may be solved through calibration, such solutions require more complexity and area.

IV. Dual-Slope Integrating A/D

A simplified circuit implementation of a dual-slope converter is shown in Fig. 2. It consists of a wide-linear-range operational transconductance amplifier (WLR OTA) [25] and integrating capacitor $C_{\rm int}$ to serve as the integrator, another amplifier to serve as the comparator (a standard five-transistor OTA suffices), and an offset storage capacitor $C_{\rm az}$. The latter three components are tied in a global feedback loop when the auto-zeroing switch AZ is closed. The A/D conversion has three phases of operation. During phase I, $V-$ is tied to $V_{\rm ref}$ and switch AZ is closed, so the offset of the WLR is stored on $C_{\rm az}$ and the offset of the comparator is stored on $C_{\rm int}$. In phase II, AZ is opened, and $V-$ is switched to $-V_{\rm in}$, which causes the WLR to charge up $C_{\rm int}$ with a current $I_{\rm int}$ proportional to $V_{\rm in}$, for a fixed time $T_{\rm int}$. $V_{\rm o1}$ will hence reach a final voltage V_f, proportional to $V_{\rm in}$. Finally, in phase III, $V-$ is switched to $V_{\rm deint}$ (while AZ stays open), which causes the WLR to discharge $C_{\rm int}$ back down to ground, with a fixed current $I_{\rm deint}$. The time it takes to discharge, called $T_{\rm deint}$, is proportional to V_f. This time is counted with a clock, and is thereby a digital measure of $V_{\rm in}$. These three phases are diagrammed in Fig. 3.

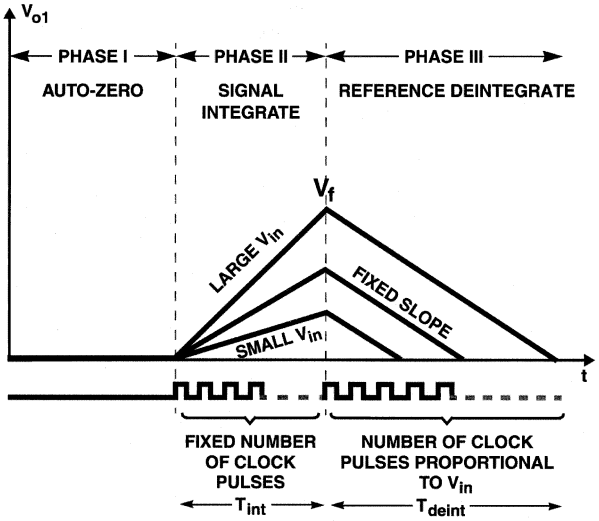

Fig. 3. Dual-slope operation.

This auto-zeroing algorithm found in standard dual-slope architectures [26] allows one to reduce the dc offset in each amplifier by the loop gain of the feedback loop.

Another property of the dual-slope strategy stems from the ratiometric dependence of $T_{\rm deint}$ on $I_{\rm int}/I_{\rm deint}$, as shown in the following equation:

$$\begin{aligned} V_f &= \frac{I_{\rm int}}{C_{\rm int}} \times T_{\rm int} \quad (I \rightarrow V \text{ transformation}) \\ T_{\rm deint} &= \frac{V_f}{I_{\rm deint}/C_{\rm int}} \quad (V \rightarrow t \text{ transformation}) \\ &= \frac{I_{\rm int}}{I_{\rm deint}} \times T_{\rm int}. \end{aligned} \tag{1}$$

$T_{\rm deint}$ is thus the product of a current-to-time conversion, computed through the intermediate voltage V_f. However, this relation can be derived more simply if we note that no net charge was added to the capacitor over the conversion cycle, since $C_{\rm int}$ starts and ends in the same state. Then by conservation of charge, we can arrive at

$$\begin{aligned} \mathrm{Q}_{\rm added} &= \mathrm{Q}_{\rm removed} \\ I_{\rm int} \cdot T_{\rm int} &= I_{\rm deint} \cdot T_{\rm deint} \\ T_{\rm deint} &= \frac{I_{\rm int}}{I_{\rm deint}} \cdot T_{\rm int}. \end{aligned} \tag{2}$$

Dual-slope conversion, therefore, has the property of path-independence (in voltage), which supports the fact that both capacitance and voltage are intermediate variables which cancel out in (1). Any nonlinearity in $C_{\rm int}$ therefore does not matter, and also renders the A/D insensitive to component drift.

Furthermore, since $I_{\rm int}$ and $I_{\rm deint}$ are both generated by the same WLR with bias current I_b (as in Fig. 2), any dependence of these currents on I_b is divided out when we take the ratio of the currents in (2). The ratiometric nature of the converter provides it with immunity to temperature and other slow variations in I_b.

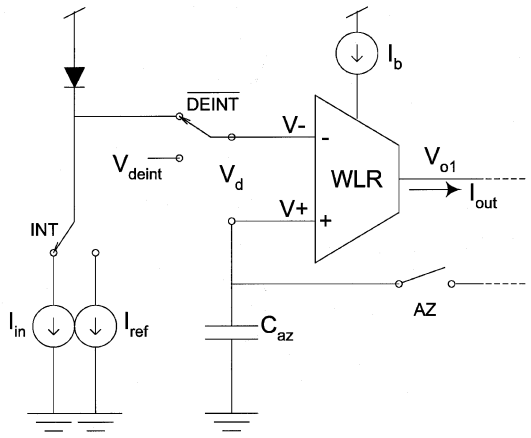

Fig. 4. Logarithmic I-to-V-to-I conversion.

V. Making the A/D Input Stage Logarithmic and Temperature Independent

For the dual-slope converter to be a logarithmic A/D, $V_{\rm in}$ (or equivalently, the differential voltage $V_{\rm d}$ in Fig. 2) must be a logarithmic function of the current input $I_{\rm in}$. The logarithm is easily implemented by letting $I_{\rm in}$ drop a voltage across a device with an exponential I–V characteristic. The device is typically a diode, a bipolar transistor, or an MOS transistor in the subthreshold regime. A logarithmic input stage to our A/D can thus be implemented as shown in Fig. 4. During the auto- zeroing phase, a reference input current $(I_{\rm ref})$ corresponding to a minimum envelope detector output is fed to the diode, while, during the integration phase, the actual input current $I_{\rm in}$ is fed to the diode. During the de-integration phase, the WLR input is tied to $V_{\rm deint}$, otherwise it is tied to the diode output.

The voltage across the diode increases by ϕ_T per e-fold increase in current. Hence, the differential voltage $V_{\rm d}$ is given by

$$\begin{aligned} V_d &= \phi_T \ln \frac{I_{\rm in}}{I_s} - \phi_T \ln \frac{I_{\rm ref}}{I_s} \\ &= \phi_T \ln \frac{I_{\rm in}}{I_{\rm ref}} \quad (\log I \rightarrow V \text{ transformation}). \end{aligned} \tag{3}$$

By taking the difference between two logarithmic voltages, the dependence on the saturation current of the diode I_s is cancelled, and any temperature coefficient common to $I_{\rm in}$ and $I_{\rm ref}$ is also divided out. This is important because I_s and subthreshold currents both vary strongly with temperature. The temperature dependence remaining in V_d is now merely proportional to absolute temperature (PTAT). However, the transfer function from $I_{\rm in}$ to $I_{\rm out}$ in Fig. 4 is given by

$$\begin{aligned} I_{\rm out} &= G_m \cdot V_d \quad (\text{linear } V \rightarrow I \text{ transformation}) \\ &= \frac{I_b}{V_L} \cdot \phi_T \ln \frac{I_{\rm in}}{I_{\rm ref}} \end{aligned} \tag{4}$$

where V_L is defined as the linear range of the G_m transconductor and I_b is its bias current. Since the linear range of a subthreshold transconductor is also PTAT because of its dependence on ϕ_T [25], the PTAT dependence of ϕ_T cancels with the PTAT dependence of V_L and $I_{\rm out}$ now only bears the temperature dependence of I_b. However, the dual-slope topology cancels the temperature dependence of I_b as well: (2) shows that if the integration and de-integration currents are both proportional to I_b as they are in the scheme of Fig. 4, then the final digitized value that is proportional to $T_{\rm deint}$ is independent of I_b.

For accurate cancellation, the WLR and diode need to be in thermal proximity. More importantly, we must operate within the linear range of the transconductor at all times. We use the techniques of bump linearization, well inputs, and source degeneration as described in [25] to extend V_L to at least 180 mV, the diode voltage range corresponding to a 60-dB range in input current.

VI. Global Feedback: Dynamics and Noise Analysis

Auto-zeroing dual-slope integrators traditionally rely on global feedback, such that offsets in the integrator and comparator blocks can be zeroed out together [26]. By global feedback, we mean that one global feedback loop automatically ensures that the offset of the WLR and the offset of the comparator in Fig. 2 are zeroed out. In contrast, we describe a local feedback scheme for zeroing offsets in Section VII that uses two separate feedback loops for zeroing out each of these offsets. In this section, we present experimental results from a traditional global feedback converter before describing our local feedback converter in Section VII.

The global feedback of Fig. 2 has poor phase margin without compensation because the WLR and comparator blocks have high dc gain and slow dominant poles. The loop was therefore compensated with a classic split-pole technique as employed in standard two-stage operational amplifiers [27], and employs an additional OTA follower to act as a feedback resistor. This compensation scheme is described in [29].

A dual-slope converter with this global feedback topology was fabricated in a 1.5-μm process, with $C_{\rm int} = 1.5$ pF and $C_{\rm az} = 2$ pF. When biased with the requisite current for a sampling rate of 300 Hz, we measured the power spectral density (PSD) of the noise on $V_{\rm o2}$ during the auto-zeroing phase, and found very good agreement with theory. The calculations were done in a manner analogous to noise calculations described in [4] and [28] and are described in detail in [29]. They take into account shot noise from all transistors in the circuit (the dominant form of noise in subthreshold MOS operation) and their effect on the overall circuit noise due to differing transfer functions to the output. We shall not describe these tedious but straightforward calculations here.

Fig. 5 shows the measured PSD and total noise at the node $V_{\rm o2}$ $(=V+)$ when the switch AZ is closed in Fig. 2. The measurements were obtained with a SR785 Spectrum Analyzer. Below 10 kHz, the total PSD is dominated by the contribution from the WLR. However, at frequencies greater than 10 kHz, the total PSD curve starts to flatten out, because the contribution from the comparator becomes more significant. The cumulative noise power is integrated over frequency on the lower plot in Fig. 5, with the total calculated noise being 348 μVrms and the total measured noise being 375 μVrms. However, the 375 μVrms number only measures the standard deviation of the noise distribution. The peak-to-peak noise amplitude is almost 3 mV, because the peak-to-rms ratio of a

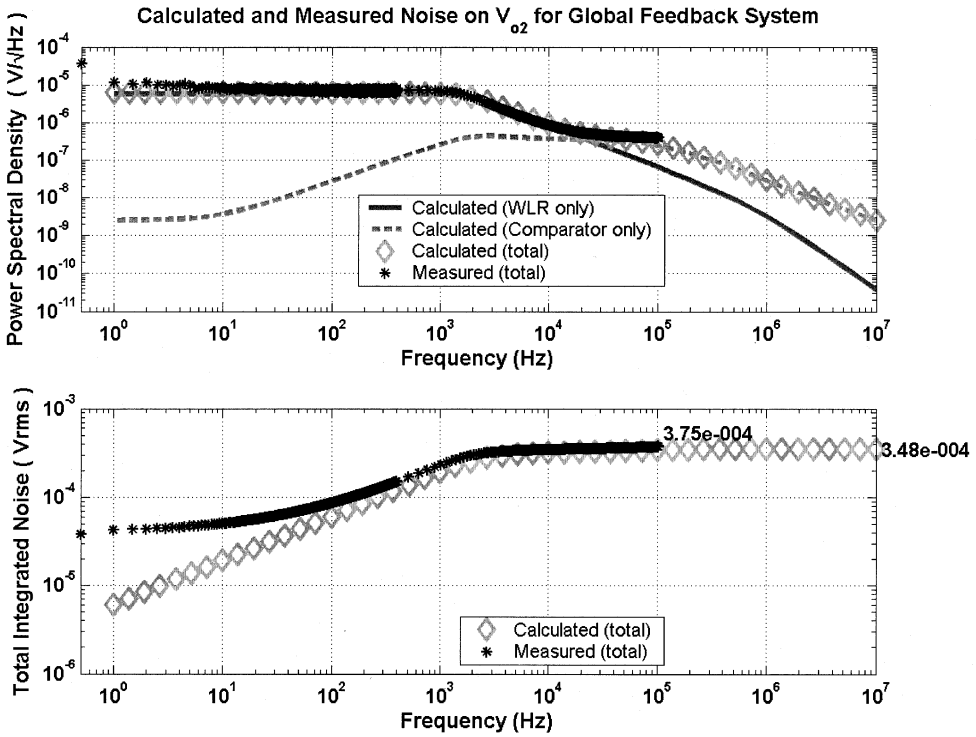

Fig. 5. Power spectral density and total integrated noise on V_{o2} in the global feedback converter.

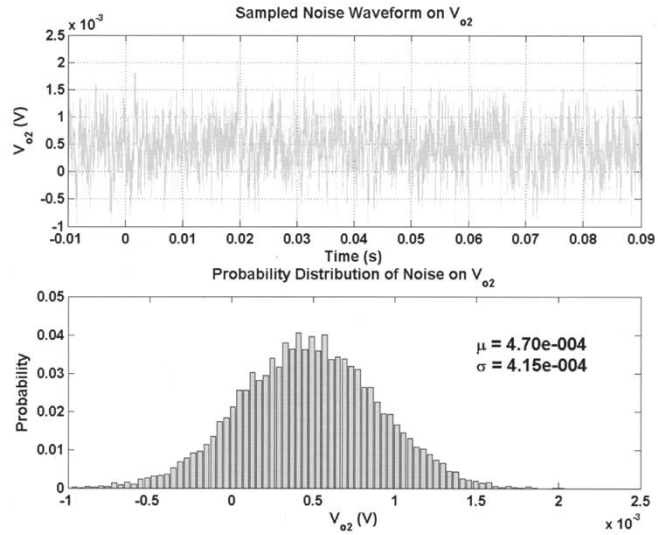

Fig. 6. Time-domain profile of noise on V_{o2} in the global feedback converter.

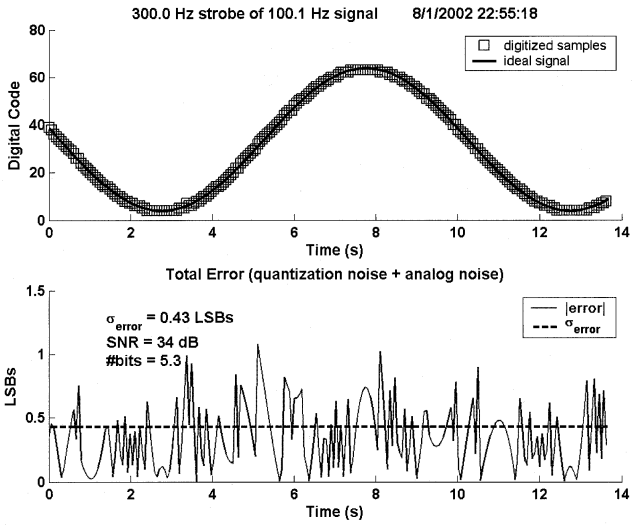

Fig. 7. SNR test of the global feedback converter.

Gaussian noise signal is 3–3.5, implying that the peak-to-peak noise is 6–7 times the rms value.

The time-domain waveform of the noise of V_{o2} is shown in the upper plot of Fig. 6. Each sample is binned to create a histogram of the noise distribution on the lower MATLAB plot. The time-domain waveform shows clearly that the noise on V_{o2}, when sampled onto the input, reduces the converter's precision by a full 3 mV rather than just a single standard deviation of approximately 400 μV. Of course, this is true only if we insist on having a very low bit-error rate on all bits of the converter, including the least significant bit (LSB). As this converter uses subthreshold MOS diodes, it has an input full scale of $\phi_T/\kappa \cdot \ln(1000) \approx 280$ mV [24]. Hence, 3 mV of thermal noise at the input immediately restricts us to an analog precision of $280/3 \approx 93$ discriminable levels, or 6.5 bits.

We confirm this precision using a standard sine-tone signal-to-noise ratio (SNR) test for A/D converters [30], [31]. Fig. 7 shows that a 100.1-Hz sine input stroboscopically sampled at 300 Hz has an SNR of 34 dB, yielding a precision of 5.3 bits. The digital bits were read out by an Agilent 1670G Logic Analyzer. The degradation of $\sim$1 bit from the analog precision of 6.5 bits is due to additional noise introduced by quantization of the analog signal [32].

TABLE I
ANALOG POWER CONSUMPTION OF THE GLOBAL FEEDBACK CONVERTER

Block	Power consumption
WLR	0.09 μW
Comparator	0.30 μW
Follower (for freq. compensation)	0.30 μW
V_{deint} biasing	0.27 μW
Total	0.96 μW

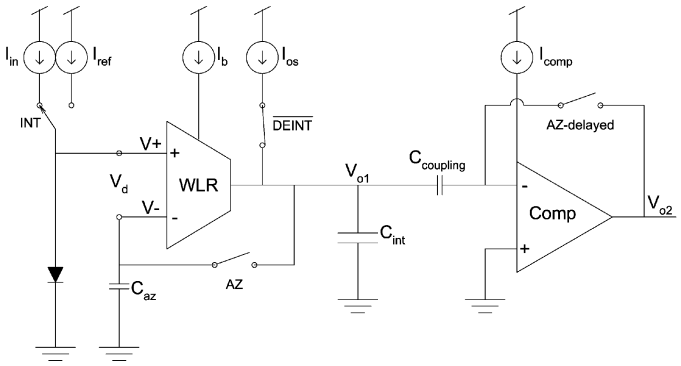

Fig. 8. Logarithmic A/D local feedback topology.

Other sources of noise in the circuit do not limit its precision like the sampled thermal noise of V_{o2} does. For example, the input-referred noise of the comparator is sampled onto V_{o1} during auto-zeroing but does not result in much error because it is a small fraction of the 2-V full scale of V_{o1}. Effectively, when referred to the input, the latter error is reduced by the gain of the integrating stage, $A_{int} \triangleq 2\ V/280$ mV. The noise at the input diode, the noise contributed by the follower used for feedback compensation, the integration of shot-noise currents during conversion, and the comparator's input-referred voltage noise were all found to be small in comparison with the sampled thermal noise on C_{az}.

The analog power consumption of the various subcircuits of Fig. 2 is listed in Table I.

VII. LOCAL FEEDBACK: A 2.5-BIT IMPROVEMENT IN PRECISION

As we have shown above, the precision of a global feedback topology is determined by the level of thermal noise sampled onto the offset capacitor C_{az}. In this section, we present a local feedback design, in which feedback loops are closed around each amplifier block individually. This strategy enables the noise on C_{az} to be lowered at the same level of power, and consequently improves the precision. A schematic of this local feedback design is given in Fig. 8.

The operation is similar to the global feedback topology; when AZ and AZ-delayed are closed, the WLR and comparator both auto-zero their offset. During this time, I_{ref} is applied to the input diode and I_{os} to the output of the WLR. Switch AZ is opened just before AZ-delayed, to avoid the latter's charge injection from affecting C_{az}. In the integrate phase, I_{in} is switched onto $V+$, and the WLR charges up C_{int} with a current

TABLE II
ANALOG POWER CONSUMPTION OF THE LOCAL FEEDBACK CONVERTER

Block	Power consumption
WLR	0.60 μW
Comparator	0.30 μW
I_{os} biasing	0.15 μW
Total	1.05 μW

proportional to its input differential voltage V_d, which measures the log of I_{in}/I_{ref}. To de-integrate, I_{ref} is switched back onto the diode, and I_{os} is disconnected from V_{o1}. This action forces the WLR to discharge C_{int} with a current equal in magnitude to I_{os}. The current I_{os} serves as the de-integration current, and is a scaled copy of I_b in order to preserve the ratiometric cancellation described by (2). The current I_{os} serves not only as the de-integration current, but also to offset the WLR into the negative quadrant of its linear range, thus doubling the useable linearity of the WLR.

The noise on C_{az} is lowered in this topology because of the following reasons. First, the devices which contribute noise to C_{az} are reduced to devices in the WLR alone, not devices in the WLR and comparator. This is because the comparator noise is greatly attenuated by a dc-blocking capacitor $C_{coupling}$, so its effect on V_{o1} is minimal. Second, we note from Table I that a large quantity of power is spent in the follower, to compensate the global feedback loop. In this topology, each amplifier is unity-gain stable, hence no compensation is required. All the power that was spent on compensation can therefore be used to increase the bias in the WLR, which allows a larger value of C_{int} to be used, while maintaining the same sampling rate. The larger value of C_{int} therefore lowers the WLR noise, which is the dominant source of noise. The redistribution of power is listed in Table II.

This topology also allows the effect of charge injection to be minimized. First, charge injection from AZ does not affect the comparator offset, since the comparator is still being reset when switch AZ is turned off. Second, when AZ-delayed breaks the feedback around the comparator, the charge injection onto C_{int} is divided by the gain of the integrating stage, A_{int}. Thus, the only charge injection that matters is that of the switch AZ onto C_{az}. However, even this is only a fixed offset error, which does not reduce the precision of the converter. This approach to minimizing charge injection is well known in multistage comparators and useful to us as well [33].

The importance of minimizing the WLR's linear range can be understood from the shot noise calculations of a subthreshold G_m-C filter as developed in [4], where N is the equivalent number of shot noise sources. These calculations are given as follows:

$$\begin{aligned}\text{WLR PSD}^2 &= \frac{N \cdot 2q \cdot (I_b/3)}{{G_m}^2} = \frac{N \cdot 2q \cdot V_L^2}{3I_b} \\ \text{WLR Noise}^2 &= \text{WLR PSD}^2 \cdot \text{BW} \cdot \frac{\pi}{2} \\ &= \frac{N \cdot 2q \cdot (I_b/3)}{{G_m}^2} \cdot \frac{G_m}{2\pi C} \cdot \frac{\pi}{2} \\ \text{WLR Noise} &= \sqrt{\frac{N \cdot q \cdot V_L}{6C}}. \end{aligned} \tag{5}$$

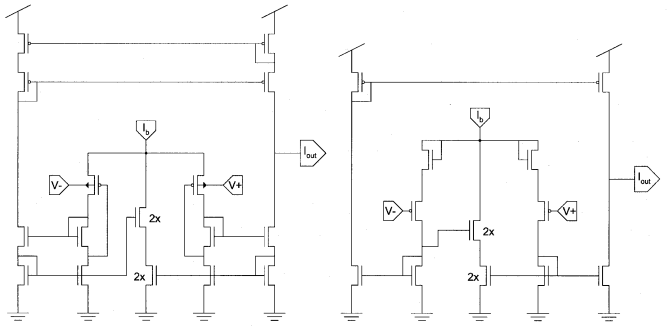

Fig. 9. Well-input WLR used in global feedback on the left, and gate-input WLR used in local feedback on the right.

Note that $I_b/3$ flows through each transistor instead of the usual $I_b/2$, due to the use of bump-linearization to extend V_L [25]. As the total noise increases with the square root of V_L, we need V_L to be as low as can be and still handle the full input range. To accommodate a reduction in V_L, real diodes are used to give the converter a smaller input full scale of 180 mV, corresponding to the desired 60-dB dynamic range in input current. The use of real diodes, together with the current offset of $I_{\rm os}$, then allow V_L to be several times smaller than that of the global feedback design. The WLR topologies used in both designs are shown in Fig. 9.

The WLR noise is reduced by the difference in $\sqrt{(N \cdot V_L)}$ between the two topologies. The gate-input WLR with a smaller V_L ($N = 7, V_L = 240$ mV) achieves $\sqrt{2.5}$ or $1.6\times$ less noise than the well-input WLR ($N = 3.5, V_L = 1.2$ V) for the same sized $C_{\rm int}$. Calculations for the above values of N and V_L are described in [29]. This improvement accounts for less than a 1-bit increase in precision but is nevertheless significant.

The more important improvement comes from our ability to increase the size of $C_{\rm int}$. As we have a smaller V_L and can also use more power in the WLR, we were able to increase the value of $C_{\rm int}$ from 1.5 pF in the global feedback case to 30 pF in the local feedback case, while maintaining the same closed-loop bandwidth as before, i.e., $G_m/(2\pi C) = 1.3$ kHz.[1]

In addition, $C_{\rm az}$ and $C_{\rm coupling}$ were set at 10 pF each, bringing the total capacitance seen at $V_{\rm o1}$ to 50 pF during auto-zeroing. The shot noise contributed by the WLR is therefore reduced by a factor of $\sqrt{(50\ {\rm pF}/1.5\ {\rm pF}) \times 2.5} = \sqrt{83}$ or roughly $9\times$ from the global feedback topology. Table III summarizes the various mechanisms for noise reduction between the global and local feedback topologies.

From Table III, we immediately note two things: First, our measurement of total noise for the global feedback topology is 375 μVrms, rather than 273 μVrms as calculated here, because the well-input WLR is not in a unity feedback G_m-C configuration. Loop dynamics and the comparator's noise contribution account for an additional 100 μV of noise in global feedback, which is substantial. Second, by reducing the WLR noise to 30 μVrms, another thermal noise source that was previously negligible now becomes comparable, namely, the noise contributed from the input diode. We calculate the effect of the diode below, where $I_{\rm ref} = 320$ pA, $g_m = I_{\rm ref}/\phi_T$, and $N = 2$

[1]The 1.3-kHz bandwidth allows complete auto-zero settling when our sampling frequency is 300 Hz.

TABLE III
REDUCTION IN WLR NOISE (ASSUMING G_m-C CONFIGURATION) ALLOWED FOR BY A CHANGE IN TOPOLOGY

Parameter	Well-input WLR	Gate-input WLR
N	3.5	7
V_L	1.2V	240mV
$C_{\rm int}$	1.5pF	50pF
Total Noise	273 μVrms	30 μVrms

TABLE IV
TOTAL NOISE CONTRIBUTIONS FROM WLR AND DIODE

	PSD (μV/$\sqrt{\rm Hz}$)	Total noise (μVrms)
WLR	0.66	30
Diode	1.2	54
Total	1.4	62

because the current source feeding the diode also accounts for a device's worth of noise. These calculations are

$$\begin{aligned}\text{Diode PSD} &= \sqrt{\frac{N \cdot 2q \cdot I_{\rm ref}}{g_m^2}} \\ &= \sqrt{\frac{2 \cdot 2q \cdot \phi_T^2}{I_{\rm ref}}} \approx 1.2\ \mu V/\sqrt{\rm Hz} \\ \text{Diode Noise} &= \text{Diode PSD} \times \sqrt{\text{WLR BW} \times \frac{\pi}{2}} \\ &= 1.2\ \mu V/\sqrt{\rm Hz} \times \sqrt{1.3\ {\rm kHz} \times \frac{\pi}{2}} \approx 54\ \mu{\rm Vrms}.\end{aligned} \tag{6}$$

The diode and WLR noise sources are statistically independent; hence, we can calculate their combined effect by taking the square root of the sum of their squares. In addition, we can predict the total noise PSD by the same method. Using $I_b = 100$ nA, $N = 7$ and $V_L = 0.24$ V, the WLR PSD can be calculated from (5). The results are shown in Table IV.

Compared with $\sim$375 μVrms of noise in the global feedback topology, local feedback achieves a roughly $6\times$ reduction in noise, amounting to an extra 2.5 bits of precision. Thus, we are able to do substantially better than conventional dual-slope topologies which employ global feedback for auto-zeroing, by using local feedback instead.

VIII. EXPERIMENTAL RESULTS

A. Scope Waveforms

Fig. 10 is an oscilloscope screenshot of a typical dual-slope conversion cycle. The scale is 200 mV/div on the y axis and 200 μs/div on the x axis. The voltage $V_{\rm o1}$ shows the dual-slope waveform, with an upward integration for a fixed time of 800 μs ($T_{\rm int}$), the de-integration for a measured time of 280 μs ($T_{\rm deint}$), and finally, the auto-zeroing phase once de-integration is complete. $V_{\rm o2}$ shows the comparator output going low upon the start of integration. Once de-integration is complete, $V_{\rm o2}$ goes high

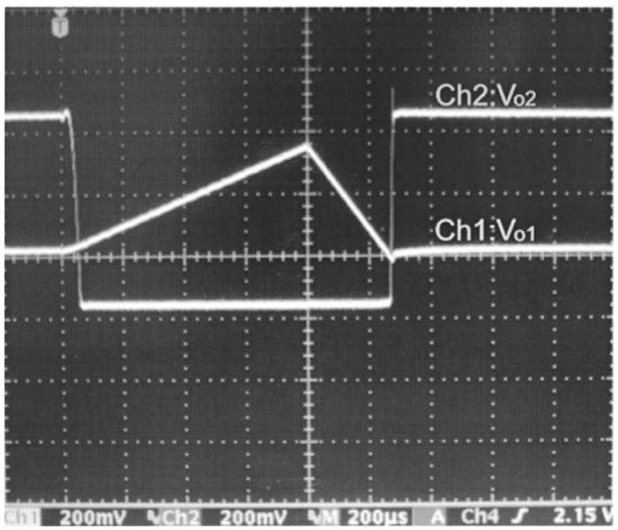

Fig. 10. Typical dual-slope (V_{o1}) and comparator (V_{o2}) waveforms.

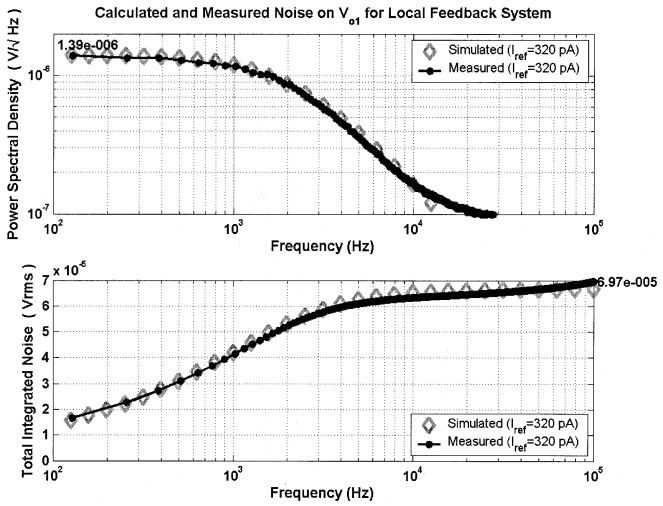

Fig. 11. Power spectral density and total integrated noise on V_{o1} in the local feedback converter.

again, and like V_{o1}, auto-zeroes to its initial level immediately thereafter.

B. Noise and Precision Measurements

Measured experimental values for the PSD and total integrated noise on node V_{o1} are plotted in Fig. 11, together with SPICE simulation results. The I_{ref} used is 320 pA, corresponding to a minimum detectable level for I_{in}. Measured results are seen to agree closely with simulation, and also match predicted levels from theory. The measured PSD is 1.39 μV/$\sqrt{}$Hz, matching the calculated level of 1.4 μV/$\sqrt{}$Hz. A first-order roll-off is also observed slightly above 1 kHz, near the calculated closed-loop bandwidth of 1.3 kHz. Finally, the total integrated noise comes to 70 μVrms, near the calculated level of 62 μVrms.

From (6), we predict that as I_{ref} is increased, the diode PSD will become negligible compared with the WLR PSD. To verify this prediction, the total PSD at $V+$ and V_{o1} in Fig. 8 at various levels of I_{ref} were measured and are plotted in Fig. 12.

We see the diode's underlying contribution by looking at the power spectrum on $V+$. First, the PSD is indeed 1.2 μV/$\sqrt{}$Hz when $I_{ref} = 320$ pA, and reduces by a factor of $\sqrt{2}$ when I_{ref} is doubled, verifying our theoretical calculations in (6). Second, the -3-dB bandwidth at $V+$ is around 5 kHz, and indeed is higher than the 1.3-kHz bandwidth set by the WLR. Thus, $V+$ has the ability to follow faster signals if a higher sampling rate is desired. When $I_{ref} = 100$ nA, the noise power contributed by the diode (measured by the PSD on $V+$) drops far below the PSD measured on V_{o1}. Thus, Fig. 12 shows that when $I_{ref} = 100$ nA, the measured PSD of 750 nV/$\sqrt{}$Hz on V_{o1} is dominated by the noise of the WLR, not by the noise of the diode. This noise is slightly higher than the predicted 660 nV/$\sqrt{}$Hz thermal noise of the WLR because of the influence of $1/f$ noise, somewhat significant at the high bias current level of $I_b = 100$ nA in the WLR.[2] Not surprisingly, the total

[2]In subthreshold, $1/f$ noise gets more significant at relatively higher bias levels [25] but is still usually not as dominant as thermal noise for device sizes that are at least $10\lambda \times 10\lambda$, with 2λ being the effective gate length.

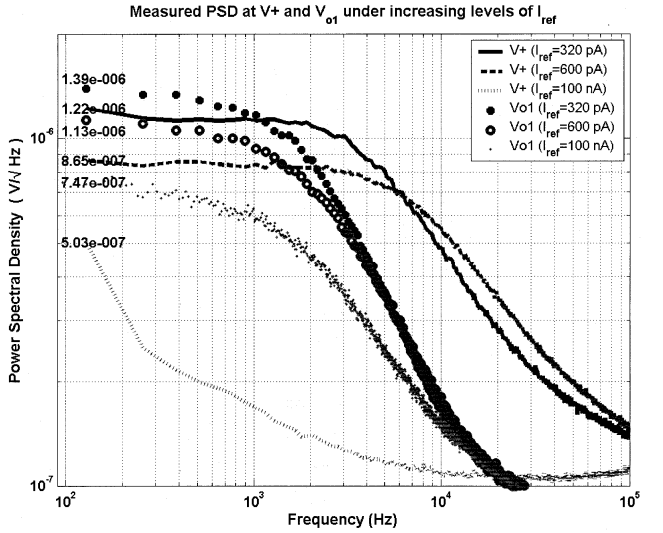

Fig. 12. Reduction in PSD with increasing values of I_{ref}. The curves for $I_{ref} = 320$ pA and 600 pA show the diode noise (noise at $V+$) dominating the total PSD on V_{o1}, while the curves for $I_{ref} = 100$ nA show the WLR noise dominating the total PSD on V_{o1}.

integrated noise is 70 μVrms, slightly higher than the calculated value of 62 μVrms. A value of I_{ref} that is approximately 320 pA makes the thermal noise of the diode dominant over the WLR and sets the minimum required current input to the circuit.

The time-domain measurements of Fig. 13 confirm the expected 70 μVrms of noise on V_{o1} and the approximate 420 μV peak-to-peak 6σ spread of this noise in a Gaussian distribution.

The analog precision is therefore limited to $180/0.42 \approx 428$ discriminable levels, or 8.7 bits. The converter once again suffers the loss of $\sim$1 bit in the quantization process, and yields a final precision of 7.8 bits as shown by the SNR measurement in Fig. 14.

These results show that the local feedback converter indeed presents a $6\times$ or 2.5-bit improvement over the 5.3-bit global feedback converter, to arrive at a digital precision just under 8 bits *at the same level of power*.

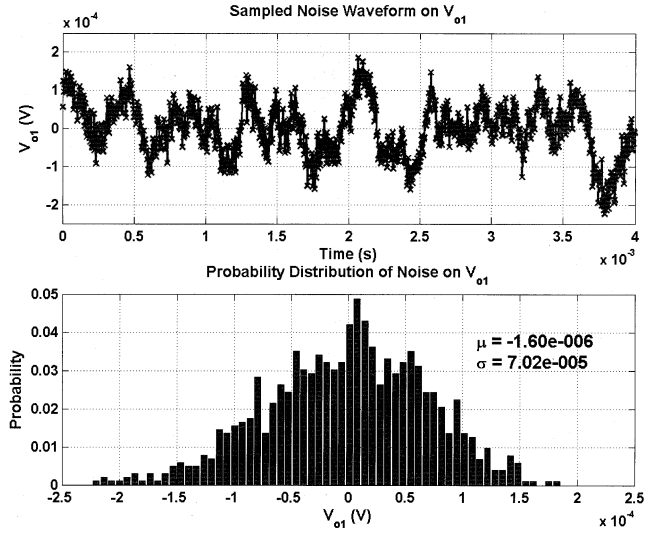

Fig. 13. Time-domain profile of noise on V_{o1} in the local feedback converter.

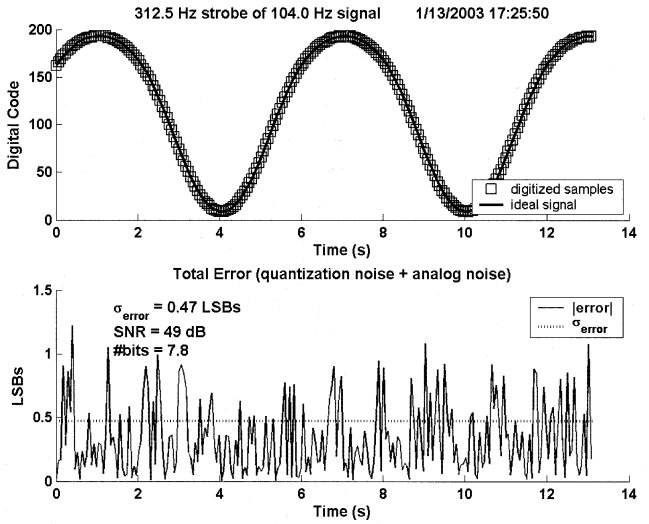

Fig. 14. SNR test of the local feedback converter.

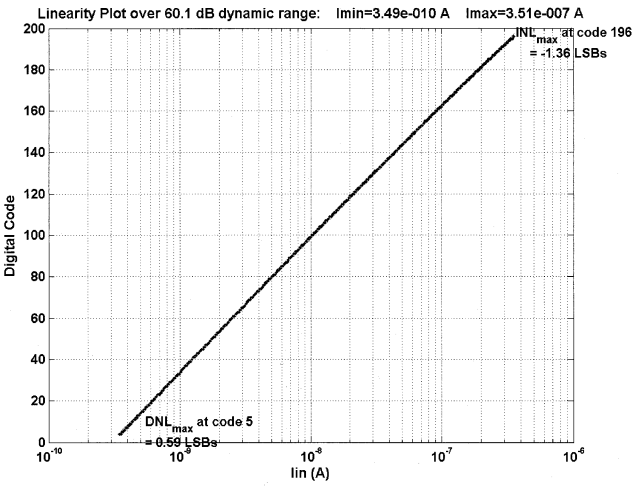

Fig. 15. Transfer curve showing the logarithmic A/D conversion.

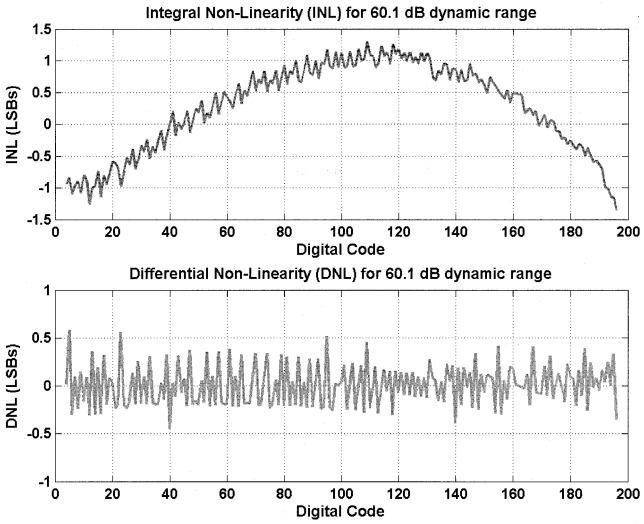

Fig. 16. Integral and differential nonlinearity curves.

C. Linearity

The current input was swept over 60 dB from 350 pA to 350 nA, and the transfer curve is plotted in Fig. 15. We observe that the transfer characteristic is monotonic and fairly linear, with the worst nonlinearities occurring at either end of the input range. The integral nonlinearity (INL) and differential nonlinearity (DNL) were computed in MATLAB as defined in [28] and plotted in Fig. 16, which shows an INL of approximately ± 1 LSB and a DNL of $\pm 1/2$ LSB across the input range, which is unlikely to adversely affect performance.

D. Power Supply Rejection

To test the A/D's power supply rejection, a 100-mVpp tone was applied to its power supply rail, and the degradation in analog precision was obtained by measuring the total spread of the output pulse $T_{\rm deint}$'s jitter. This data is plotted in Fig. 17. At an 8-bit 312.5-Hz sampling rate, the pulsewidth of 1 LSB or one clock cycle corresponds to 6.25 μs. Hence, the analog precision of the converter may be expressed in bits. The lower plot of

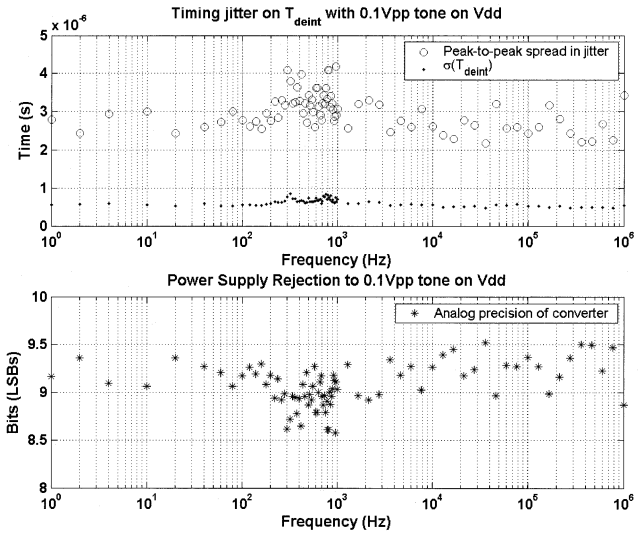

Fig. 17. Power supply rejection of the logmap A/D.

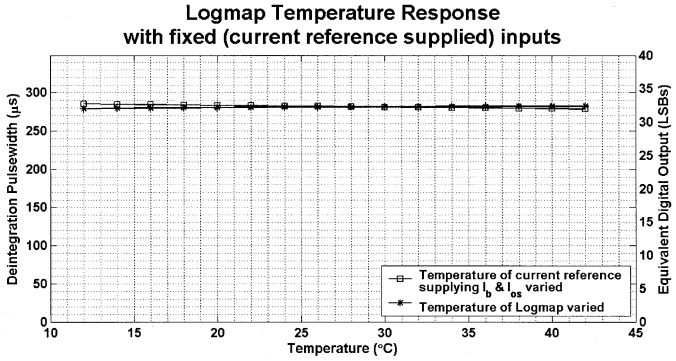

Fig. 18. Temperature dependence of the logmap A/D.

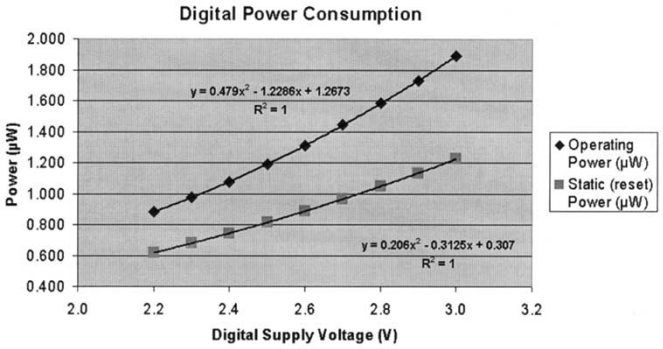

Fig. 19. Digital power consumption in the logmap A/D.

Fig. 17 shows that over a wide range of interfering power supply frequencies, the converter maintains 9 bits of analog precision before quantization, as predicted in Section VIII-B.

These results were obtained by supplying the logmap with fixed inputs and fixed biases from two off-chip current references, each having ∼60 dB of power supply rejection. In subthreshold, where an exponential sensitivity to gate voltage exists, it is necessary to use such references for robust current biasing. Nevertheless, our circuit will operate robustly as long as $I_{\rm in}$ and $I_{\rm ref}$ vary concomitantly with an interfering signal.

E. Temperature Independence

As we discussed in Section V, the differential voltage $V_{\rm d}$ of the WLR due to the input diode and the linear range of the WLR, V_L, are both PTAT. The output of the logmap, which is determined by their ratio, is therefore invariant with temperature. Also, the dual-slope converter divides out any temperature-dependent change in both the integration current (proportional to I_b) and de-integration current (proportional to $I_{\rm os}$) as described in (2). Fig. 18 shows data from experiments designed to test these hypotheses over a range of temperatures from 12 °C to 42 °C. The temperatures were controlled with Temptronic's TP04100A temperature forcing system, which uses a high-velocity temperature-controlled air stream with thermocoupled feedback to precisely set the temperature of a device.

When we vary the temperature of the logmap itself and plot the change in the logmap output as asterisks, the total change over 30 °C is seen to be less than 1/2 of an LSB. The asterisk data thus show that the $V_{\rm d}$-with-V_L temperature cancellation is effective. When we vary the temperature of a PTAT current reference supplying both I_b and $I_{\rm os}$, and plot the response as square boxes, the total change over 30 °C is less than 1 LSB. Hence, the temperature dependence of this 8-bit logmap is better than 150 ppm/°C.

F. Digital Power Consumption

The digital power consumption was measured and plotted in Fig. 19 as the digital power supply is increased from 2.2 to 3 V, with a static midrange input applied. The digital section is seen to consume ∼2 μW of power on a 3-V rail. The data was fit to a quadratic model, and the near-perfect fit is as expected from the formula $P = f \cdot C \cdot V_{\rm dd}^2$ [34]. The digital counter consumes most of the power even when the controller is held in reset, as shown by the square boxes. Thus, we can conclude that the controller consumes only 33% to 40% of the total power. Therefore, significant power savings can be obtained in multichannel systems by latching a single global counter's value into each local converter at the termination of its de-integration pulse. As the counter accounts for ∼60% of a single converter's digital power, the average digital power can be cut by more than half if one counter is shared among six or more converters.

TABLE V
RELATIONSHIP BETWEEN PRECISION, SAMPLING RATE, AND POWER IN THE THERMAL-NOISE LIMITED LOGMAP

	Analog Power	Digital Power
Precision (P)	$\propto P^2$	$\propto P$
Sampling Rate (f_s)	$\propto f_s$	$\propto f_s$

The power consumption can be further reduced by a factor of 2 if the digital supply is lowered to 2.2–2.3 V even as the analog supply is maintained at 3 V. We can also expect all digital switching capacitances to scale down at least an order of magnitude if ported from our 1.5-μm process to a submicron process. The digital power should then be negligible compared with the 1-μW analog power. Thus, our design could be modified to operate on a single microwatt of power in such processes.

IX. POWER, SPEED, AND PRECISION TRADEOFFS

The power consumption of this converter scales linearly with sampling rate, because a higher sampling rate requires an increase in both the clock frequency (digital power) and also in the bias currents I_b and $I_{\rm os}$ (analog power). For constant sampling rate, digital power scales linearly with increased precision $P\,(2^{\#\rm bits})$ because counting an extra bit at the same sampling rate means that the clock speed must double. For constant sampling rate, analog power scales *quadratically* with precision as an increase in precision under a thermal-noise regime requires a squared increase in capacitance. We have shown that this converter is thermal-noise limited. Thus, for constant analog power consumption, it is possible to reduce the capacitance by 4×, halve the precision, and obtain four times the sampling rate. These relationships are summarized in Table V.

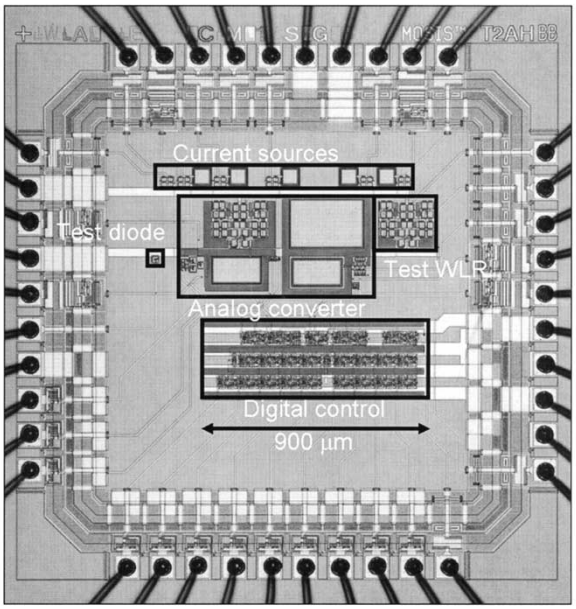

Fig. 20. Die micrograph of the logmap A/D.

X. Conclusion

The factor of $\sim 100\times$ in power savings over a DSP, robust temperature and matching performance, and an architecture suited to parallel implementation makes an analog logarithmic A/D solution very attractive for the next generation of fully implanted bionic ears or portable speech-recognition front-ends. The use of local feedback calibration as opposed to global feedback calibration yields a 2.5-bit improvement in a dual-slope converter topology at the same power consumption. Power, speed, and precision may be traded in the A/D to satisfy different performance specifications. The A/D was fabricated by MOSIS in AMI's 1.5-μm process on a 2.2 mm $\times$ 2.2 mm chip. The die micrograph is shown in Fig. 20.

Acknowledgment

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Dr. Sarpeshkar has received several awards, including the Packard Fellow Award given to outstanding young faculty, the Office of Naval Research Young Investigator Award, and the National Science Foundation Career Award.