Extended Dynamic Range From a Combined Linear-Logarithmic CMOS Image Sensor

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***Abstract*—A CMOS image sensor that can operate in both linear and logarithmic mode is described. Two sets of data are acquired and combined in the readout path to render a high dynamic range image. This is accomplished in real-time without the use of frame memory. A dynamic range in excess of 120 dB was achieved at 26 frames/s (352 × 288-array). The system addresses the problems of high fixed pattern noise (FPN), slow response time, and low signal-to-noise ratio (SNR) in logarithmic mode. FPN has been effectively reduced by single and two parameter calibration, the latter achieving FPN of 2% per decade. A novel on-chip method of deriving a reference point has been implemented. The system is fabricated in a 0.18-μm 1P4M process and achieves a pixel pitch of 5.6 μm with 7 transistors per pixel.**

***Index Terms*—CMOS images, dynamic range, image sensors, fixed pattern noise, linear-logarithmic response, pixel architecture.**

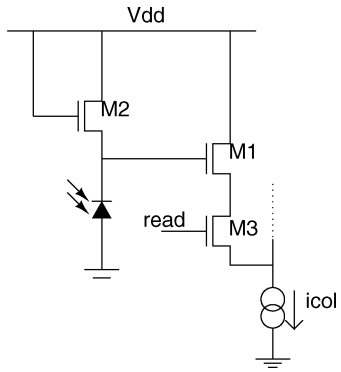

Fig. 1. Conventional 3T logarithmic APS.

I. Introduction

THE DYNAMIC range of an imaging system determines the ability to see detail in scenes with a varying illumination intensity. There are two distinct measures of dynamic range: interscene and intrascene. The first is the absolute range viewable when the viewing mechanism has time to adapt to each illumination level separately. The interscene range will be determined by the minimum and maximum exposure of a linear imaging system. The range viewable at a single setting in time is referred to as the intrascene dynamic range and will be less than the interscene range.

Many methods to extend the intrascene dynamic range have been suggested. To maintain a linear response technique includes multiple exposure systems [1], [2], predictive sampling [3], and time stamping or time to saturation systems [4]–[6]. Nonlinear techniques include well adjustment [7], [8] and logarithmic response [9]–[11].

In contrast to the majority of CMOS imagers which operate in a sampled manner, the logarithmic pixel operates continuously in time. An image sensor incorporating logarithmic pixels has the inherent ability to image scenes of a high dynamic range. A conventional three-transistor (3T) logarithmic pixel is shown in Fig. 1 and is very similar to a linear 3T pixel. It was stated in [12] that linear or logarithmic output could be achieved with simple variation of the reset signal applied to a 3T pixel. The absence of the reset signal in a logarithmic pixel prevents linear operation but should improve the optical performance since there is less metal routing across the array.

The photodiode of Fig. 1 generates a current which is supplied by diode connected device *M2*. The small photocurrent causes *M2* to operate in the subthreshold region. In the subthreshold (or weak inversion) region of operation, the gate-source voltage varies as the logarithm of the current flowing, thus providing nonlinear compression on the photosignal.

Such compression means a much wider range of illumination levels can be sensed, making it ideal for extended dynamic range applications. However, the pixel suffers from considerable disadvantages including lower signal-to-noise ratio (SNR), increased lag and increased fixed pattern noise (FPN). It is not uncommon for FPN to amount to 100% of the voltage swing per decade of illumination. In addition, the absence of a reference level prevents simple FPN correction as is done in linear integrating mode systems.

This correspondence presents a pixel architecture which generates independent linear and logarithmic responses [13]. Both responses are read from the pixel before a decision is made on which to use. If the linear result has not saturated then it will be used, otherwise the logarithmic result is output. This ordering means the logarithmic data is used for higher light levels where the SNR is maximized and the lag minimized. Other architectures to create a linear-logarithmic response [14], [15] combine the two responses within the pixel, and thus process a single set of data. Such operation means it is not possible to independently optimize the linear and logarithmic data.

Section II begins by presenting the new pixel architecture and operation. Section III describes how single and two parameter calibration of the logarithmic mode can be performed and

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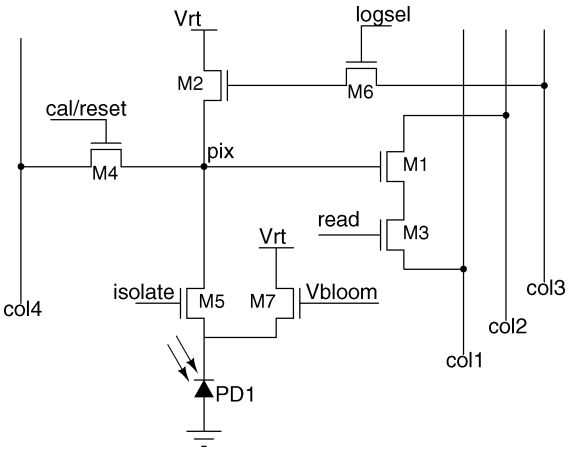

Fig. 2. Linear-logarithmic pixel.

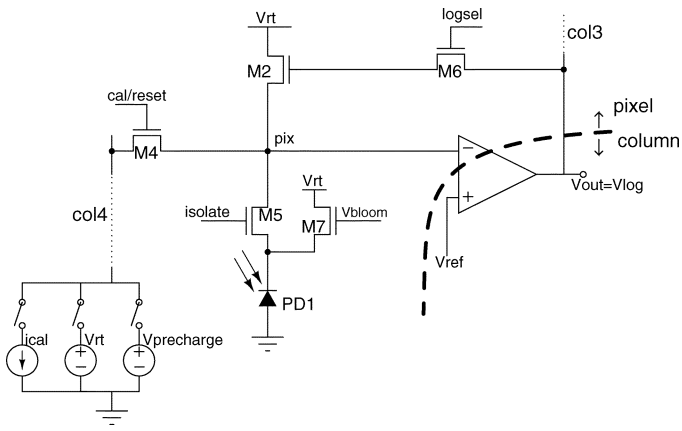

Fig. 3. Logarithmic arrangement.

Section IV details how the linear and logarithmic data is combined to create the high dynamic range image. Section VI provides a full characterization of the device. The two modes are characterized separately in addition to giving an overall performance figure to allow for comparison with other work in the field.

II. Linear-Logarithmic Pixel

The seven-transistor pixel capable of linear and logarithmic operation, is shown in Fig. 2.

The pixel is reset in linear mode by raising the control line *cal/reset* such that device *M4* is ON and *pix* is charged to the voltage of *col4* (*col4* $= V_{\rm rt}$ during the reset phase). *isolate* will also be ON, thus, the photodiode voltage will be equal to the voltage on *pix*. Simultaneously, *M6* is turned ON to precharge the gate of *M2* to 0 V. This prevents *M2* conducting current from $V_{\rm rt}$ to *pix*. The lowering of *cal/reset* starts the integration and since device *M5* remains ON, the pixel behaves like a conventional 3T configuration. After the set exposure period the pixel voltage is read out via a conventional source follower: *col2* is raised to $V_{\rm rt}$, a current source is connected to *col1*, and *read* is pulsed high.

The reference voltages $V_{\rm rt}$ and $V_{\rm bloom}$ do not vary over time and are fixed at 2.7 V and 1 V, respectively. The use of a separate supply voltage $V_{\rm rt}$, from the analog supply with which to reset the pixel, aims to reduce noise. A noise-free signal is not so important for $V_{\rm bloom}$ which is connected to the gate of *M7* in every pixel in the array to prevent blooming.

To derive a logarithmic result, the pixel is switched into the configuration shown in Fig. 3. Devices *M1* and *M3* from Fig. 2, become part of the amplifier, the remainder of which is situated in the column.

The noninverting input of the amplifier is held at a reference voltage ($V_{\rm ref}$) which is supplied by one of two on-chip DACs. This causes the node *pix* to settle to this voltage also.

$$V_{\rm pix} = V_{\rm ref} + V_{\rm offset} \tag{1}$$

where $V_{\rm offset}$ is the input offset of the amplifier and may be significant.

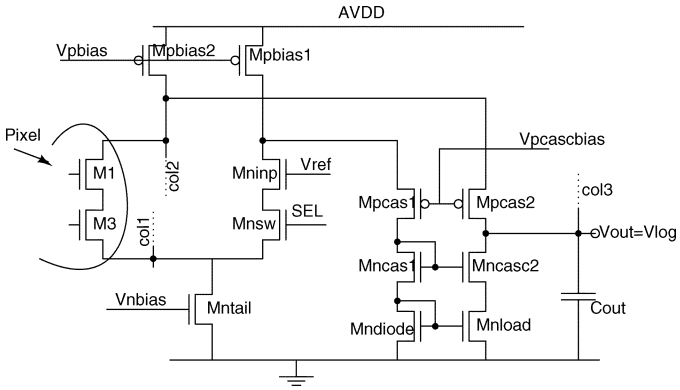

Fig. 4. Column amplifier for logarithmic operation.

A. Logarithmic Mode Stability

The topology of the amplifier used is a folded cascode as shown in Fig. 4. The main reason for the choice is the occurence of the dominant pole at the output $(1/(R_{\rm out}C_{\rm out}))$. The output of each amplifier sees the capacitive load of a column from the pixel array. The feedback from the output of the amplifier to the inverting input forms a source follower, where the current flowing in device *M2* is the photocurrent. Since the photocurrent is dependent on the incident light, the response of the source follower changes with the light intensity. The source follower has a pole at $-(gm + gmb + gds)/(C_{\rm gs2} + C_{\rm pix})$ and a zero at $-gm/C_{\rm gs}$. The pole occurs at a lower frequency because the pixel capacitance is much larger than the gate-source capacitance of *M2*.

The source follower is a common block in CMOS circuits but usually the current flowing (directly affecting the transconductance, gm) means the pole and zero are located at a frequency outwith the operation of the system. In this application, the current flowing through the source follower device is the photocurrent over which the designer does not have control. Increasing the *pix* node capacitance causes a greater phase shift because the distance between the pole and zero is increased. This is an important result as the closed-loop response is the addition of the response of the amplifier and the source follower. It is thus desirable to minimize the pixel capacitance. Any increase in noise

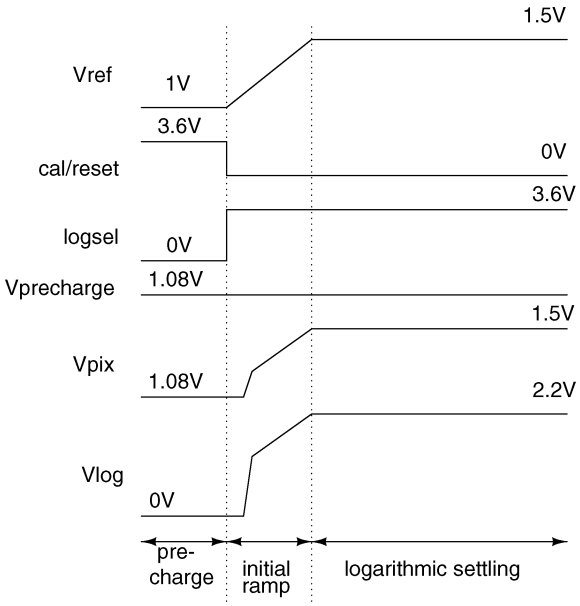

Fig. 5. Timing for reduced overshoot.

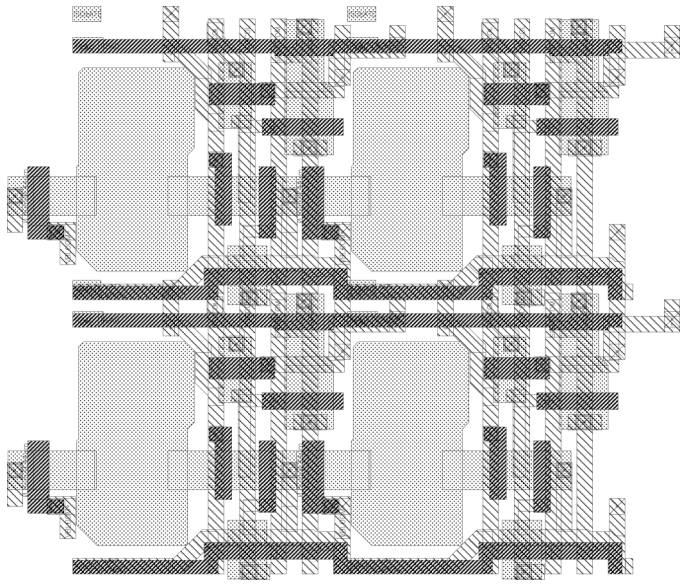

Fig. 6. 2 ×2 pixel layout.

from a reduced pixel capacitance should be filtered out by the amplifier's reduced bandwidth.

The unity-gain frequency and phase margin of the combined response are highly dependent on the photocurrent flowing which can easily vary from a few pA to tens of nA. The unity-gain frequency was simulated to vary from a few hundred kHz to over 1 MHz with the phase margin dropping as low as 20°. The low phase margin causes the amplifier to overshoot when it is first connected in the logarithmic arrangement. The next subsection discusses a method to reduce this overshoot.

B. Improved Logarithmic Settling Time

When switching the pixel into logarithmic mode, the overshoot of the amplifier can cause long settling times for low photo-currents. Due to the feedback in the pixel, the node *pix* will attempt to follow the output of the amplifier to maintain a constant gate-source voltage on *M2*. The *pix* node can charge up quickly with excess current being supplied by turning device *M2* more ON but can only discharge at a rate governed by the photocurrent. Thus, at low illumination, *pix* will increase fast then take a long time to discharge to its settling point. The switch to logarithmic mode was set to reduce the problem of overshoot as listed below and illustrated in Fig. 5.

- $V_{\rm ref}$ is set a few hundred mV below its final value.
- *logsel* is low (*M6* OFF).
- *pix* is precharged via *M4* to a voltage, such that $V_{\rm out}$ is low. The amplifier is now operating in open-loop configuration.
- *M4* is turned OFF and *M6* ON.
- $V_{\rm ref}$ ramps UP to its final value.

The ramping of $V_{\rm ref}$ serves to absorb the overshoot caused by the amplifier. As V increases, *pix* does not have to discharge to its settling point. The settling point moves up to meet $V_{\rm pix}$.

C. Layout

The pixel designed uses seven transistors and the 5.6-μm pitch (1/7 inch) is achieved by the use of a 0.18-μm process. However, the devices in the pixel are required to operate up to 3.3 V and have a minimum dimension of 0.35 μm. The area reduction achieved by using a 0.18-μm process comes from the interconnect width and spacing rules which permit a higher density of circuitry in the pixel. The pixel achieves a 33% fill factor. An n-well/p-substrate photodiode is used, providing compatibility with a conventional CMOS process with no special layers. The layout of 2 ×2 pixels is shown in Fig. 6. A layer of metal 3 was placed over as much of the circuitry as possible (excluding the photodiode) to prevent light-induced currents corrupting the logarithmic calibration.

III. Logarithmic Calibration

Logarithmic calibration usually relies on the generation of a reference point to allow differencing with the illumination dependent signal. Uniformly illuminating a sensor is a possible way of creating a reference point but requires the addition of a frame memory to store the offsets [10], [16]. On-chip methods of forcing a matched reference current to flow in each pixel eliminates the need for a frame store [17], [18]. Each time a row of pixels is addressed, the reference current can be made to flow immediately after sampling the signal. Such operation requires a fast settling time for the reference state.

If the FPN is not simply an offset error, then the simple differencing operation described will not be effective at reducing the FPN. Fig. 7 shows the response of a single pixel when an offset error is introduced (dotted line) and when offset and gain errors exist (dashed line). Two parameter calibration aims to correct for offset and gain variation and requires a minimum of two reference points in addition to the sampled signal. The second added complexity of two parameter calibration is how to apply the correction algorithm to the data.

Applying an algorithm to the three samples is likely to be simpler if performed in the digital domain. Thus, the three samples can be readout and digitized individually. The algorithm used in this work for two-parameter calibration is taken from the publication by Joseph and Collins [19]. The number of reference

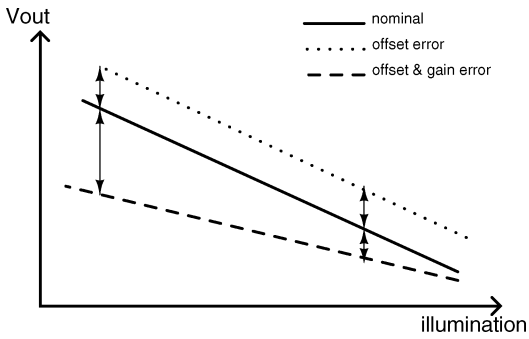

Fig. 7. Pixel responses.

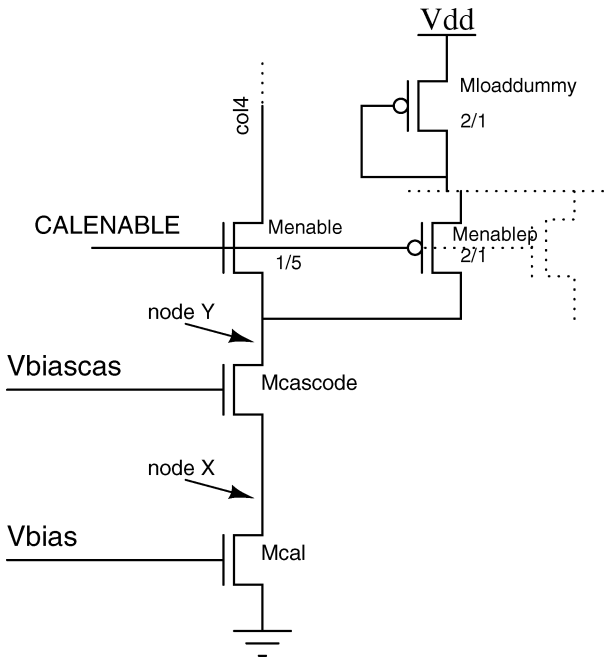

Fig. 8. Column current source for calibration.

points used was reduced to two to permit real-time operation. The algorithm aims to set all pixel responses equal to a nominal response which is found by averaging the reference points of all pixels in the array. It was found that for the correction algorithm to be effective, the two reference points were required to lie either side of the actual illumination level. This set a challenge to design a scheme capable of generating high and low reference currents for real-time operation.

The following sections detail two methods of deriving a reference current for logarithmic calibration.

A. Column Calibration

The reference generation scheme implemented on the device was a column-based cascode current mirror. The circuit is shown in Fig. 8 and is activated by turning on device *Menable*. At the same time *M4* from the pixel is turned ON and *M5* OFF. Thus, the column current source pulls current through *M2* in the pixel and sets up the appropriate gate-source voltage to be sampled.

The current source operates continuously and either steers current to the pixel or to a dummy path. This continuous operation along with the cascode output minimizes the coupling to $V_{\rm bias}$ in Fig. 8. Coupling was minimized to aid the settling time. Device *Mcal* was made long to improve matching between columns.

The reference current was designed to be programmable from 2 to 28 nA. The bias voltages $V_{\rm bias}$ and $V_{\rm biascas}$ were generated on-chip by a simple current mirror which divided down a 10-μA current. Reference currents lower than 2 nA were found to cause instability in the logarithmic configuration. This is caused by the large column capacitance which is now seen at the inverting input of the amplifier.

B. In-Pixel Calibration

A novel method of generating a matched current across the array has been devised and implemented on the test device. The scheme permits calibration currents at reduced magnitudes to be derived without the stability problems associated with the column current source approach.

A constant current can be generated if there is a constant rate of change of voltage across a constant capacitance.

$$I = C\frac{\delta V}{\delta t}. \tag{2}$$

Using (2) and knowing the capacitance, a voltage ramp can be programmed to produce a constant current. This technique can be applied to the circuit of Fig. 3 without modification. Devices *M4* and *M5* are turned OFF and the reference voltage is linearly ramped. The voltage on node *pix* will track the reference voltage, thus inducing a current due to the capacitance on *pix*. The current must be supplied by device *M2*, thus it is brought into a reference state for calibration. The capacitance seen on node *pix* will be composed of:

- drain capacitance of *M5*;
- drain capacitance of *M4*;
- gate capacitance of *M1* (inverting input of amplifier);
- source capacitance of *M2*;

and was estimated to be 2.8 fF. The ramp is generated by one of two on-chip DACs, thus to induce a reference current of 20 pA, the range of the voltage ramp would need to be 143 mV in a 20-μs time window, which is quite achievable. The output should be sampled when $V_{\rm ref}$ reaches the settling level used in normal logarithmic mode. This ensures that the source-bulk voltage of device *M2* in the pixel is the same for both samples.

IV. Linear-Logarithmic Stitching

The algorithm to be presented substitutes logarithmic data for all saturated pixels of the corresponding linear image. If valid linear and logarithmic data exist for a pixel then the linear is used due to its higher SNR. It should be noted that the substitution is always performed on over-exposed linear pixels and never on under-exposed regions.

Fig. 9 shows how a typical linear response could be aligned with a logarithmic curve to extend the dynamic range. The logarithmic curve has been appropriately shifted and a gain applied such that the slope of the logarithmic data is close to that of the linear at the stitching point. For illumination levels below the stitching point, the linear data will be output but above this level the logarithmic data will be used. The logarithmic compression

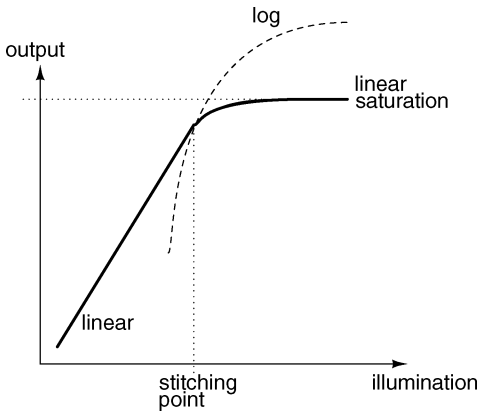

Fig. 9. Linear and logarithmic curve stitching.

on the photosignal produces a reduced voltage swing in the data compared to the linear. Without additional gain, the logarithmic data will have a low contrast compared to the linear. For a set integration, linear saturation is reached if there is sufficient illumination to discharge the pixel past the lower operating point of the source follower or outwith the input range of the column ADC. All pixels that have saturated, contain no image data and are useless. Lost information in the saturated pixels of a linear image could be restored if logarithmic data were substituted in their place.

The algorithm, first, shifts the logarithmic data to align with the linear range. The shift is calculated by comparing nonsaturated linear and logarithmic data from the same pixel. This comparison level is labeled as the *stitching point* in Fig. 9. The stitching point is chosen close to the linear saturation level to maintain as much linear data as possible to benefit from the higher SNR. Linear-logarithmic mapping is calculated in the following way.

1) Select pixel(s) which have a value nearest to the set threshold.
2) Get the logarithmic equivalent value from selected pixels (average if more than one pixel).
3) Calculate the difference between the linear and logarithmic values to create the mapping.

The mapping requires one-frame delay to calculate the offset to be applied to the logarithmic data before any substitution can occur. Once the mapping has been calculated, it can be continuously updated or refreshed after a certain time period. It must be recalculated if the linear integration time is altered, however, no frame buffer is required for the substitution.

A simple Boolean substitution is performed on the linear image to instantiate the logarithmic values. If a linear pixel has a value greater than the stitching point, then the equivalent pixel value from the logarithmic image is mapped then substituted. In this work, the substitution was performed in the FPGA as the data was read out of the chip.

V. Chip Overview

A chip micrograph of the test sensor designed is shown in Fig. 10. The CIF format pixel array is addressed by means of a

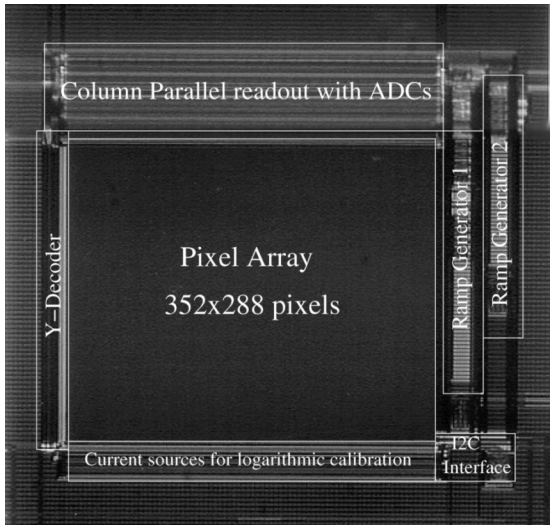

Fig. 10. Chip micrograph.

Y-decoder situated to the left of the array and, dependant on the signal sought, either the logarithmic amplifier or linear current source is connected to the pixels addressed. A column parallel sample and hold architecture is situated just below the ADC in the column. The analog-to-digital conversion of the signals is also carried out on a per-column basis, with the digital results being stored in one of two sets of SRAM banks. During the subsequent ADC cycle the previous values from SRAM are readout serially, with the X-decoder addressing each column in turn.

Matched current sources for logarithmic calibration are situated below the pixel array and provide a reference current for the addressed row of pixels. Also, shown in Fig. 10 is the analog control circuitry which includes two DACs. The first DAC is used to supply the ramp to the single slope ADC [20], and the second controls the reference voltage applied to the amplifier used in logarithmic configuration.

Fig. 11 shows the timing of events to readout linear data, followed by offset calibrated logarithmic data. Time $T1$ is the total time required to sample the linear signal and reset level from the pixel. The sampling of the linear signal and reset level is uncorrelated, thus kTC noise is not removed. The signal level is first sampled then the pixel is reset, released from reset before the second sample is taken. *sample1* and *sample2* from Fig. 11, represent the control signals of the two sample and hold capacitors situated in the column. $T1$ is partly determined by pixel's source follower current and was set to 10 μs. The ADC cycle time ($T2$) is set by the length of the ramp supplied by one of the on-chip DACs and was set to 50 μs. $T2$ also dictates the settling time for logarithmic mode. After the linear ADC conversion, the raw logarithmic value is sampled and held and the pixel next switched into one of the reference generation modes. There will be a delay of around 25 μs ($T3$) while the column current source settles or the reference voltage to the pixel is ramped and the reference value sampled onto the second capacitor. The second ADC conversion begins immediately after the logarithmic reference value is sampled. The digital output contains the difference

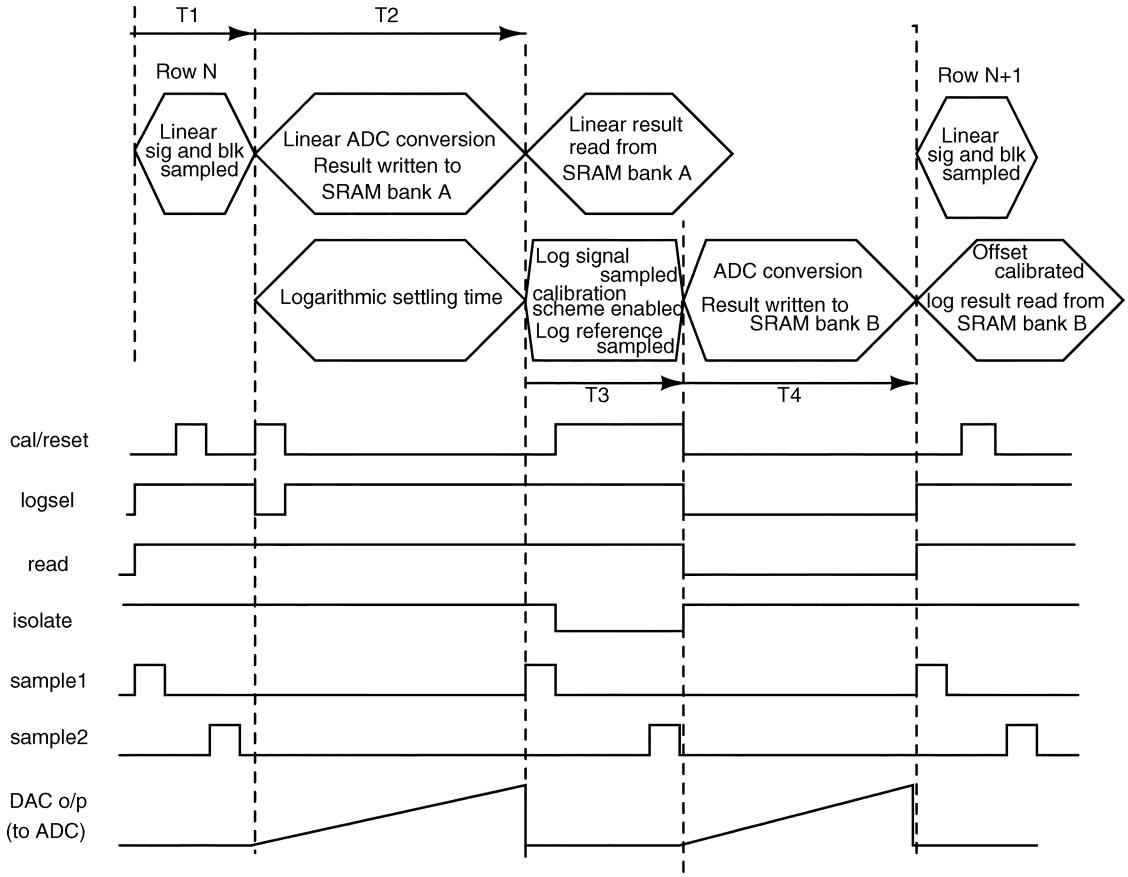

Fig. 11. Readout timing: linear data and offset calibrated logarithmic data.

between the raw logarithmic value and the reference point as required in offset calibration.

Thus, the total line time is given by

$$T1+T2+T3+T4 = 10\,\mu\text{s}+50\,\mu\text{s}+25\,\mu\text{s}+50\,\mu\text{s} = 135\,\mu\text{s}.$$

This equates to a maximum frame rate of 26 fps for an array of 288 rows.

For a higher resolution imager, the combined linear-logarithmic architecture would operate at a reduced frame rate in its current form. A reduction in the line time could be achieved by improving the ADC conversion time but the settling time of the logarithmic mode ($T2$) cannot be reduced if the dynamic range is to be maintained. Increasing the frame rate and/or maintaining it at higher image resolutions would be best achieved by improving the pixel sensitivity, increasing the photodiode area or a combination of both. This will increase the absolute photo-current for a given illumination and improve the settling response in logarithmic mode. Since the fabricated pixel is nonoptimised and uses only standard CMOS processing layers, this may indeed prove successfull. The lowest FPN is achieved when using two-parameter calibration in logarithmic mode, however, this further reduces the frame rate.

VI. Measurements

This section provides the results of measurements made on the test device. Information is provided separately for both the linear and logarithmic operating modes in addition to the combined performance. The test setup is shown in Fig. 12. The sensor is situated on a test board along with an FPGA, which provides the necessary timed signals to the sensor and is used to implement the linear-logarithmic substitution during readout. A PC controls the FPGA setup via an I^2C interface and displays a real-time image via frame-grabber software.

For measurements requiring a uniform illumination across the sensor, the arrangement shown in Fig. 13 was used. The sensor was placed at the opening of an integrating sphere.

A. Linear Mode

Using the photon transfer technique described by Janesick *et al.* in [21], the conversion factor of the test device was found to be 15.35 $\mu\text{V}/e^-$. This equates to a pixel capacitance of 10.4 fF and is slightly higher than the 8 fF predicted from the simulation models and layout at the design stage. The reason for this is thought to be the connection of two n^+ regions to the n-well photodiode. It is known that highly doped n-diffusion regions have a greater associated capacitance than lower doped n-well areas. The estimation of the total pixel capacitance used a value for the photodiode based on measurements from a photodiode structure with a single connection to highly doped n-diffusion. At the design stage, the pixel pitch was prioritized over the pixel capacitance.

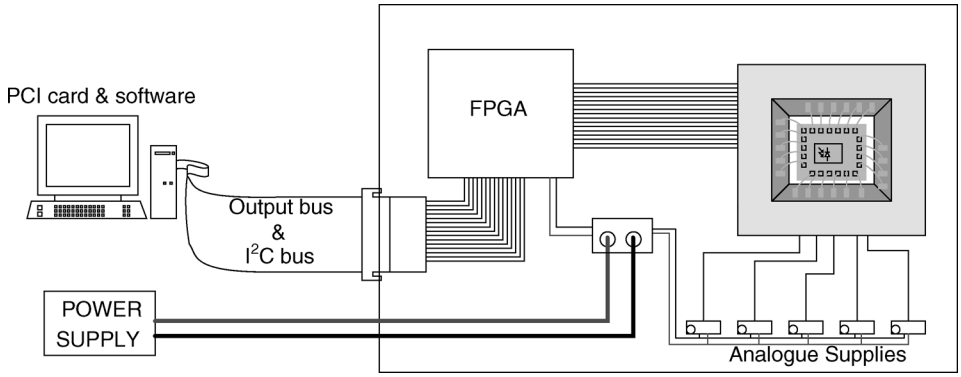

Fig. 12. Test board setup.

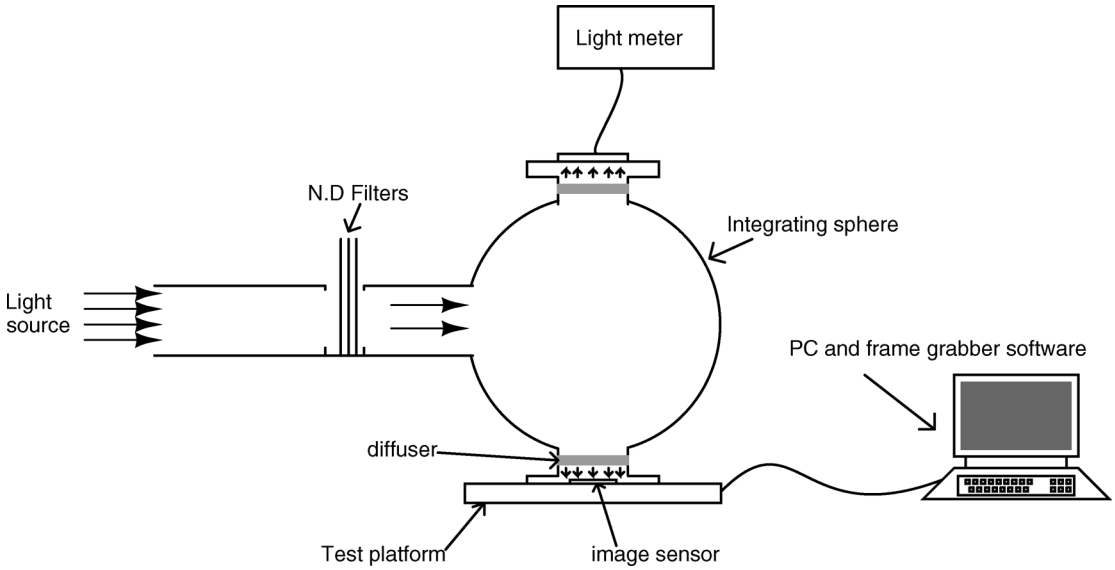

Fig. 13. Uniform illumination setup.

The SNR and dynamic range were calculated using (3) and (4):

$$\mathrm{SNR(sat)} = 20\log_{10}\left(\frac{\mathrm{Signal\_at\_saturation}}{\mathrm{Noise\_at\_saturation}}\right) \quad (3)$$

$$\mathrm{Dynamic\_Range} = 20\log_{10}\left(\frac{\mathrm{Max\_Signal}}{\mathrm{Noise\_floor}}\right). \quad (4)$$

The SNR at saturation was found to be 48.1 dB, where the saturation level of the device equated to a full well capacity of 64000 electrons. Converting the saturation point to a voltage and using (4), the dynamic range of the linear mode was found to be 58.7 dB. The temporal noise value measured and used in (4) had a standard deviation of 0.95 mV.

Using a fixed exposure in linear mode and placing various neutral-density filters (in addition to the IR filter permanently in place) between the light source and the sensor a sensitivity plot was constructed. The sensitivity was found to be 726 mV/lx·s.

To measure the dark current at room temperature a long exposure time of over 500 ms was set in addition to covering the sensor to block any incident radiation. A frame of zero exposure was subtracted to remove any offsets and FPN. A mean of 0.388 fA was measured which becomes 1.24 nA/cm^2 when related to the area of the pixel.

B. Logarithmic Mode—Sensitivity

1) Uniform Illumination: Using a Halogen light source and the setup shown in Fig. 13, the response shown in Fig. 14 was constructed. It shows the output of the sensor in logarithmic mode as a function of irradiance. The data follows a straight line because the illumination level is displayed on a logarithmic scale. This confirms the logarithmic compression as the photocurrent is converted to a voltage in each pixel. The codes plotted at each illumination level represent the mean over the whole pixel array. Below about 20 mW/m^2, the response begins to deviate from a straight line. This is due to the logarithmic mode not settling in the allocated time. The straight line could be extended to lower illumination levels by operating the device at a reduced frame rate. More information on the settling response in logarithmic mode is given later in this section.

Using the data above an irradiance level of 20 mW/m^2, the log slope was calculated to be 100 codes/decade. This equates to 80 mV/decade. This result compares favourably with Loose [18] and Kavadias' [17] work, of which the former achieved 130 mV/decade with two stacked devices (therefore, $\approx$65 mV for a

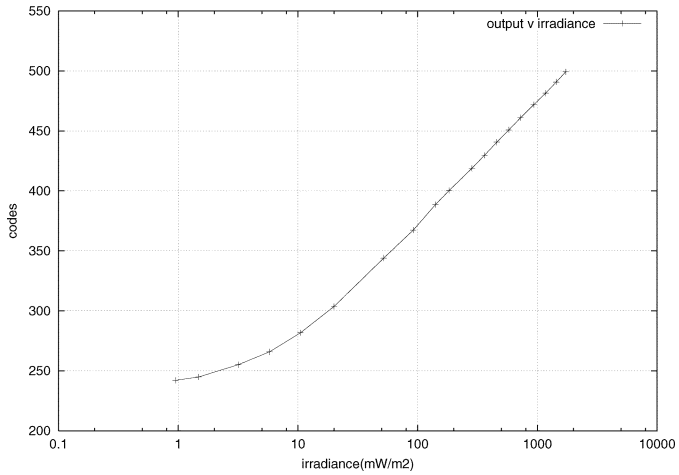

Fig. 14. Logarithmic response to irradiance.

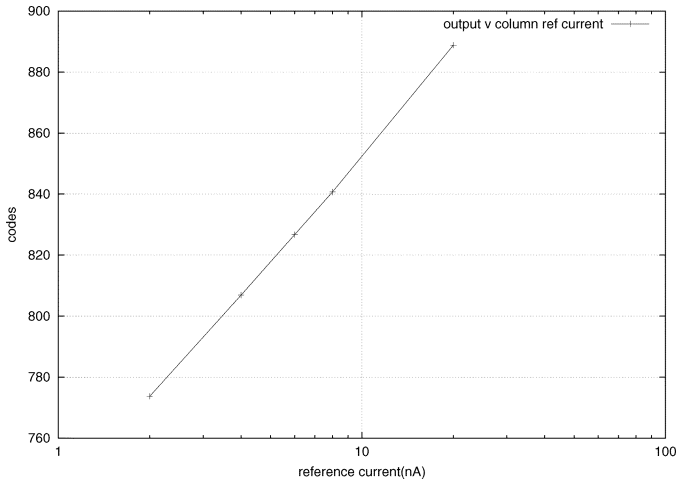

Fig. 15. Response with programmable column current source.

single device) and the latter 50 mV/decade. Huppertz *et al.* [22] reports a slightly superior 84 mV/decade which is achieved with feedback.

To calculate the raw FPN in logarithmic mode, a series of 30 frames were averaged on a per pixel basis, thus reducing the temporal noise by $\sqrt{30}$. The FPN in the averaged image was then calculated and found to have a standard deviation of 36 mV. The ratio of the raw FPN to the logarithmic response is thus 45%.

2) Column Current Sources: In this configuration the column current sources were connected to the pixel, whilst the photodiode was isolated from device *M2*. The programmable reference current was used to calculate the logarithmic response to programmed current. Fig. 15 shows the output recorded across the 1.15 decades of programmable reference current.

The response was calculated to be 100 codes/decade which matches that found when illuminating the device. It should be noted that the bias for the column current source is derived by means of an offchip voltage reference placed across a resistor. The mirroring of this master current will vary with the absolute resistor value. This is not a problem if only trying to measure the slope of the response as all currents will be scaled appropriately. Uncertainties result if the absolute current level is to be determined. A simulation at the process corners showed the column current could vary by $\pm 30\%$. This is important if trying to estimate absolute photocurrent levels.

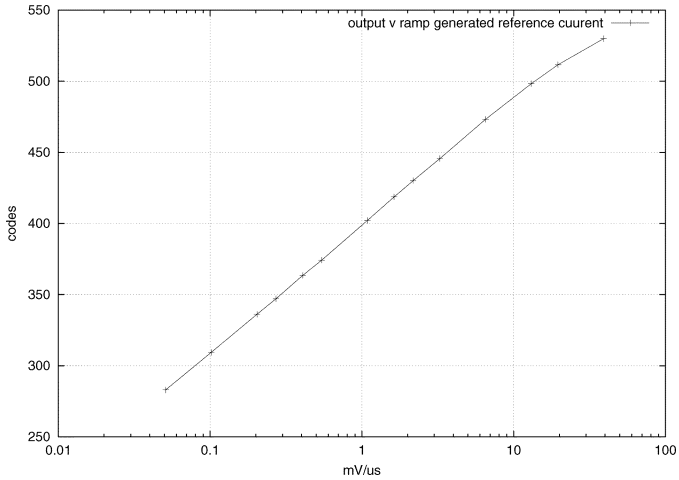

Fig. 16. Response using ramp to generate reference current.

3) Voltage Ramp: The second on-chip reference generation scheme used a novel means of generating an in-pixel current. The reference voltage applied to the amplifier of Fig. 3 was ramped, while the logarithmic compression device (*M2*) was isolated from the photodiode. It was thought that the matching across the array of the capacitance on the isolated pixel node would directly affect the matching of the reference current.

The sampled value is plotted against the time per code in Fig. 16. To enable a wider range of slopes to be programmed the clock frequency supplying the chip was also altered. From Fig. 16 a slope of 94 codes/decade was measured which corresponds to 75 mV/decade. The slope is close to that found when using a halogen light source and the column current sources.

A reference image created from the voltage ramping scheme was measured to have 45 codes FPN (St.Dev). This was the same as was measured for the logarithmic mode using uniform illumination. However, since the process variations relating to the load device and amplifier greatly exceed those expected from the current matching, it is not possible from this result alone to determine if the reference point was successfully created. The correction of uniformly illuminated images is performed in the following section and compares the reduction in FPN achievable using the on-chip reference generation schemes and uniform illumination as the reference points.

C. Logarithmic FPN After Calibration

As already mentioned, the raw FPN in logarithmic mode is measured on an image captured under uniform illumination. The calibration process aims to reduce the variation in the image and this is how its effectiveness is measured. Such a system relies on the ability to generate an illumination uniformity superior than the calibration algorithm can achieve. The next section shows this is achieved. To reduce the effect of temporal noise all results are after the average of 30 frames.

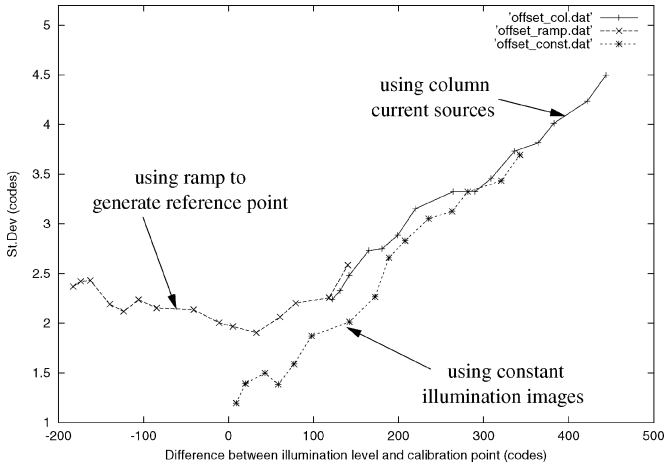

Fig. 17. Remaining FPN after offset calibration.

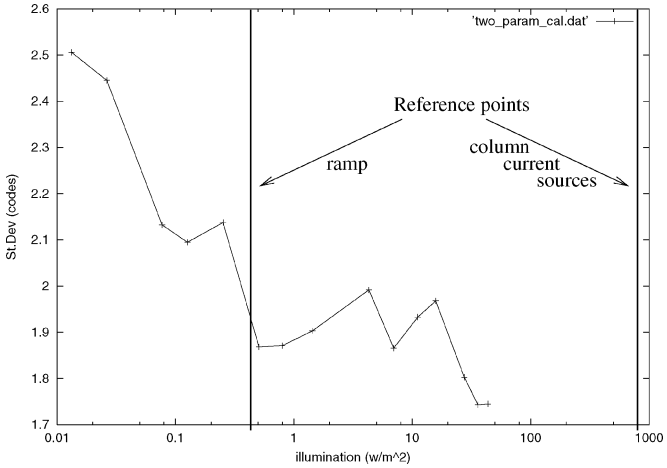

Fig. 18. Remaining FPN after two parameter calibration using column current source for the high reference point and the ramp to generate the lower.

1) Offset Calibration: Fig. 17 shows the results for offset calibration with the three different ways of generating a reference point: voltage ramp, column current sources, and uniformly illuminated images. The graph plots the standard deviation in codes against the distance between the illumination level and the reference level. Since the sensitivity of the logarithmic mode was measured to be 100 codes per decade of illuminance, the y-axis can also be read as the FPN expressed as a percentage of the sensitivity.

As expected, the FPN is minimized when the reference point is close to the illumination level (difference close to zero). The raw FPN of 45 codes has been reduced to below 3 codes if the calibration point is a maximum of 2 decades (200 codes) from the illumination level. All three cases show an increase in the remaining FPN as the distance between the reference point and the illuminance level increases. This is thought to come from variations in the subthreshold slope factor of device *M2* across the pixel array.

Using the voltage ramping scheme to create a reference point has reduced the FPN to around 2 codes when the illumination level is close to the reference point. However, the FPN can be further reduced if uniformly illuminated images were used to generate the reference point. This suggests that the matching of currents generated in each pixel by the voltage ramp is around 2%.

2) Two-Parameter Calibration: For two-parameter calibration, the raw logarithmic value and two on-chip generated reference points are read out for each pixel. The gain and offset algorithm was then applied. Fig. 18 shows the results from two-parameter calibration when the column current sources were used to generate the high reference point and the voltage ramp the lower. The results plot the standard deviation against the illumination level with the reference points marked on the plot.

The FPN has been reduced to below 2% for illuminance levels situated between the two reference points. Outside this range, the FPN increases but is still $\leq$2.5% at a decade below the lower reference point.

D. Logarithmic Mode—Response Time

The response of the logarithmic mode was investigated at various settling times in order to determine the transient performance. Fig. 19 shows a plot of the output codes against a uniform illuminance for settling times of 43, 86, 172, and 258 μs. The logarithmic dependence ends at a higher illuminance level as the settling time is decreased.

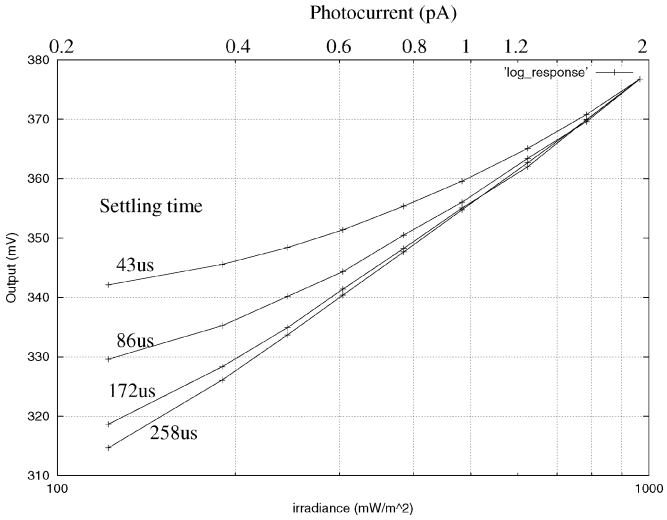

Fig. 19. Logarithmic response for varying settling times.

To estimate the photocurrent, the output measured with the column current sources enabled was used as a reference point. For a settling time of 43 μs, the logarithmic response was not apparent below about 700 mW/m^2. The difference in output between an image captured under a constant irradiance of 700 mW/m^2 and an image captured when a reference current was pulled through the logarithmic compression device was found to be 315 codes. Given the logarithmic response of 100 codes/decade, this represents 3.15 decades. Assuming the reference current was 2 nA (although this could vary by $\pm$30%), the photocurrent generated by an irradiance of 700 mW/m^2 is 1.4 pA.

700 mW/m^2 is a relatively high illumination level in relation to the photocurrent. The main reason for this is likely to be the size of the photodiode area. As the light sensing area reduces, more light is required to achieve the same photocurrent. Although the logarithmic response can extend down to lower

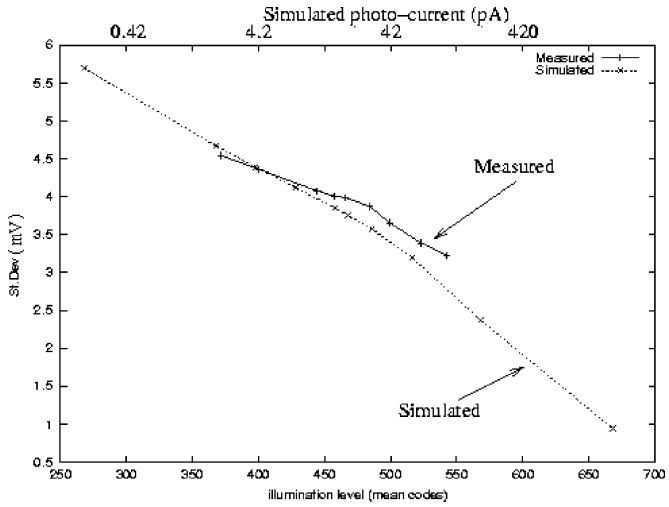

Fig. 20. Temporal noise measured and simulated in logarithmic mode.

currents, the settling time is greatly increased. Another reason for the high relative illumination level could be the density of metal in the pixel which extends up to metal 3.

E. Logarithmic Mode—Temporal Noise

To calculate the temporal noise in logarithmic mode, two images were captured under identical conditions and subtracted, then the variance of the resulting frame was divided by two to give the noise in a single frame. The sensor was exposed to a uniform illuminance from a current stabilized halogen light source to reduce the effect of lighting flicker. The plot shown in Fig. 20 was found by varying the illuminance level. The bottom x-axis gives the array average in codes (where 100 codes represents a decade of illumination) and the y-axis gives the standard deviation in mV. Recalling the results from logarithmic calibration, the FPN was reduced to 1.6 mV. From Fig. 20 it is clear the temporal noise is the limiting factor.

If photon-shot noise were dominant, the noise would be seen to increase for higher light levels. In fact, the opposite was observed. To confirm the measured results a simulation of the noise was performed. The output referred noise is also plotted in Fig. 20 and the top x-axis provides the photocurrents used. It can be seen that the simulated noise closely matches that measured.

The excessive temporal noise can be explained by examining the frequency response of the amplifier and the feedback (source follower) and remembering that the source follower's bandwidth is proportional to the photocurrent.

At frequencies within the bandwidth of the amplifier and the feedback loop, the noise generated by *M2* and by the amplifier is subject to a unity gain. However, at frequencies greater than the bandwidth (BW) of the source follower but less than the BW of the amplifier, the charging and discharging of the pixel capacitance cannot be achieved by the photocurrent alone.

In such cases, the current is supplied from the output of the amplifier via the gate-source capacitance of *M2*. The noise seen at the output is given by

$$V_{\text{onoise}} = \left(1 + \frac{C_{\text{pix}}}{C_{\text{gs}(M2)}}\right) V_N. \tag{5}$$

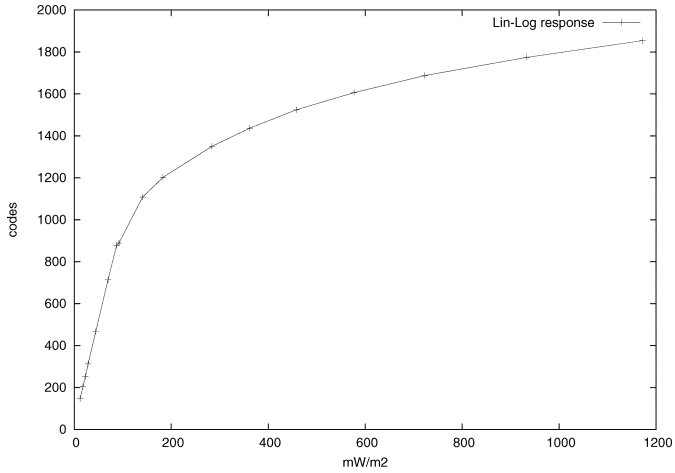

Fig. 21. Combined linear logarithmic response (log data has gain 8 applied).

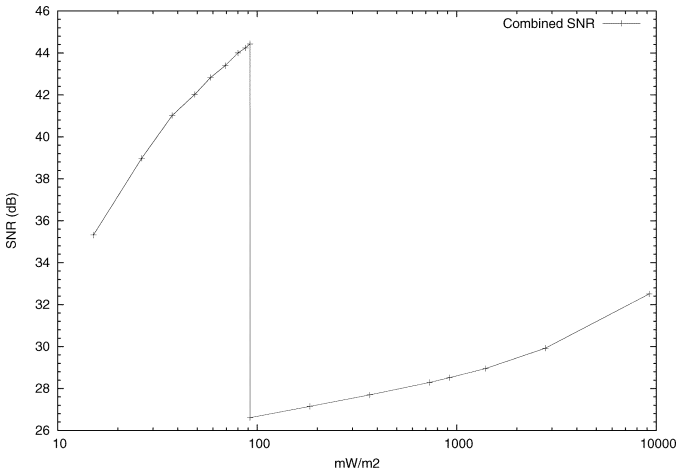

Fig. 22. Combined linear logarithmic SNR.

It can be seen the noise is amplified by the ratio of the pixel capacitance (C_{pix}) to the gate-source overlap capacitance ($C_{\text{gs}(M2)}$). At frequencies greater than the bandwidth of the amplifier the input referred noise is blocked.

Simulations have shown that by increasing the size of device *M2* to 3/1.5 and device *M1* to 2/1, the temporal noise can be reduced to a level comparable to the level of FPN after calibration. This would increase the pixel size.

F. Combined Response

The combined response of the sensor is shown in Fig. 21 and the stitching point occurs at an illumination level of 92 mW/m^2. The stitching of the data shows a good continuity between the linear and logarithmic regions.

Fig. 22 plots the combined SNR against the illumination level. The stitching point again occurs at an illumination level of 92 mW/m^2. Below the stitching point, the linear SNR increases with illumination as is expected due to the nature of photon shot noise. The SNR in linear mode does not quite reach the maximum SNR found for the linear mode since the stitching point is prior to linear saturation level. A large drop in SNR occurs above the stitching point, where the logarithmic data is output. The SNR in logarithmic mode increases with

Fig. 23. Top: Linear image (including CDS breakdown). Bottom: Combined linear logarithmic image.

ilumination level due to the characteristics of temporal noise as shown in Fig. 20.

The dynamic range in logarithmic mode increases as the settling time is extended. It is thus necessary to define the dynamic range in relation to the operating frequency. The maximum signal was taken to be 28 nA, which was the highest programmable current during column calibration. The lowest signal was taken to be 1.4 pA which is the photocurrent that permitted settling in less than 60 μs (including initial voltage ramp) and was found from Fig. 19. These measurements give a logarithmic dynamic range of 4.25 decades. Combining this with the dynamic range of the linear mode gives a maximum overall dynamic range of 143 dB. Since the stitching algorithm requires unsaturated linear and logarithmic samples, the usable range will be slightly less than this. Table I provides a full list of sensor measurements.

G. Images

The top part of Fig. 23 shows a linear image captured with the test device. The illuminated desk lamp creates a high dynamic range scene in which detail of the left and right portions cannot be seen at the same time with the linear mode. The exposure has been set to image the detail in the darker left portion of the scene. The center of the desk lamp, which should be the brightest part of the scene, actually appears darkened. This is due to the excessive illumination causing the double sampling scheme to breakdown and would need to be prevented in any future work.

The bottom part of Fig. 23 shows the same scene when saturated linear data is replaced with logarithmic data. The left side appears darker due to the increased illumination range being displayed. The original linear data of the left side is unaltered.

TABLE I
SENSOR MEASUREMENTS

Technology	0.18μm, 1P4M CMOS
Analog Supplies	2.7V, 3.3V, 3.6V
Digital Supply	1.8V
Analog Power	61mW (linear mode), 84mW (logarithmic mode)
Digital Power	5.3mW (both modes) (chip only. Not incl. FPGA)
Image Format	352x288
Pixel Size	5.6μm x 5.6μm
Fill Factor	33%
Linear sensitivity	726mV/lux.s
Dark Current at room temp	1.2nA/cm^2
Logarithmic Response	77mV per decade of illuminance
Raw FPN in Logarithmic Mode	45% of logarithmic response
FPN after Offset calibration	<4% of logarithmic response (up to 4 decades from operating point and temporal noise reduced)
FPN after 2 parameter calibration	2% of logarithmic response (when ref points lie either side of cal point)
Temporal Noise	Up to 5.5% of logarithmic response
Linear Dynamic Range	58 dB
Logarithmic Dynamic Range	85 dB
Combined Dynamic Range	Up to 143 dB

VII. CONCLUSION

We have demonstrated that it is possible to obtain high-dynamic-range images from the real-time combination of linear and logarithmic responses. This has been achieved with low FPN and without the use of a frame memory. Temporal noise was found to limit image quality in logarithmic mode, however, the mechanism is now well understood and could be reduced to the level of FPN in future work.

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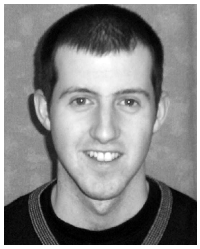

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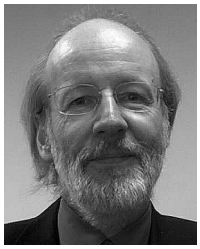

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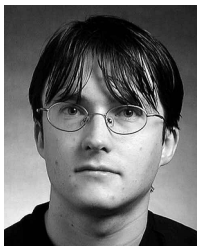

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