A CMOS Digitally Controlled, Low Power, Variable Gain Headphone Amplifier

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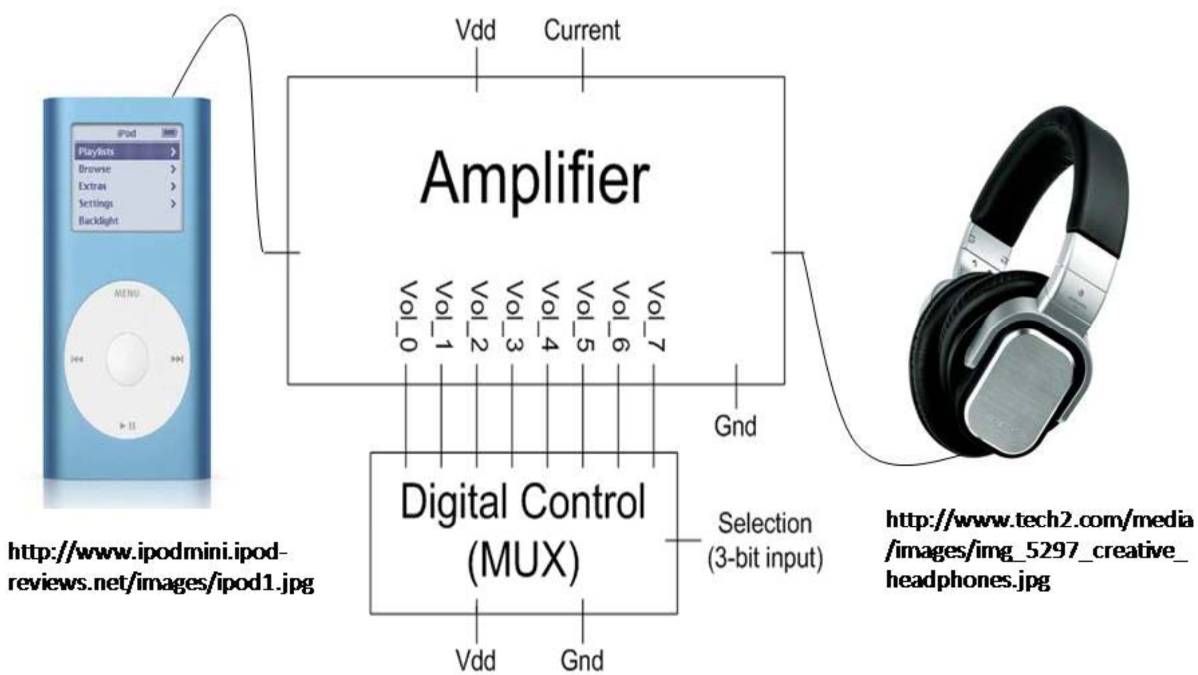
Introduction

- Application
- Goals
- Topology
- Simulation Results
- Conclusion

General Use

- Amplify the signal output by a small music device
- Connect between device and a set of headphones
- Adjustable volume control

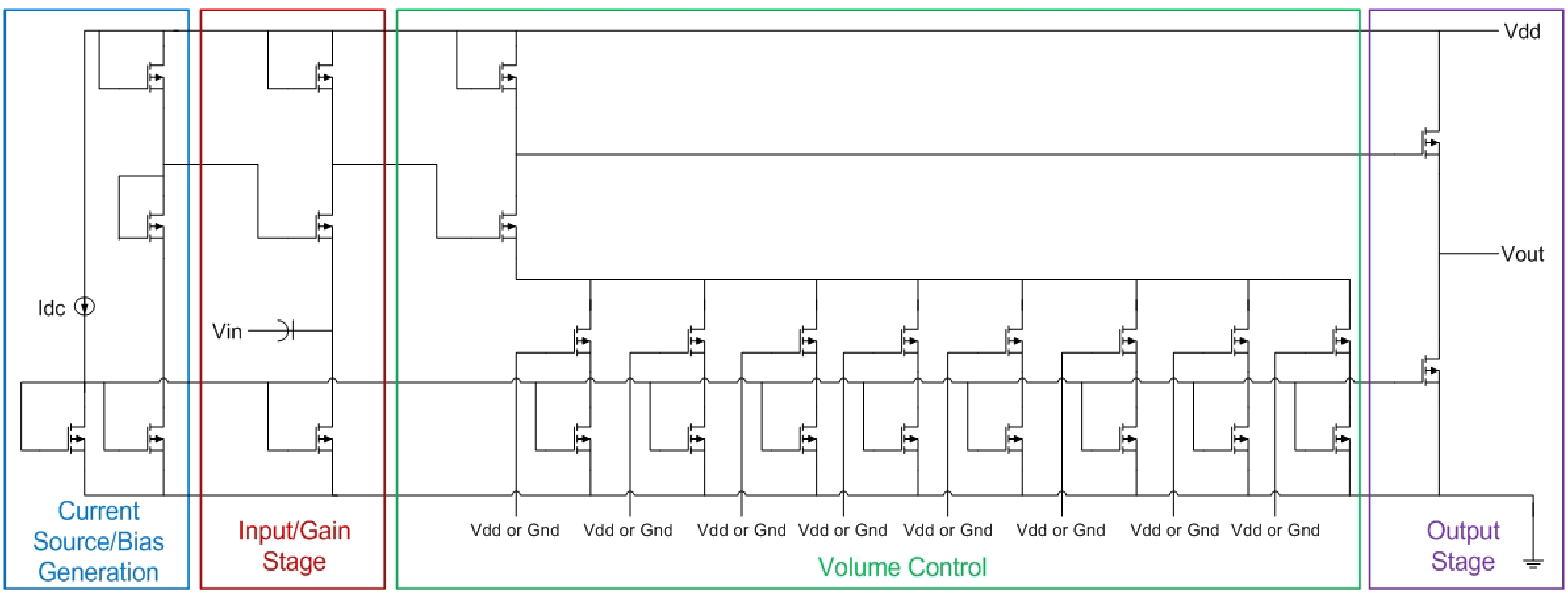


Project Goals

- Variable gain – 0dB to 20dB
- Low total power consumption
- Matched input / output impedance
- Bandwidth typical for audio applications
- Maximum input signal = 50 mV
- Total harmonic distortion < 1%

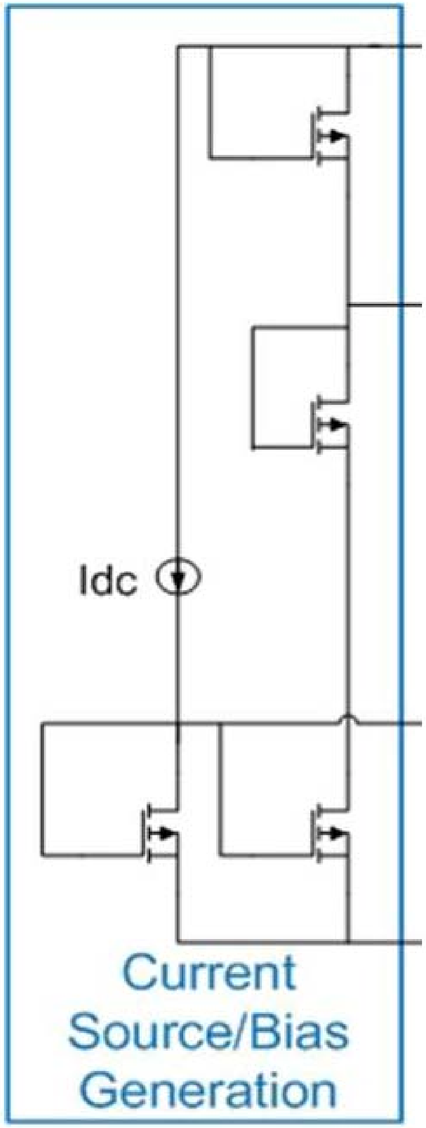
Topology

- Current generation stage
- Input stage
- Variable gain stage
- Output stage



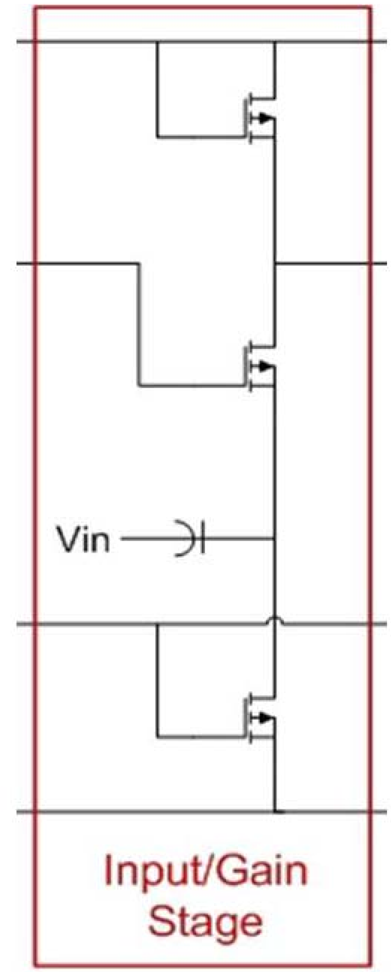
Current Source / Bias Generation Stage

- Supplies current to each stage
- Supplies desired voltage bias
- Supplies gate voltages
- Keeps transistors in saturation
- Headroom considerations



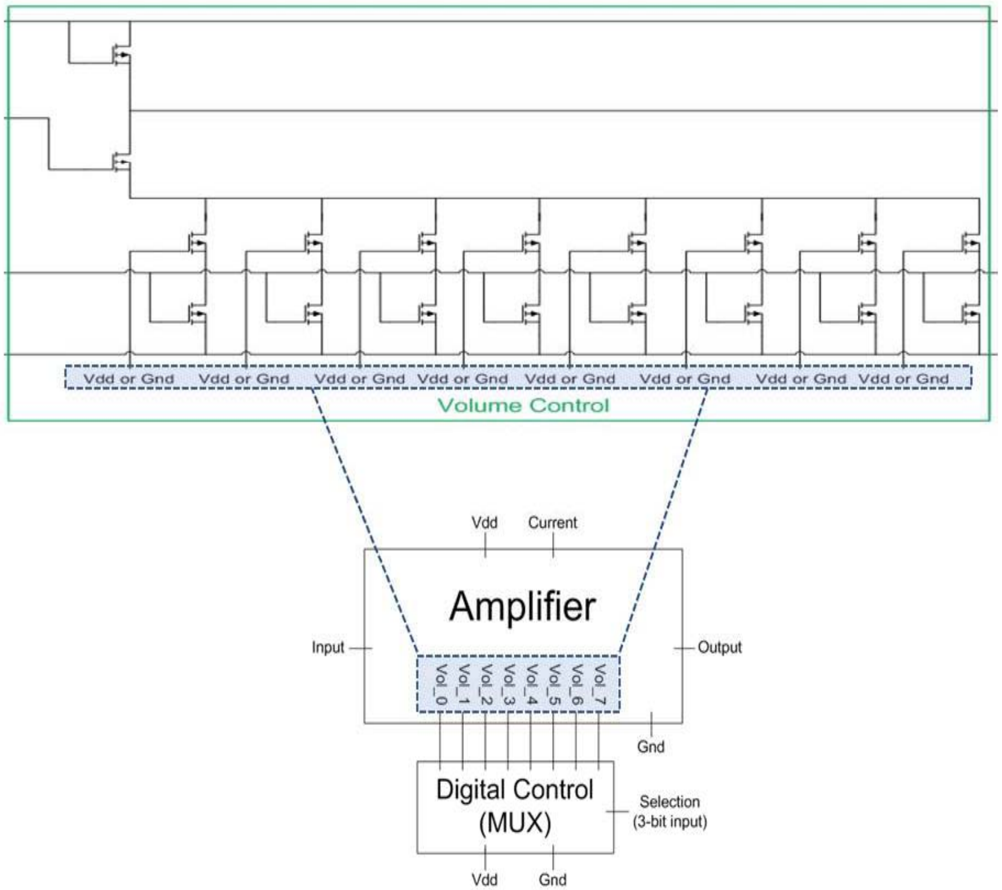
The Input Stage

- Common gate with degeneration topology
- Sets input impedance
  - Typical headphone impedance: 75-150 Ohms
- Generates Gain (~23dB)
- Rin = 1/gm1
- Gain = (gm1 + gmb1) / gm2



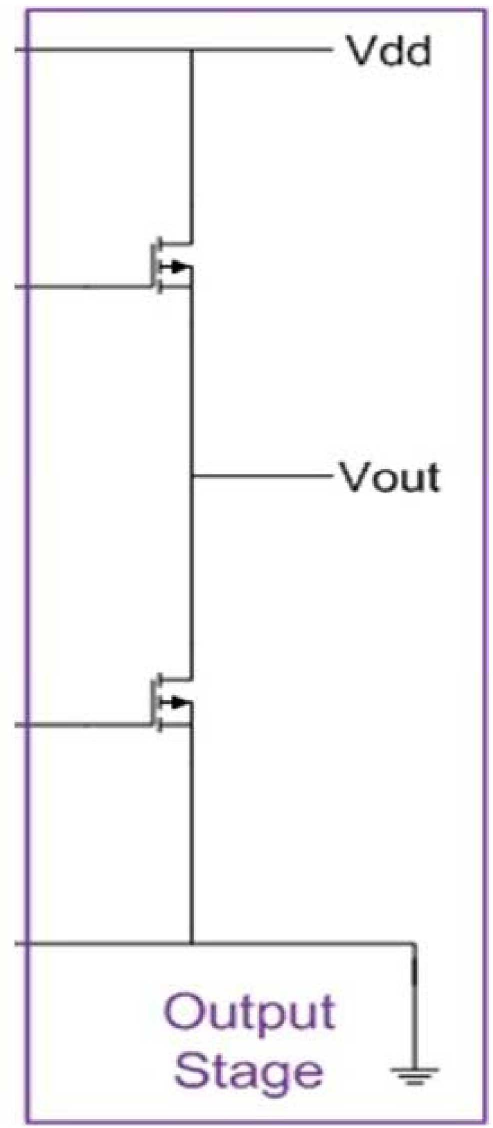
Volume Control Stage

- Allows the overall gain to be adjusted from 0dB to 20dB
- Gain is changed by switching the amount of current driven through the stage
- The switching is done by a digital control
- Common source with degeneration topology
- Gain = -gm*Rd/(1+gm*Rs)



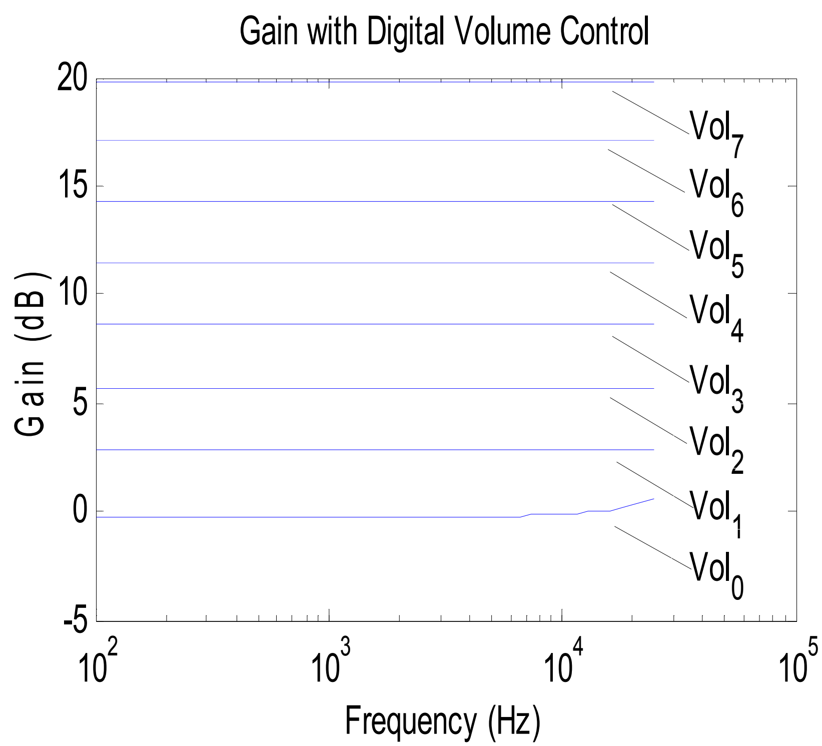
The Output Stage

- Source follower topology
- A buffer stage
- Used to set the output impedance
  - Typical headphone impedance: 75-150 Ohms
- Rout = 1/gm
- Gain = gm/ (gm+gmb)
  - Approximately –3dB
- Input stage compensates for drop in gain

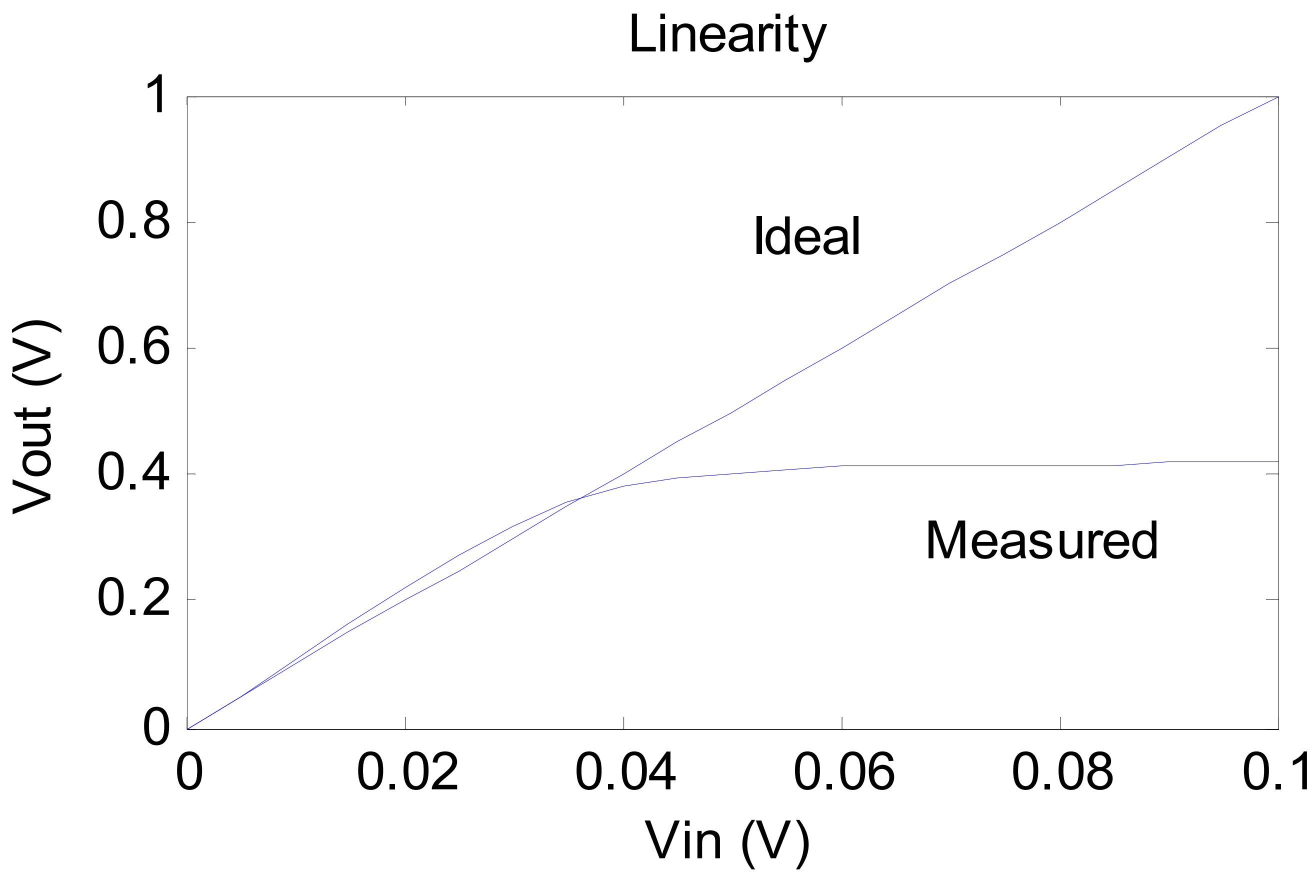


Simulation Results
Gain for each Volume Level

3-Bit Volume Control Level	Gain (dB)
0	-0.271 to 0.513
1	2.85
2	5.71
3	8.57
4	11.42
5	14.28
6	17.14
7	19.78



Simulation Results
Linearity



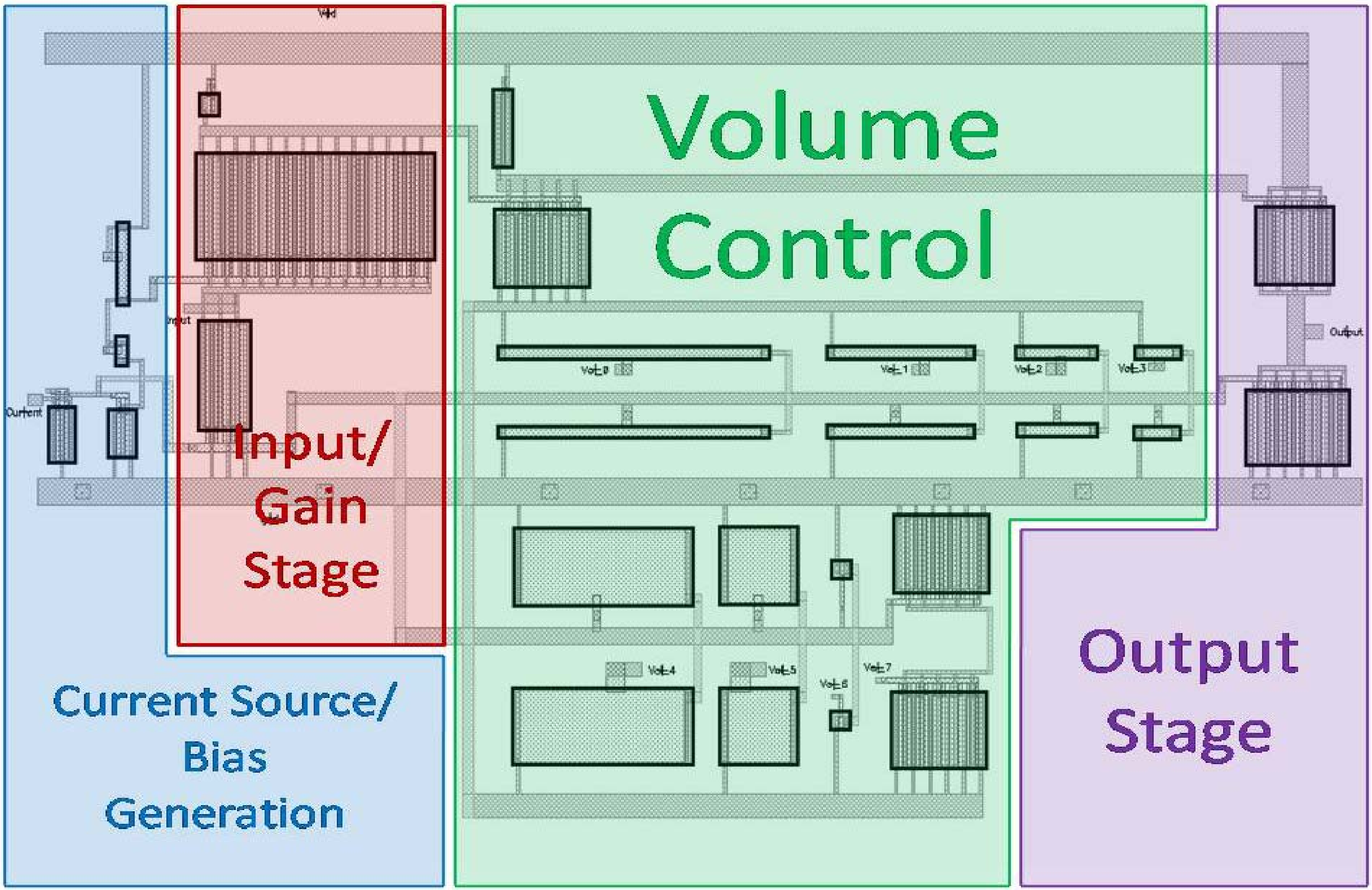
Simulation Results

Parameter	Specification	Design
Power Supply	2.5 V	2.5 V
Current Supply	100 uA	100 uA
Max Gain	20 dB	19.78 dB
Min Gain	0 dB	-0.2711 to 0.513 dB
Input Impedance	100 Ω	98.38 Ω
Output Impedance	100 Ω	100.3 Ω
Frequency Range	100 Hz to 23 KHz	100 Hz to 23 KHz
Power Consumption	< 6 mW	3.77 mW
Max Input Signal	50 mV	40 mV (for linearity)
THD	< 1% (at max gain)	0.7537% (1mV input)

Simulation Results Process Corners

Parameter	Process Corners Variation				
	TT	FF_0˚C	FF_75˚C	SS_0˚C	SS_75˚C
Gain (at max volume)	19.78dB	21.73dB	19.02dB	19.5dB	2.568dB
Input Impedance	98.38 Ω	80.46 Ω	113.4 Ω	89.85 Ω	500.1 Ω
Output Impedance	100.3 Ω	86.85 Ω	107.3 Ω	96.69 Ω	119.7 Ω
Power Consumption	3.77mW	3.851mW	3.798mW	3.724mW	3.66mW

Simulation Results
DRC and LVS Clean



Conclusion

- The circuit simulations match our goals
- Only the maximum input signal was affected by linearity
- We based our design on the specifications of other common headphone amplifiers