A Variable Gain Amplifier for UWB Systems

EECS 413 Final Project Presentation
Advisor: Prof. David Wentzloff

Ting Chang
Hsin-Han Huang
Abhishek Mitra
Motivation

Block diagram of a UWB transmitter and receiver:

Design an amplifier with:
- Variable gain range > 30dB
- Bandwidth > 528MHz
- Gains controlled by a digital counterpart
- Common-mode feedback
- A stable biasing circuit
Block Diagram of proposed VGA
Variable Gain Amplifier (VGA)

- M1-M4: cross-connected
- M5-M6: diode-connected
- M7-M8: PMOS current source

Gain depends on the ratios of $gm$

$$A_V = \sqrt{\frac{(W/L)_{1,2,3,4}}{(W/L)_{5,6}}} \sqrt{\frac{2}{I_1 + I_2}} \left(\sqrt{I_1} - \sqrt{I_2}\right)$$

- Tradeoffs: gain, bandwidth, headroom, power
VGA - PMOS Current Source Load

\[ \text{Gain} \propto \frac{1}{g_{m6}} \]

\[ g_{m6} \propto \sqrt{I_6} \]

\[ I_6 = I_{\text{total}} - I_8 \]

M8 removes 75% of the total current

Issues: value of I6 & size of M8

Gain doubles
Common-Mode Feedback (CMFB)

Keeps output DC voltage level at constant in order to drive the following stage properly.

- CM level sensing using PMOS’s operating in deep triode region as large resistors
- Working together with a capacitor, AC signals can be removed
Digital Control Circuit: 2 choices

- Choice 1: Convert from control inputs to analog control voltage using R-2R ladder

- Choice 2: Use binary weighted currents to control the gain

OUR CHOICE!!
Digital Control Circuit: Requirements

- Single Stack in Current Path to increase headroom
- Makes use of a subtraction topology
- Base currents are setup at the tail of the Gilbert Cell
- Current Mirrors are set up from the constant gm Biasing Circuit and CMFB
Digital Control Circuit: Working

I1+5uA

--- Mirrored Current

→ Current Path
Digital Control Circuit: Performance

- Linear dependence of Gain on Differential current
- Moderate power consumption
Post Amplifier

Linearity?

\[ G_m = \frac{g_m}{1 + g_m R_s} \approx \frac{1}{R_s} \]

Headroom?
Post Amplifier

\[ G_m = \frac{g_m}{1 + g_m R_s \parallel \left( \frac{1}{sC} \right)} = g_m \frac{1 + sR_s C}{1 + g_m R_s} \]
Constant-Gm Biasing

\[ V_{SG3} = V_{SG4} + I_2 R_S \]

\[ \sqrt{\frac{2I_1}{k'_{p}(W/L)_p}} + V_{th} = \sqrt{\frac{2I_2}{k'_{p}K(W/L)_p}} + V_{th} + I_2 R_S \]

\[ I_2 = \frac{2}{\mu_P C_{OX}(W/L)_N} \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2 \]
Simulation Results
Simulation Results

Power (mW) in different conditions:
- TT: 8 mW
- SS_0C: 8 mW
- SS_75C: 10 mW
- FF_0C: 4 mW
- FF_75C: 12 mW
Conclusions

• A Gilbert Cell with gain proportional to $\Delta \sqrt{I}$
• PMOS current source loads doubles the gain
• Step currents set by a Digital Control circuit
• CMFB stabilizes output DC voltage level
• A 6-dB Post-Amp with inductive peaking
• A design of constant-gm biasing circuit
<table>
<thead>
<tr>
<th>Extraction</th>
<th>TT</th>
<th>SS_0C</th>
<th>SS_75C</th>
<th>FF_0C</th>
<th>FF_75C</th>
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<tbody>
<tr>
<td>Max Gain (dB)</td>
<td>25.38</td>
<td>25.76</td>
<td>25.42</td>
<td>24.49</td>
<td>24.97</td>
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<tr>
<td>Max Gain (V/V)</td>
<td>18.568</td>
<td>19.412</td>
<td>18.654</td>
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<td>Min Gain (dB)</td>
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<td>Min Gain (V/V)</td>
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<td>Bandwidth (MHz)</td>
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<td>635</td>
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<td>Power (mW)</td>
<td>9.101</td>
<td>8.950</td>
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<td>7.048</td>
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<tr>
<th>Schematics</th>
<th>TT</th>
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<th>SS_75C</th>
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Thank You!

Questions?
References


