A Variable Gain Amplifier for UWB Systems

EECS 413 Final Project Presentation

Advisor: Prof. David Wentzloff

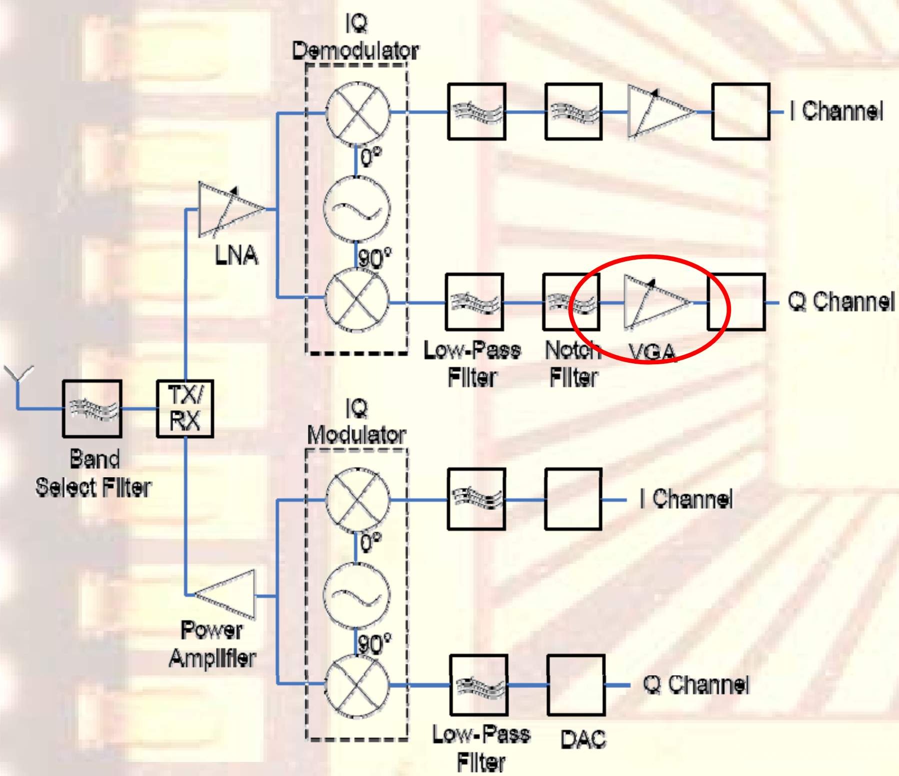
Ting Chang

Hsin-Han Huang

Abhishek Mitra

Motivation

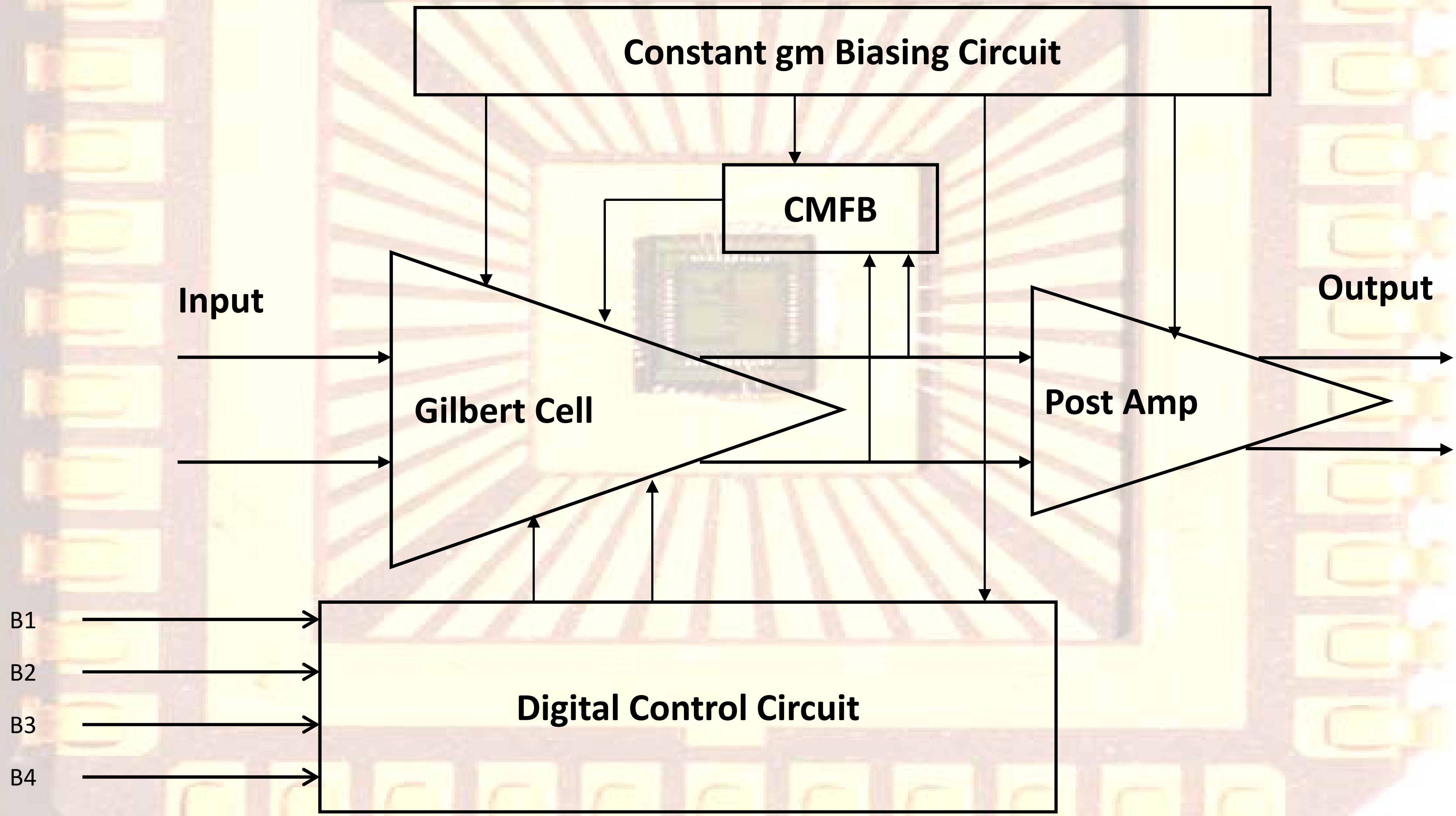
Block diagram of a UWB transmitter and receiver:



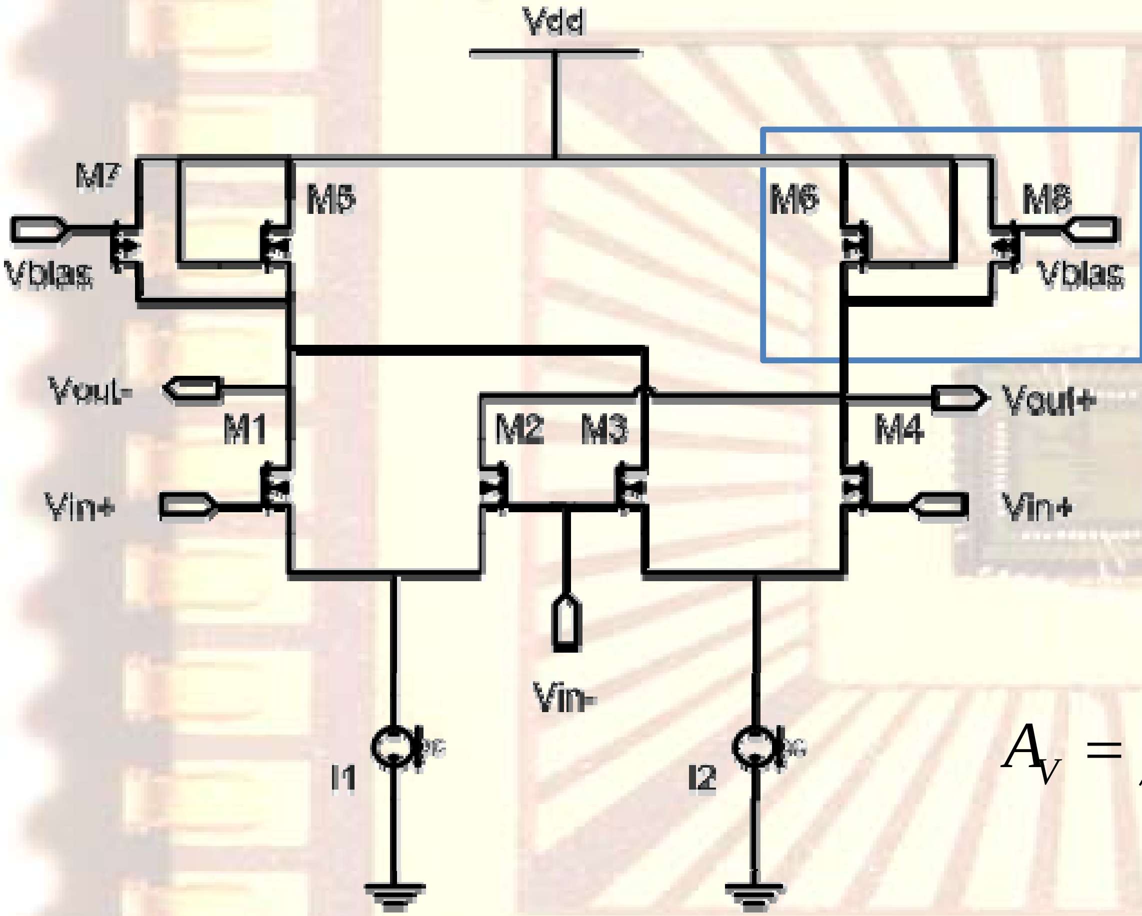
Design an amplifier with:

- Variable gain range > 30dB
- Bandwidth > 528MHz
- Gains controlled by a digital counterpart
- Common-mode feedback
- A stable biasing circuit

Block Diagram of proposed VGA



Variable Gain Amplifier (VGA)



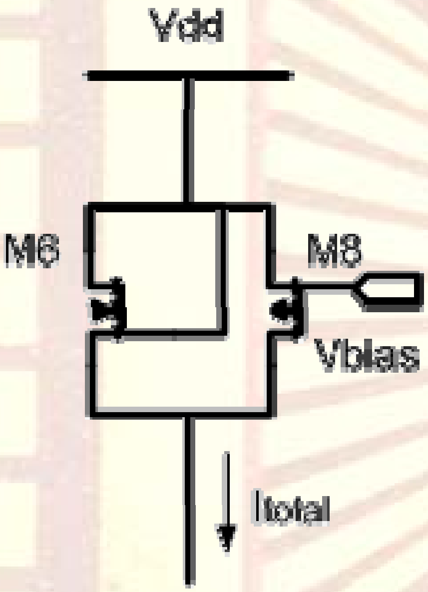
- **Gilbert Cell**
  - M1-M4: cross-connected
  - M5-M6: diode-connected
  - M7-M8: PMOS current source

Gain depends on the ratios of gm

$$A_V = \sqrt{\frac{(W/L)_{1,2,3,4}}{(W/L)_{5,6}}}\sqrt{\frac{2}{I_1+I_2}}\left(\sqrt{I_1}-\sqrt{I_2}\right)$$

- Tradeoffs: gain, bandwidth, headroom, power

VGA - PMOS Current Source Load



$$Gain \propto 1/gm_6$$

$$gm_6 \propto \sqrt{I_6}$$

$$I_6 = I_{total} - I_8$$

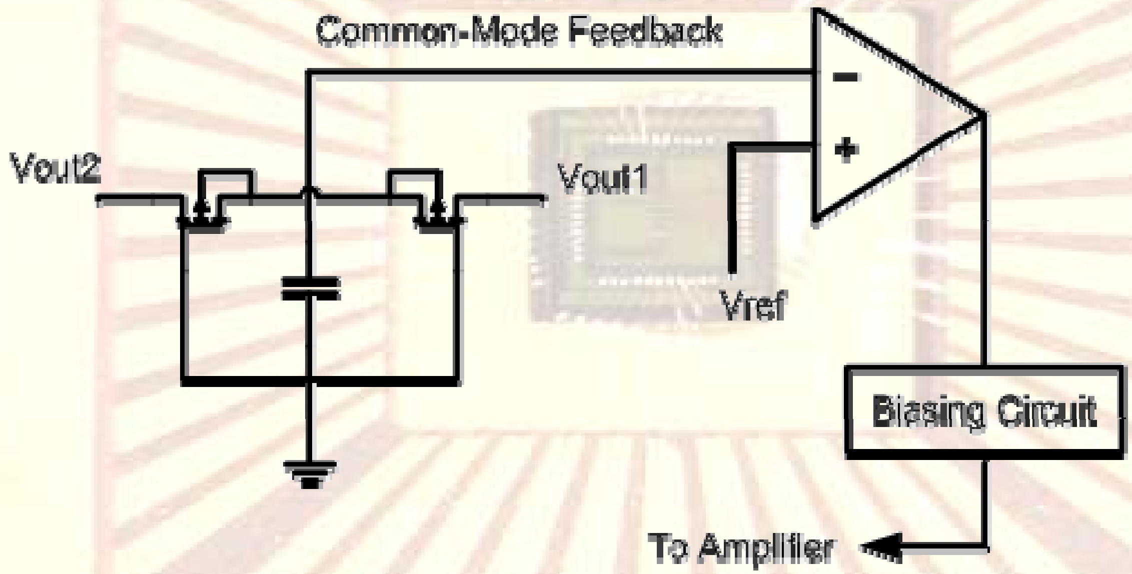
M8 removes 75% of the total current

→ **Gain doubles**

Issues: value of I6 & size of M8

Common-Mode Feedback (CMFB)

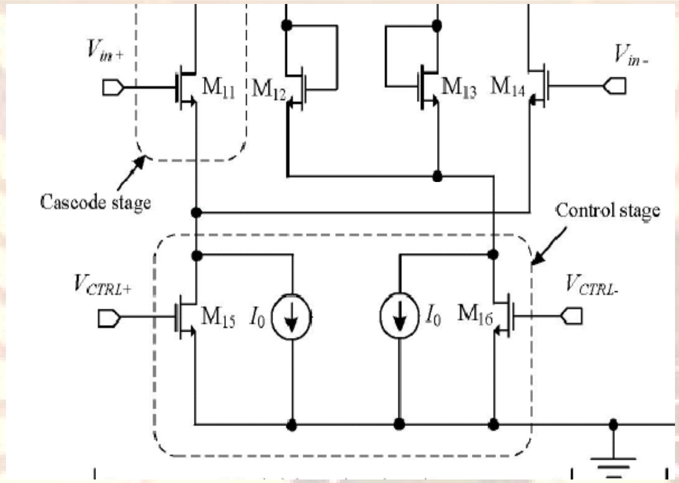
Keeps output DC voltage level at constant in order to drive the following stage properly

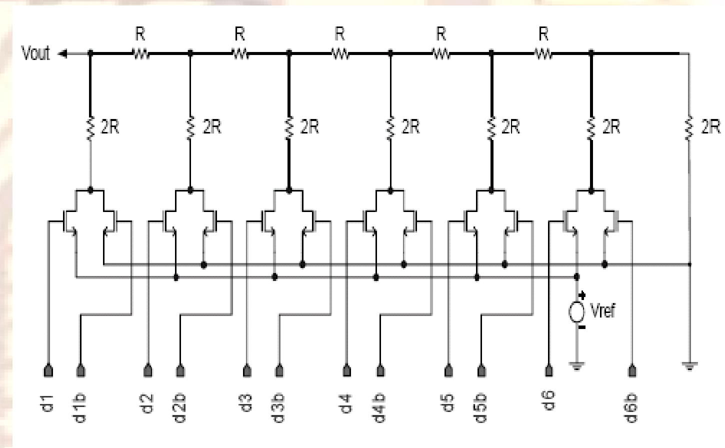


- CM level sensing using PMOS's operating in deep triode region as large resistors
- Working together with a capacitor, AC signals can be removed

Digital Control Circuit: 2 choices

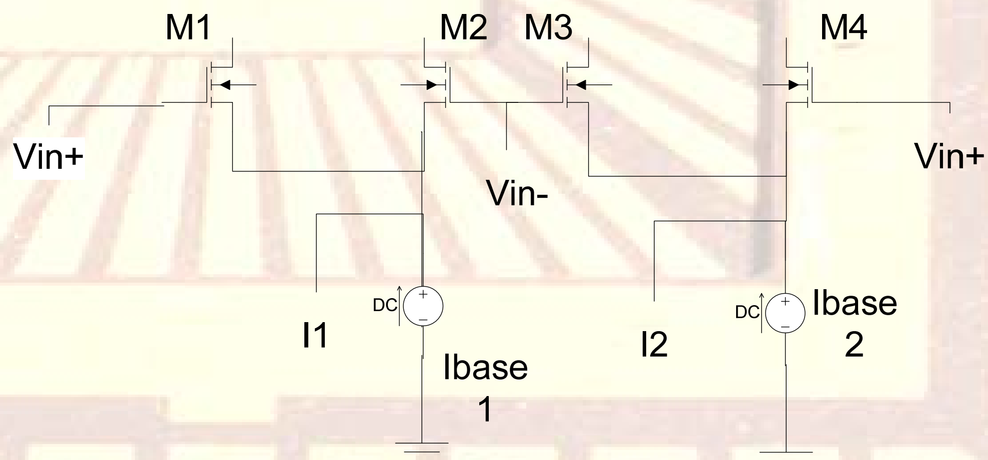
- Choice 1: Convert from control inputs to analog control voltage using R-2R ladder





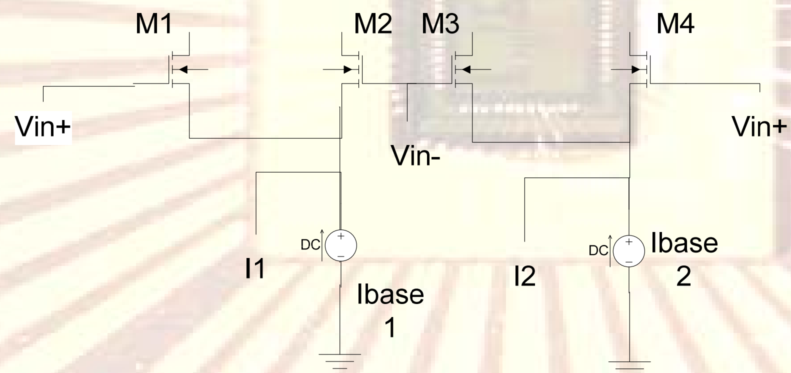
- Choice 2: Use binary weighted currents to control the gain

OUR CHOICE !!



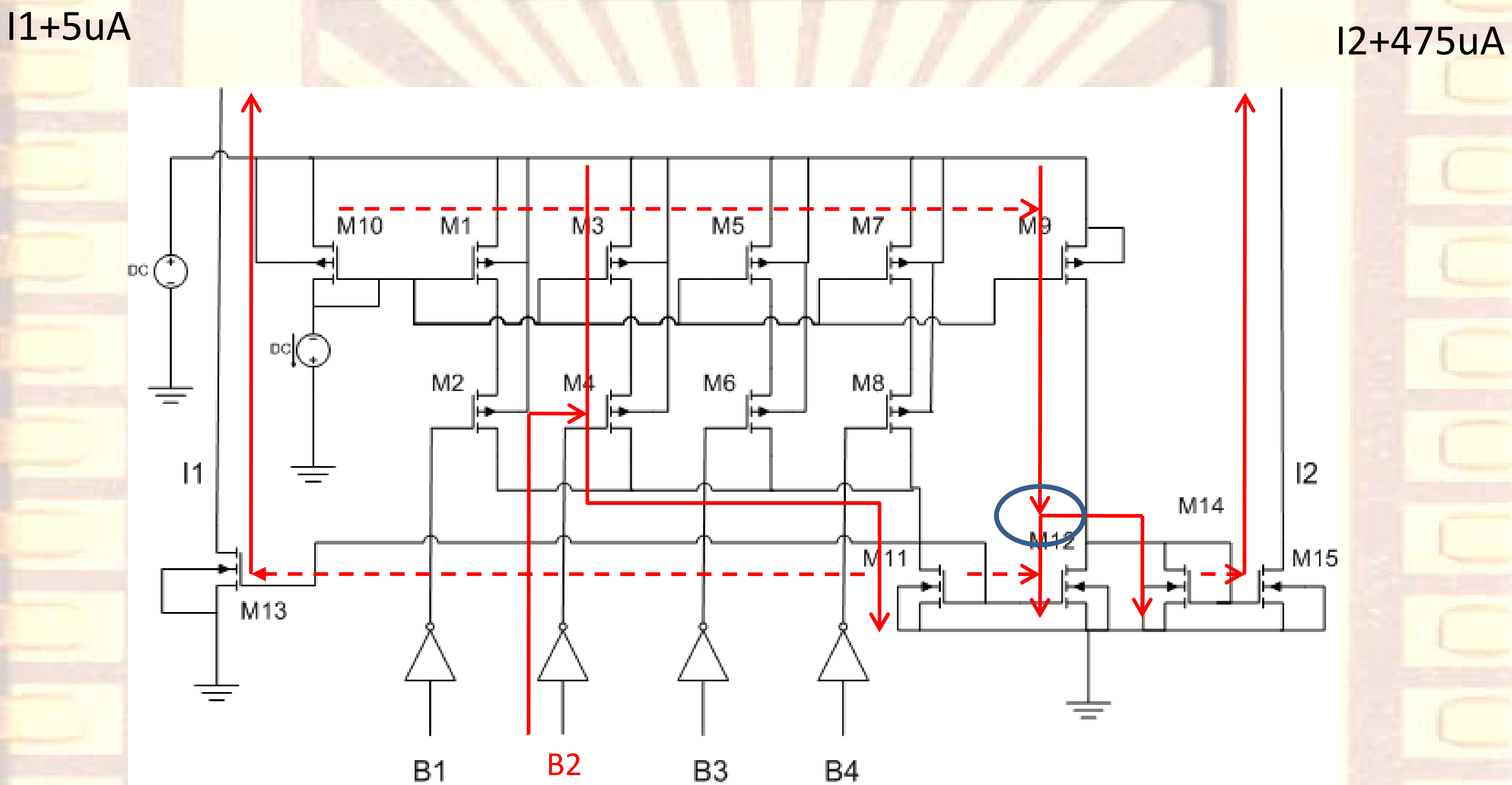
Digital Control Circuit: Requirements

- Single Stack in Current Path to increase headroom
- Makes use of a subtraction topology
- Base currents are setup at the tail of the Gilbert Cell



- Current Mirrors are set up from the constant gm Biasing Circuit and CMFB

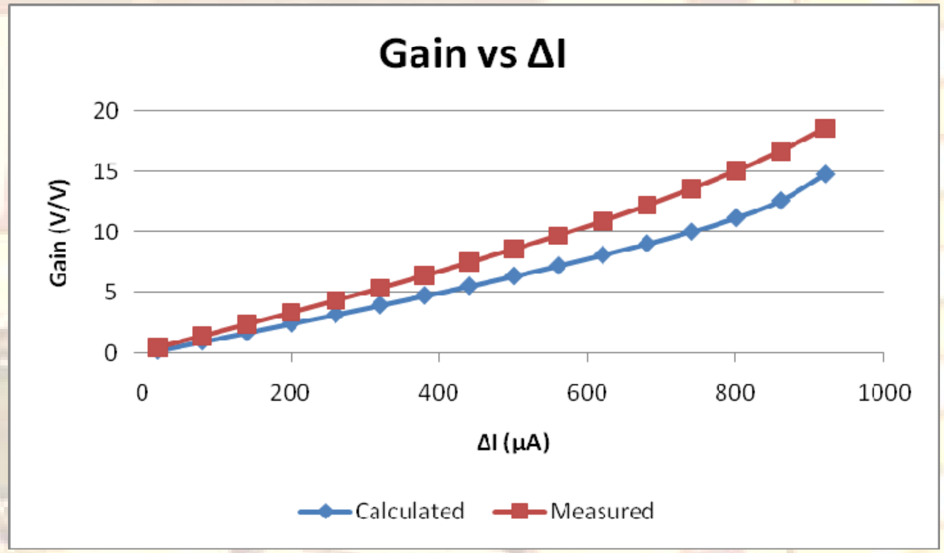
Digital Control Circuit: Working



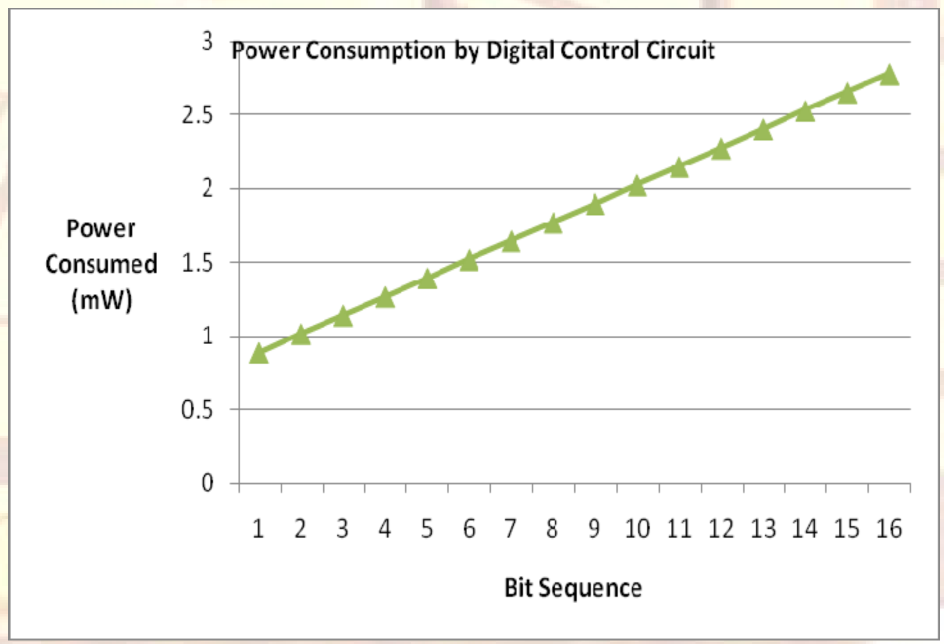
--- Mirrored Current
→ Current Path

Digital Control Circuit: Performance

- Linear dependence of Gain on Differential current



- Moderate power consumption

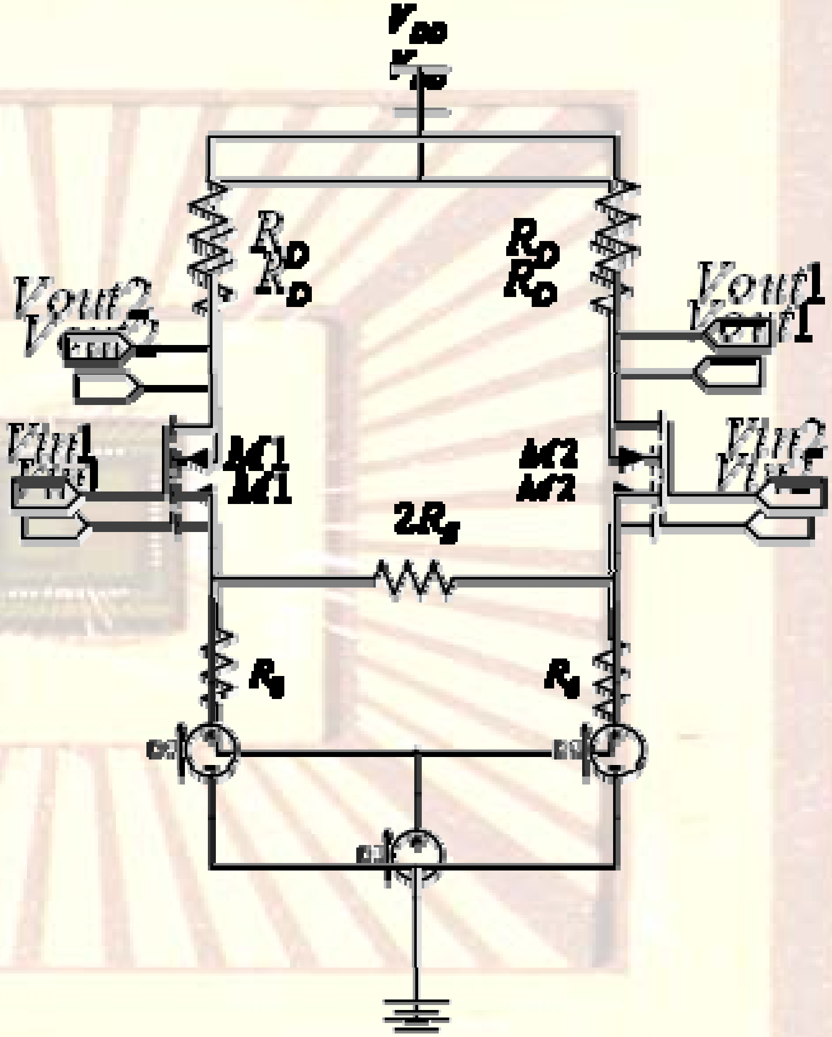


Post Amplifier

Linearity?

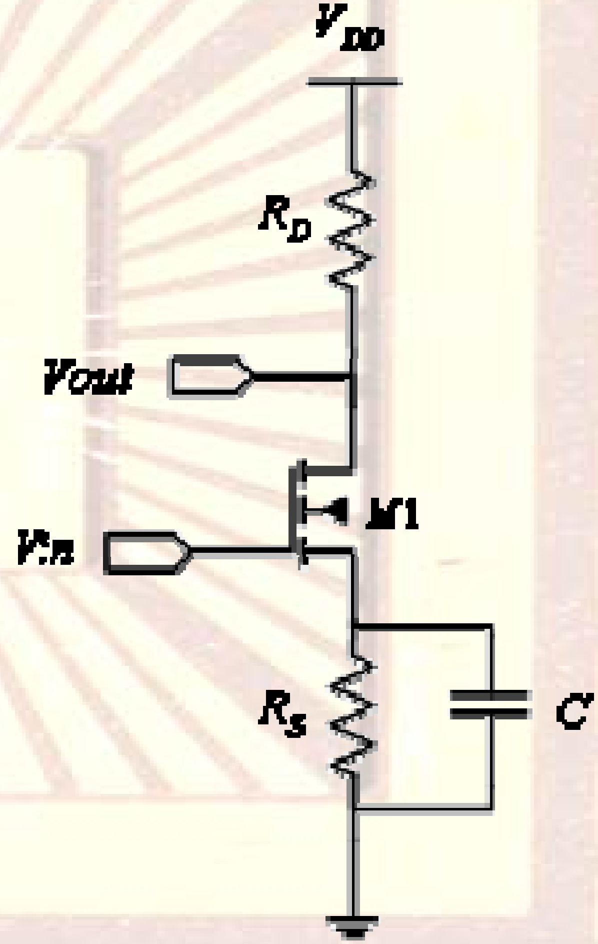
$$G_m = \frac{g_m}{1 + g_m R_S} \approx \frac{1}{R_S}$$

Headroom?



Post Amplifier

$$G_m = \frac{g_m}{1 + g_m R_S \,||\, (\frac{1}{sC})} = g_m \frac{1 + sR_S C}{1 + g_m R_S}$$

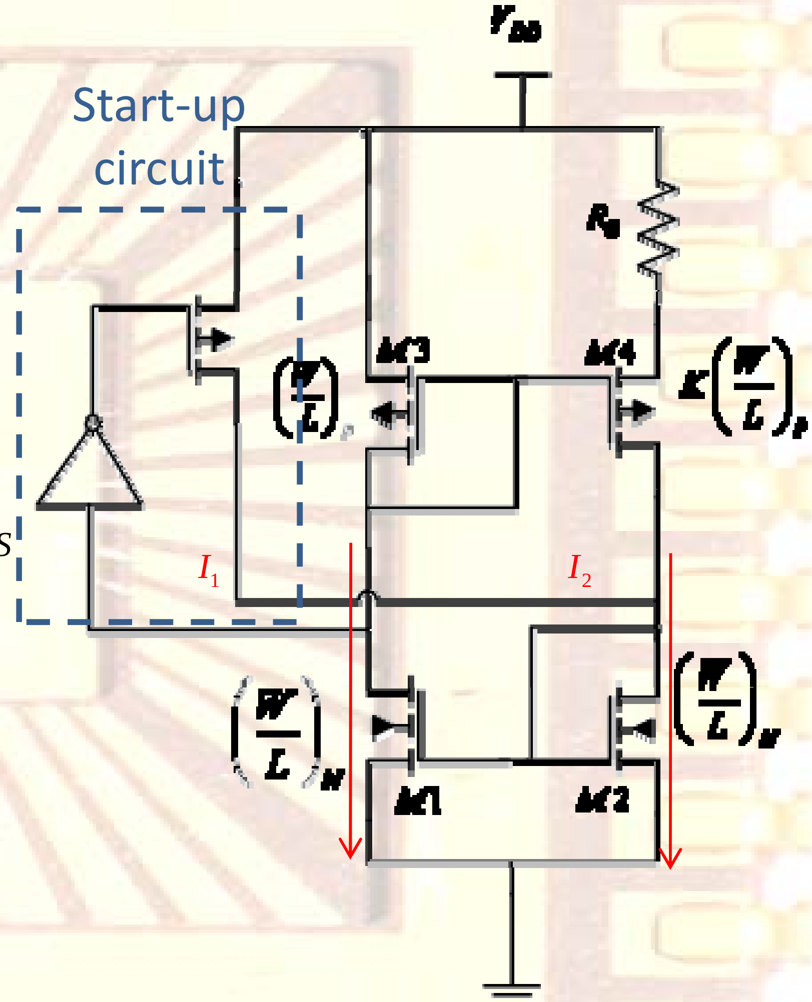


Constant-Gm Biasing

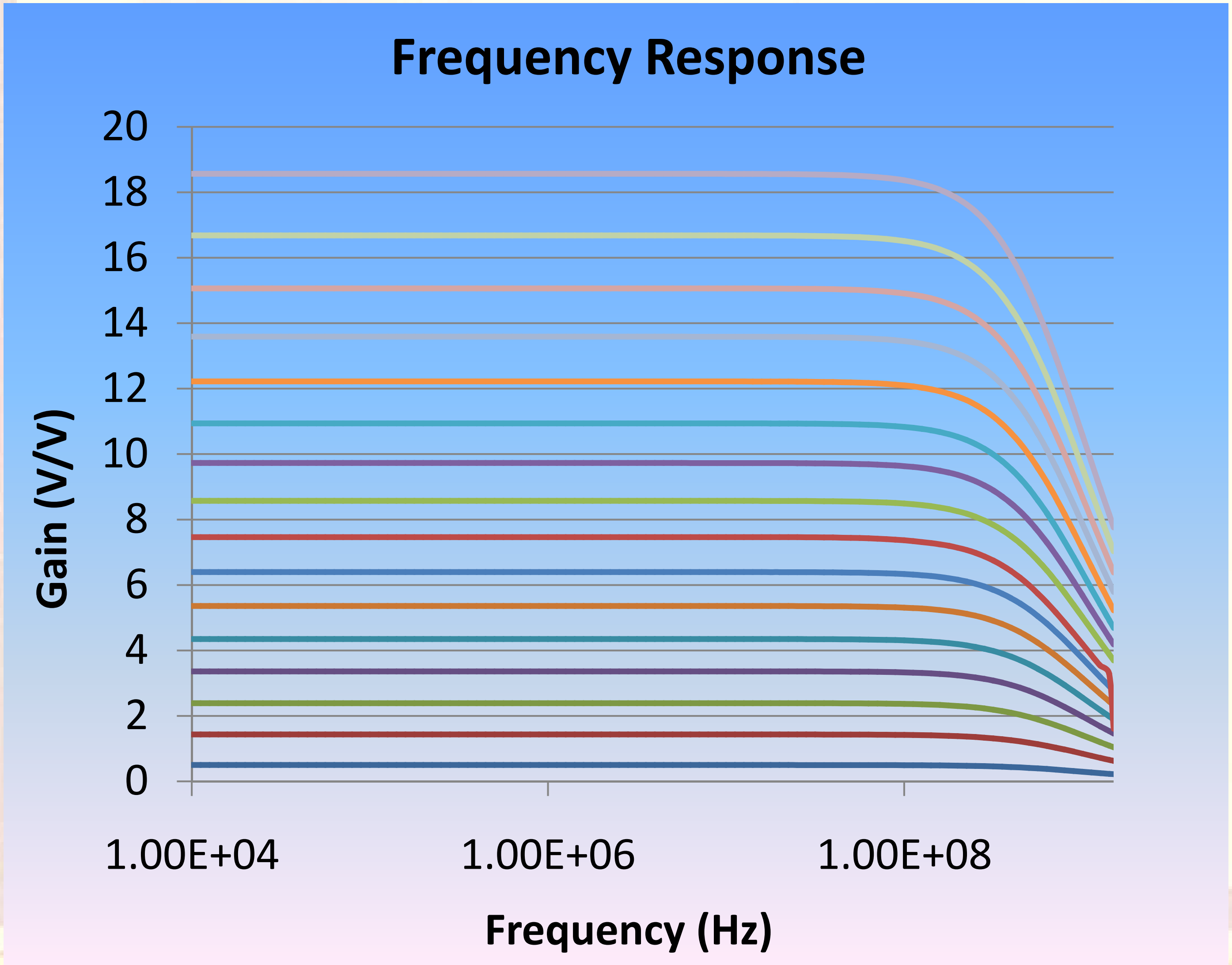
$$V_{SG3} = V_{SG4} + I_2 R_S$$

$$\sqrt{\frac{2I_1}{k'_P (W/L)_p}} + V_{th} = \sqrt{\frac{2I_2}{k'_P K (W/L)_p}} + V_{th} + I_2 R_S$$

$$I_2 = \frac{2}{\mu_P C_{OX}(W/L)_N}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2$$

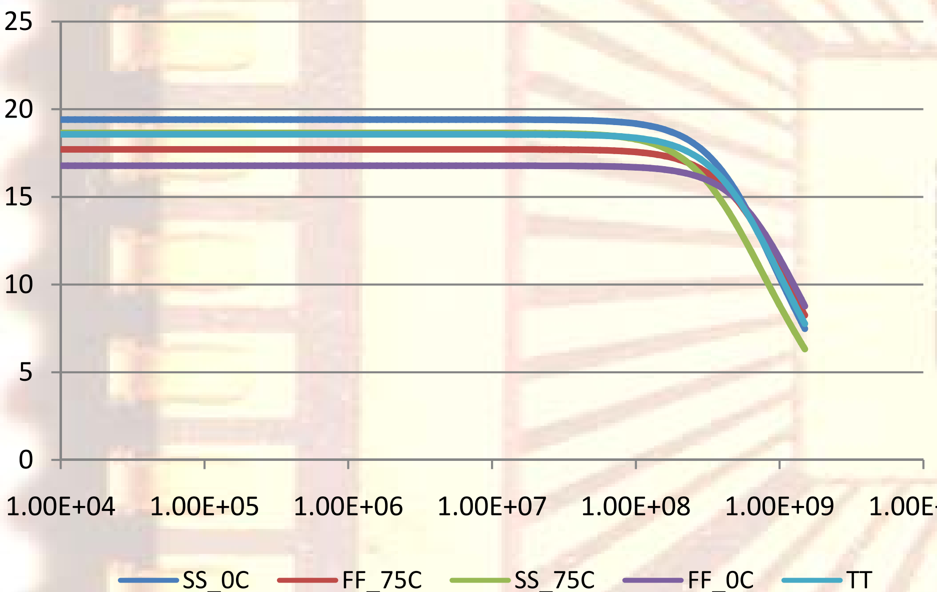


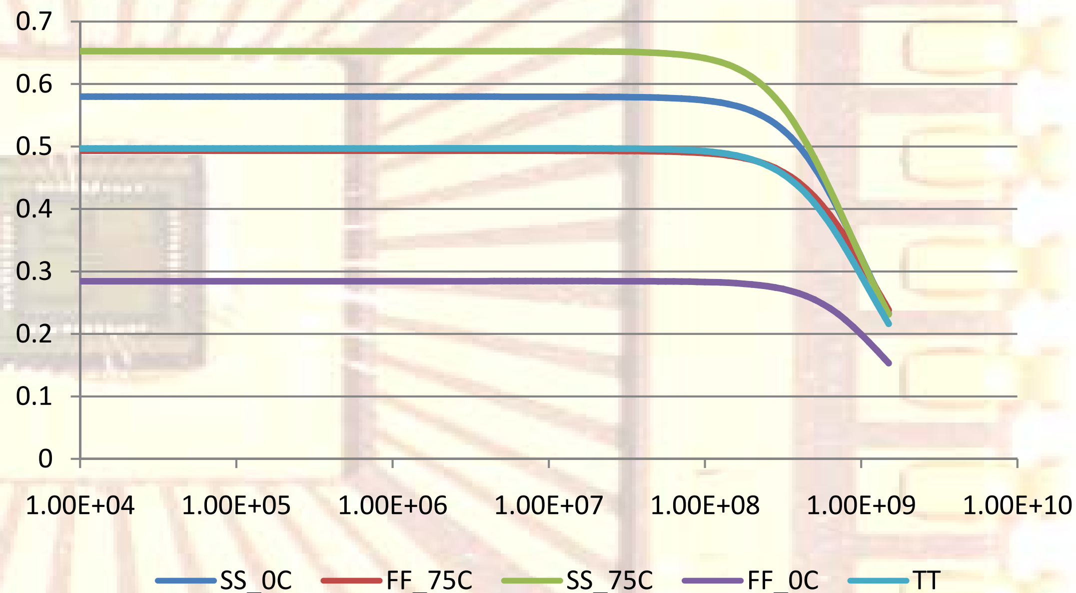
Simulation Results



Simulation Results

- Corners

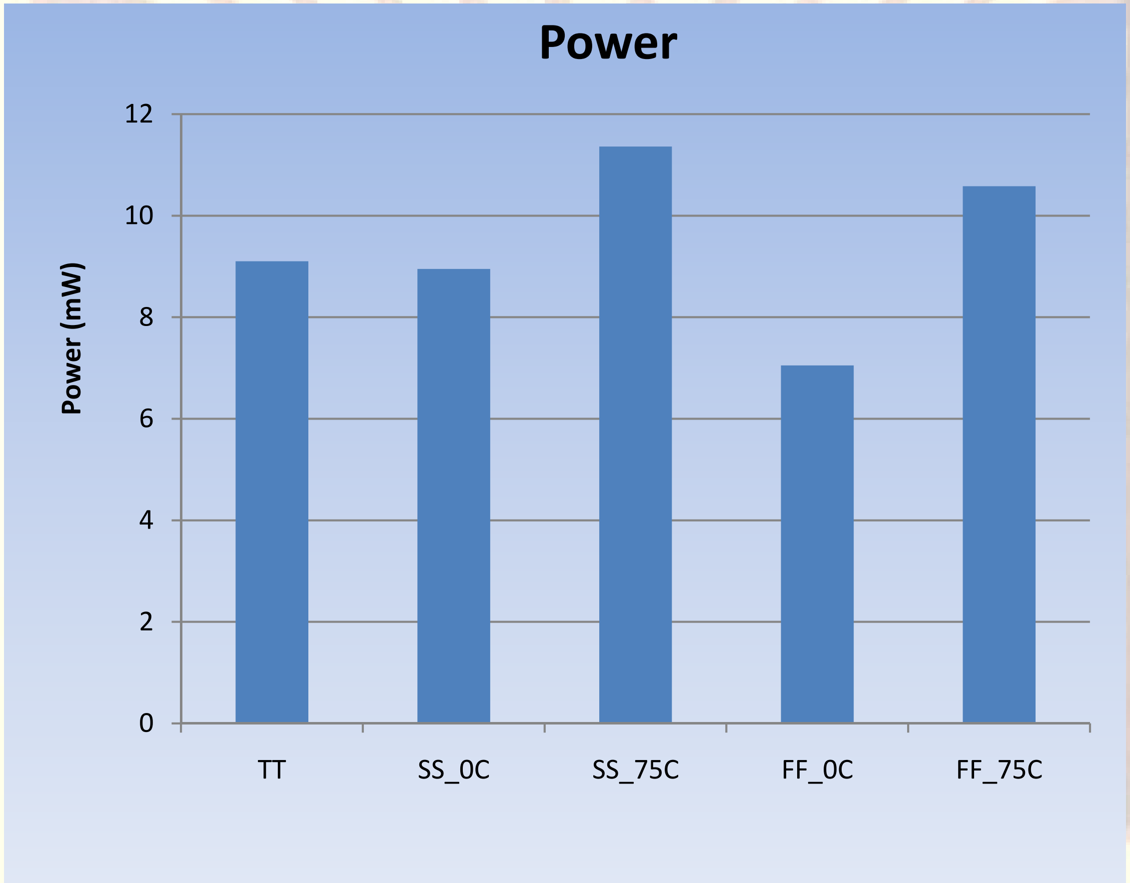




Maximum Gain

Minimum Gain

Simulation Results



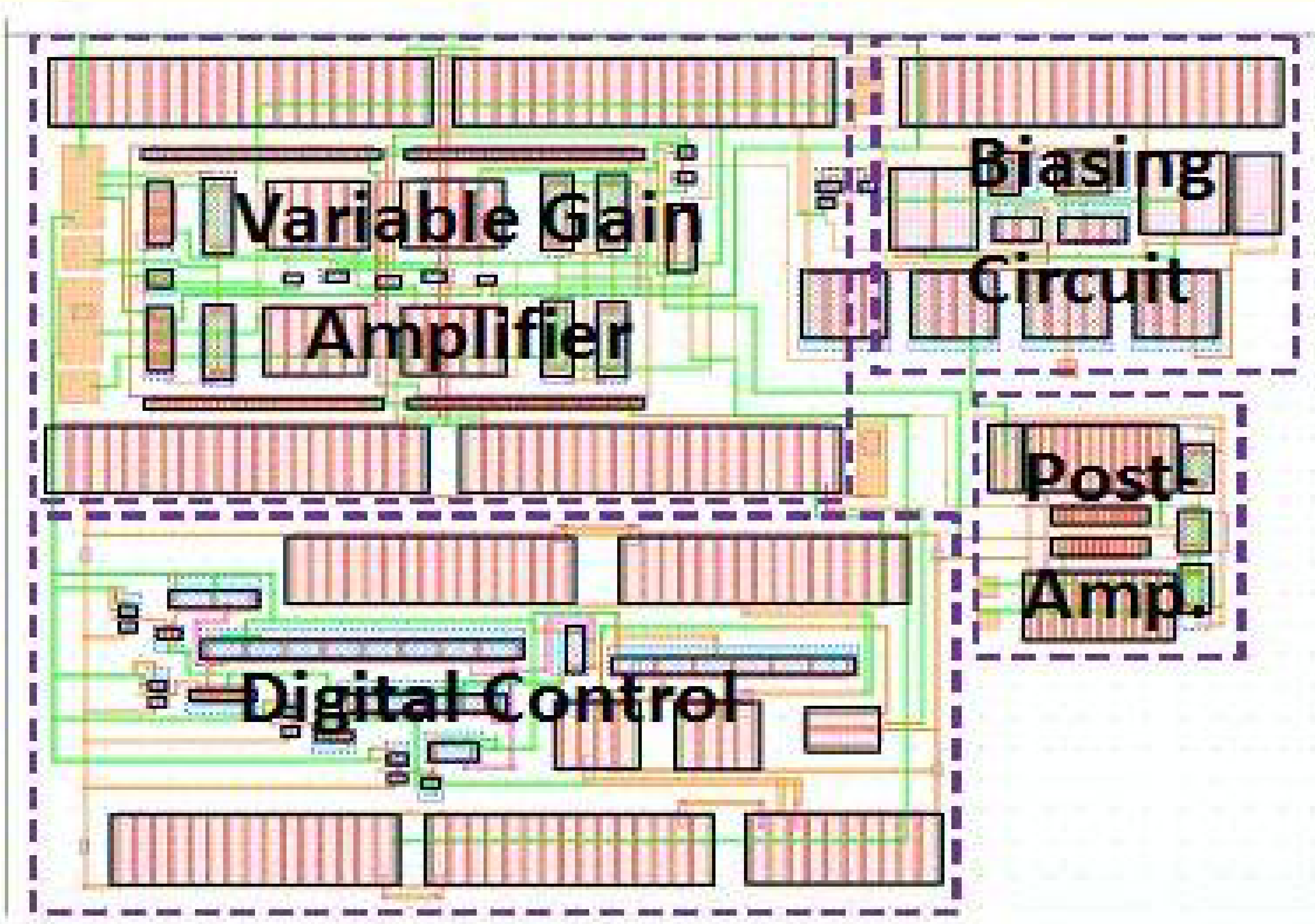
Conclusions

- A Gilbert Cell with gain proportional to $\Delta\sqrt{I}$
- PMOS current source loads doubles the gain
- Step currents set by a Digital Control circuit
- CMFB stabilizes output DC voltage level
- A 6-dB Post-Amp with inductive peaking
- A design of constant-gm biasing circuit

Result Table

		TT	SS_0C	SS_75C	FF_0C	FF_75C
Extraction	Max Gain (dB)	25.38	25.76	25.42	24.49	24.97
	Max Gain (V/V)	18.568	19.412	18.654	16.778	17.714
	Min Gain (dB)	-6.073	-4.734	-3.707	-10.92	-6.140
	Min Gain (V/V)	0.4970	0.5798	0.6526	0.2844	0.4932
	Bandwidth (MHz)	689	635	517	939	775
	Power (mW)	9.101	8.950	11.36	7.048	10.58
Schematics	Max Gain (dB)	25.38	25.76	25.41	25.08	24.97
	Max Gain (V/V)	18.568	19.412	18.652	17.946	17.716
	Min Gain (dB)	-6.069	-4.734	-3.707	-9.005	-6.136
	Min Gain (V/V)	0.4972	0.5798	0.6526	0.3546	0.4934
	Bandwidth (MHz)	899	821	637	1333	1030
	Power (mW)	9.266	9.020	11.36	8.600	10.76

Thank You !



Questions?

References

[1] Chia-Hsin Wu et. al., "A 2GHz CMOS Variable Gain Amplifier with 50 dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet", ISSCC 2004.

[2] Quoc-Hoang Duong et.al, "An All CMOS 743MHz Variable Gain Amplifier for UWB Systems", IEEE International Symposium on Circuits and Systems 2006.

[3] Sivasankari Krishnanji, "Design of a Variable Gain Amplifier for an Ultra Wideband Receiver", Master's Thesis, Texas A&M University.

[4] Po-Chiun Huang, Li-Yu Chiou, Chorng-Kuang Wang, "A 3.3V CMOS Wideband Exponential Control variable-gain-amplifier", Proceedings of the IEEE International Symposium on Circuits and Systems, 1998.