A Low Power Low Frequency Sample and Hold Circuit for Implantable Pacemaker

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Outline

• What is sample and hold circuit?
• Motivation: why low power?
• Specs and Target
• Design Topology
• Simulation Results and Analysis
• Summary
Sample and Hold Circuit

- Sample the input signal
- Hold the signal steady for a period of time until the next stage can process the signal
Why Low Power?

- Remain in body for 5-10 years
- To avoid frequently changing of battery by surgery.
Targets

• Power: nano Watts

• Leakage current: fA

• Error signal: uV
Our solutions

• Power supply: 0.7 Volts

• Subthreshold operation

• Leakage cancellation circuit
Op-amp
Op-amp simulation

![Graph showing gain and phase response over frequency for different conditions: FF_0C, FF_75C, SS_0C, SS_75C, TT. The graphs plot gain (dB) and phase (degree) against frequency (Hz) on a log-log scale.]
Leakage Current Cancellation

Advantages:
• Reduces Voltage drift during hold time
• Reduces the size of the capacitor, effectively reducing the area of the layout
Operation

- Input
- Output
- Switch Network
- C hold
- C rep
- Op_amp
- Leakage Current Cancellation Feedback
- Clock
Detailed Circuit Diagram of Leakage Current Cancellation Circuitry
Variation of cancellation current with input voltage of leakage circuitry
The variation of voltages on Crep and Chold during hold mode (left).
Simulation Results

Output of S/H circuit at 37C (upper) and zoom-in plot of hold period showing the settling time (bottom)
Simulation Results

Corner simulation of the S/H circuit over 32°C to 42 °C
## Conclusion

<table>
<thead>
<tr>
<th>Specification</th>
<th>Our work</th>
<th>Other’s work</th>
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<tbody>
<tr>
<td>Power</td>
<td>92.9nW</td>
<td>~150nW</td>
</tr>
<tr>
<td>Leakage current after cancellation</td>
<td>4fA</td>
<td>10fA</td>
</tr>
<tr>
<td>Settling time</td>
<td>4ms</td>
<td>??</td>
</tr>
<tr>
<td>Hold capacitor</td>
<td>10pF</td>
<td>1pF</td>
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</tbody>
</table>
Thank you!

Questions?