A Low Power Low Frequency Sample and Hold Circuit for Implantable Pacemaker

Fu Sun, Ali Ahmed and Guan Huang

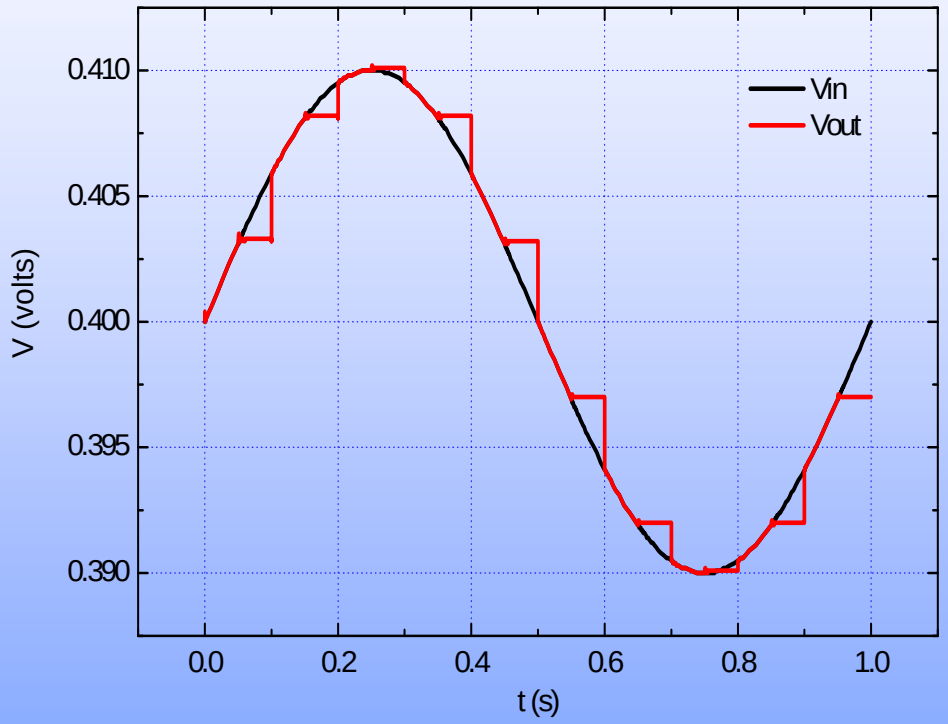
Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109-2122, USA

Outline

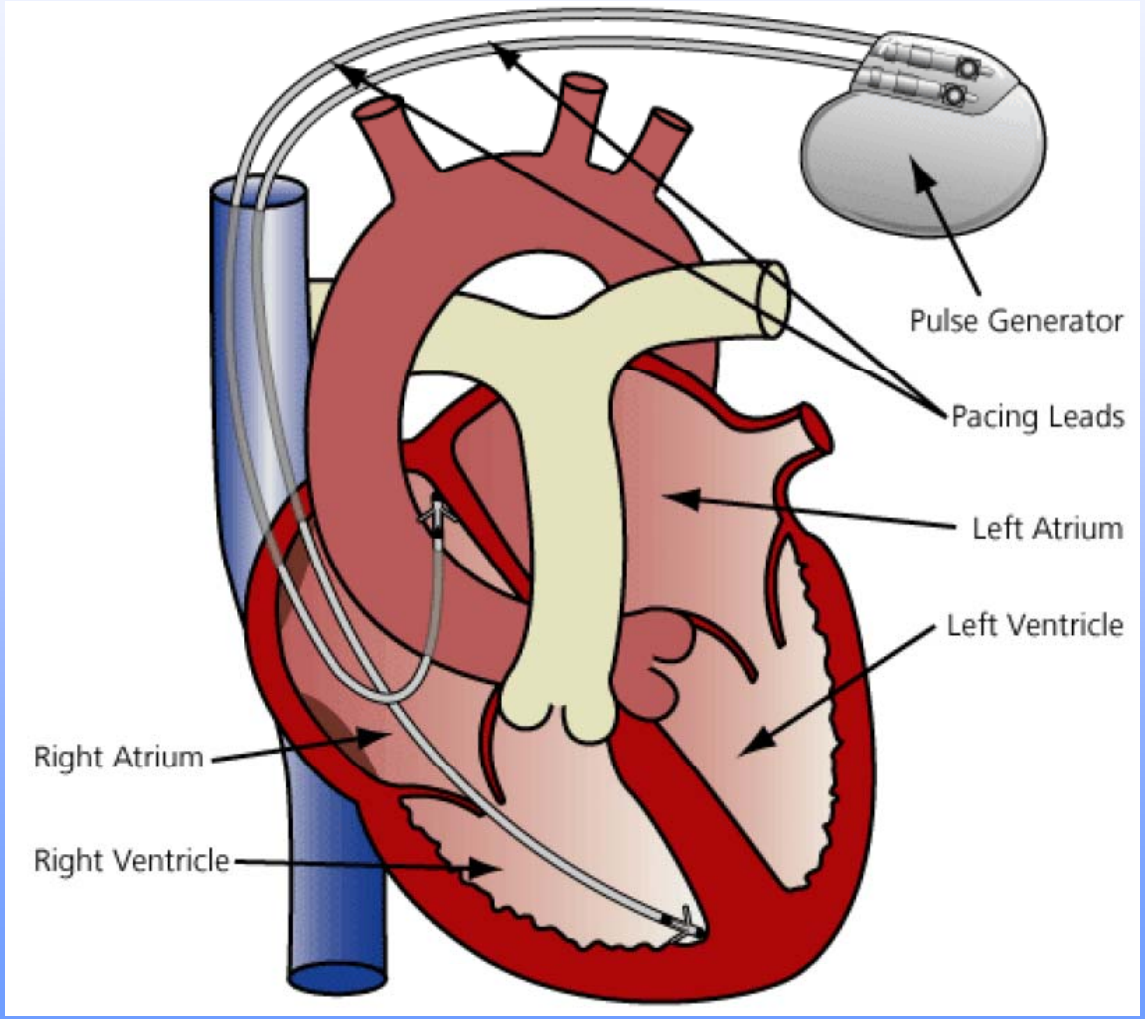
- What is sample and hold circuit?
- Motivation: why low power?
- Specs and Target
- Design Topology
- Simulation Results and Analysis
- Summary

Sample and Hold Circuit

- Sample the input signal
- Hold the signal steady for a period of time until the next stage can process the signal



Why Low Power?



- Remain In body for 5 -10 years
- To avoid frequently changing of battery by surgery.

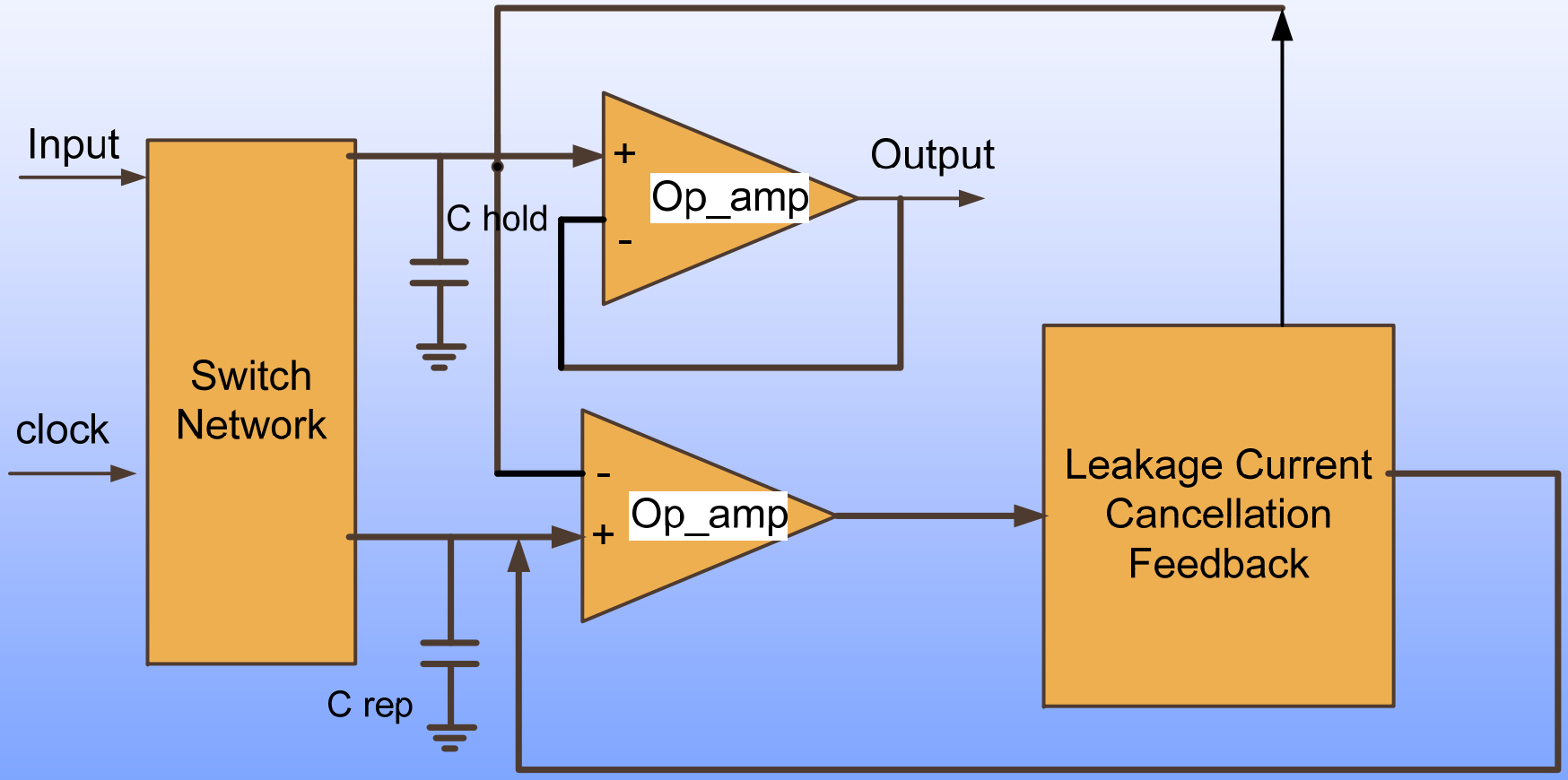
Targets

- Power: nano Watts
- Leakage current: fA
- Error signal: uV

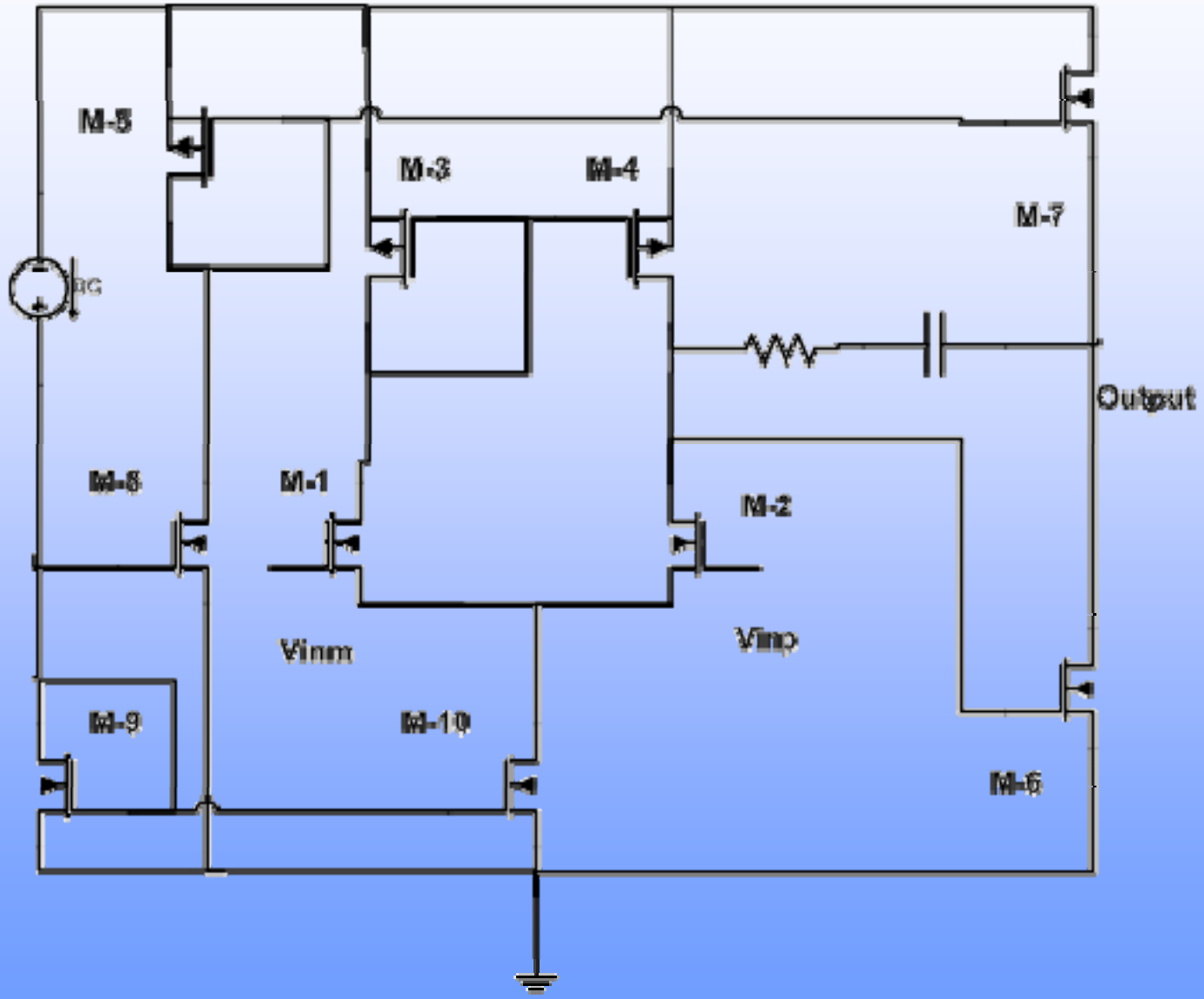
Our solutions

- Power supply: 0.7 Volts
- Subthreshold operation
- Leakage cancellation circuit

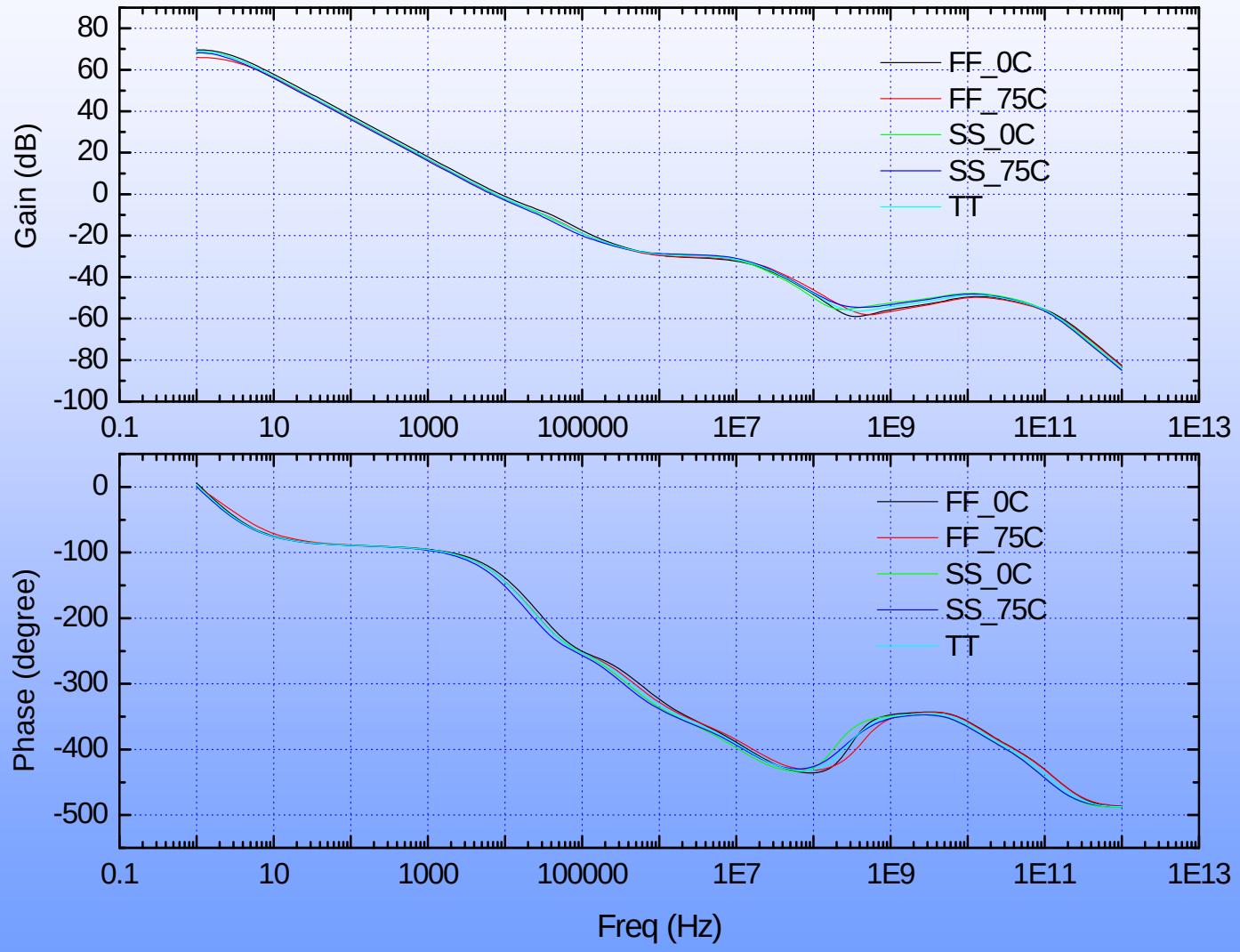
Block Diagram



Op-amp



Op-amp simulation



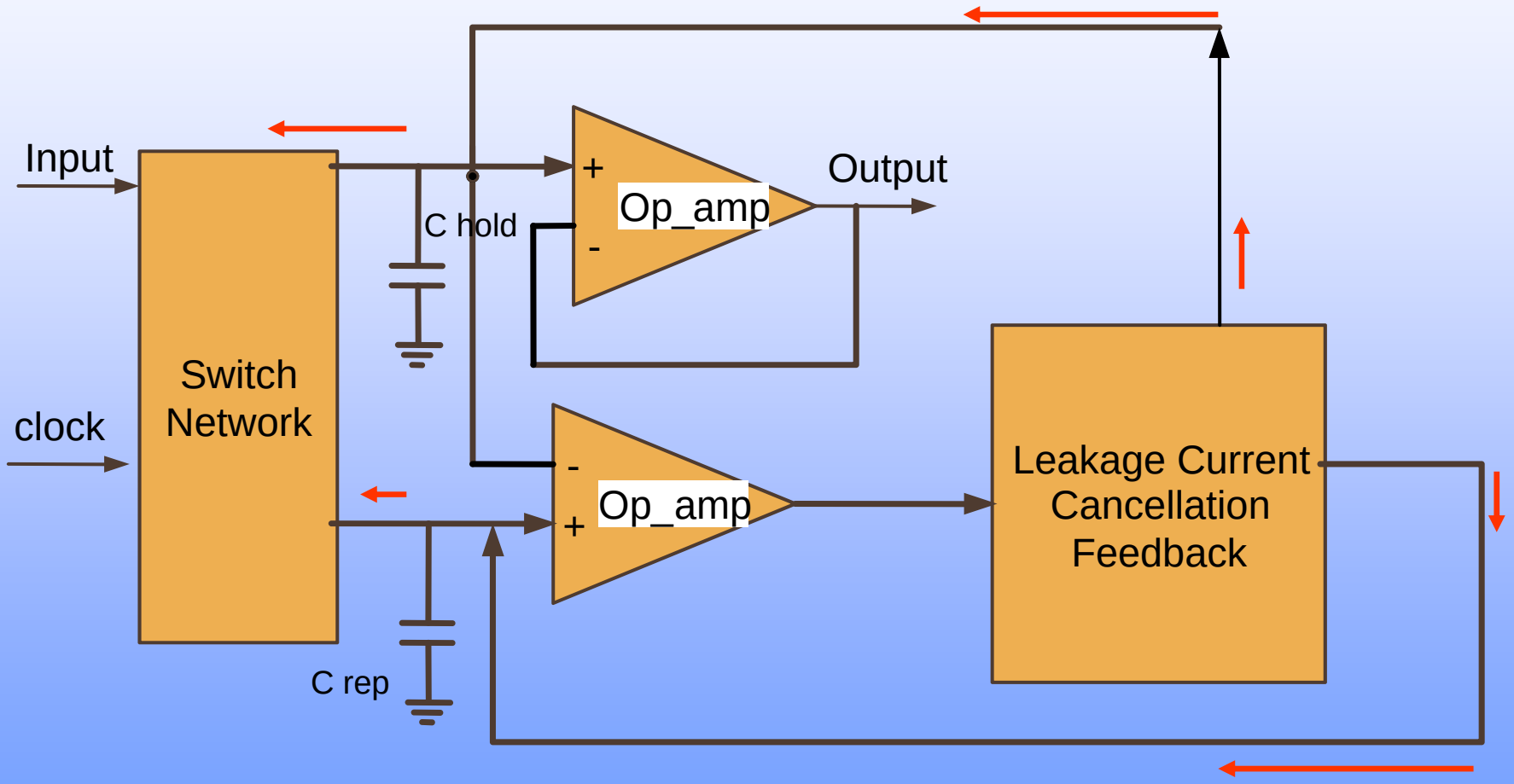
Leakage Current Cancellation

Advantages:

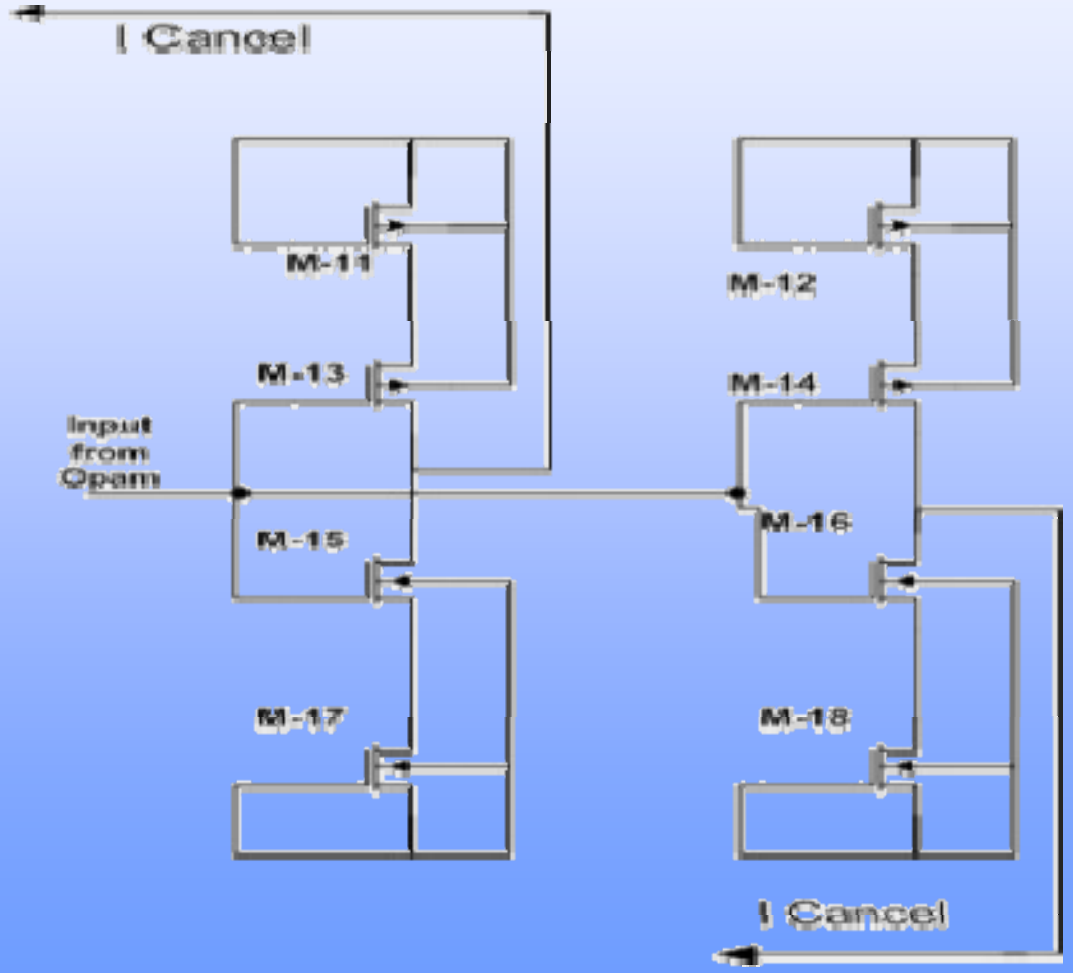
- Reduces Voltage drift during hold time

- Reduces the size of the capacitor, effectively reducing the area of the layout

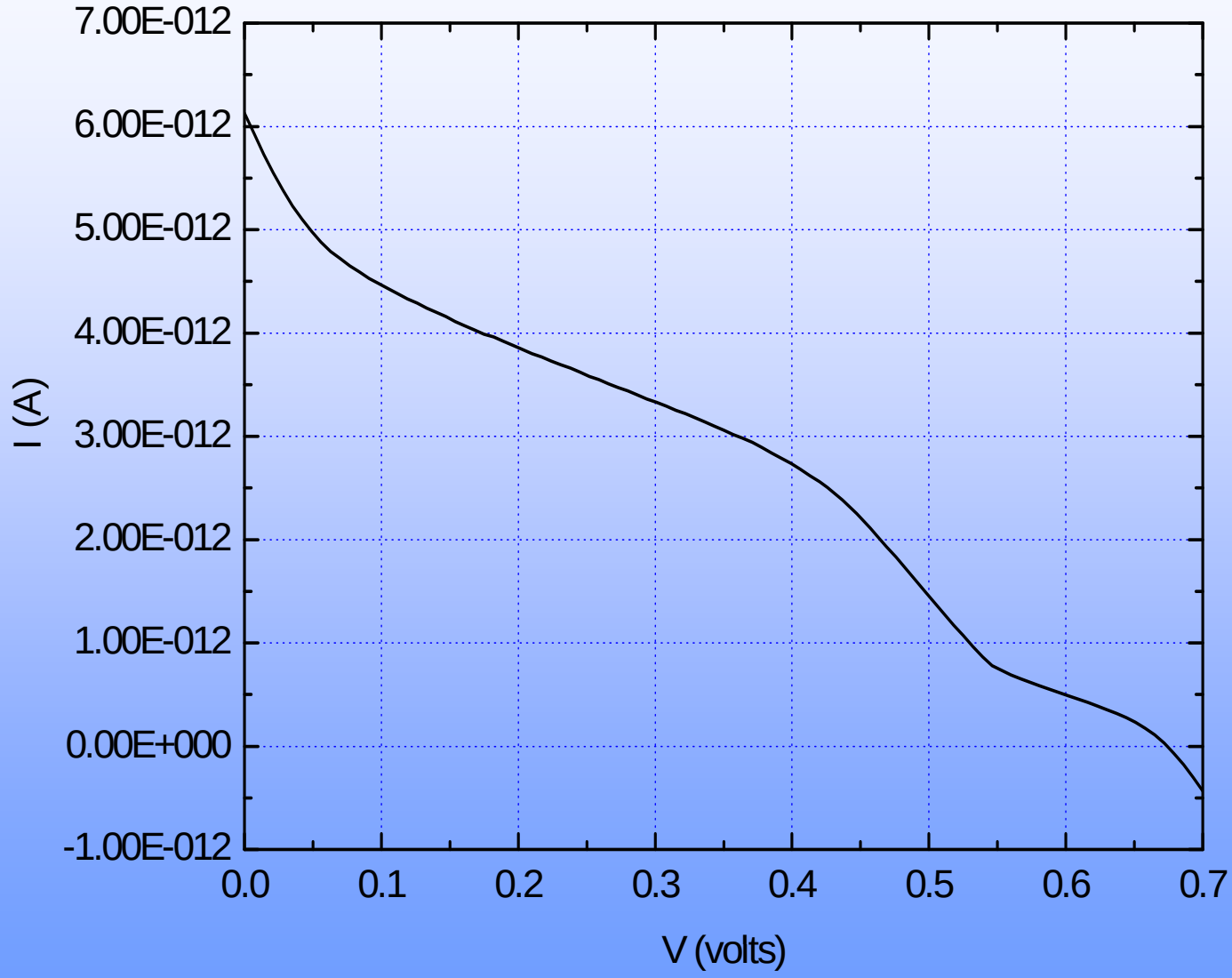
Operation

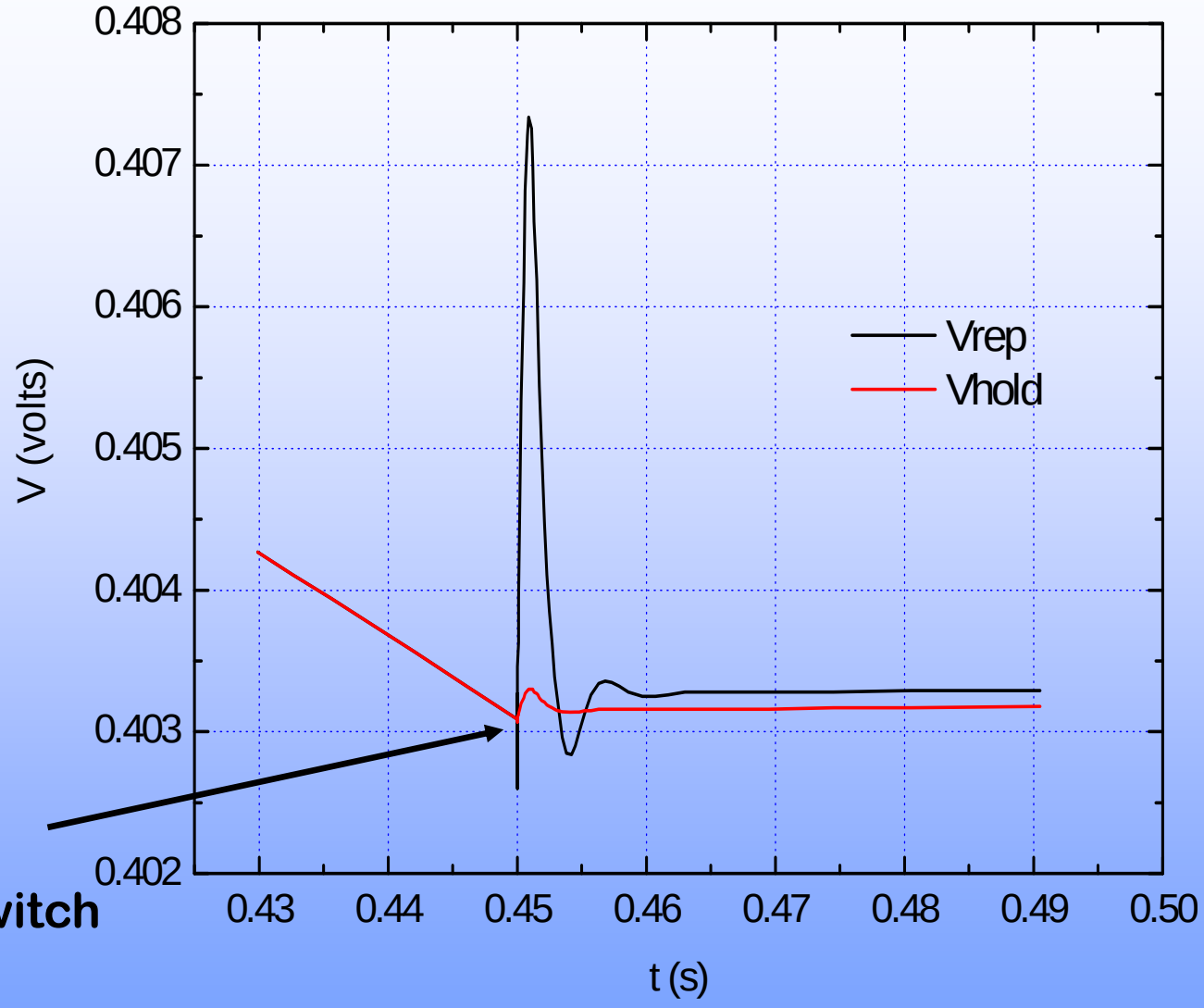

Input
clock
Switch Network
C hold
C rep
+
-
Op_amp
Output
-
+
Op_amp
Leakage Current Cancellation Feedback

Detailed Circuit Diagram of Leakage Current Cancellation Circuitry



Variation of cancellation current with input voltage of leakage circuitry

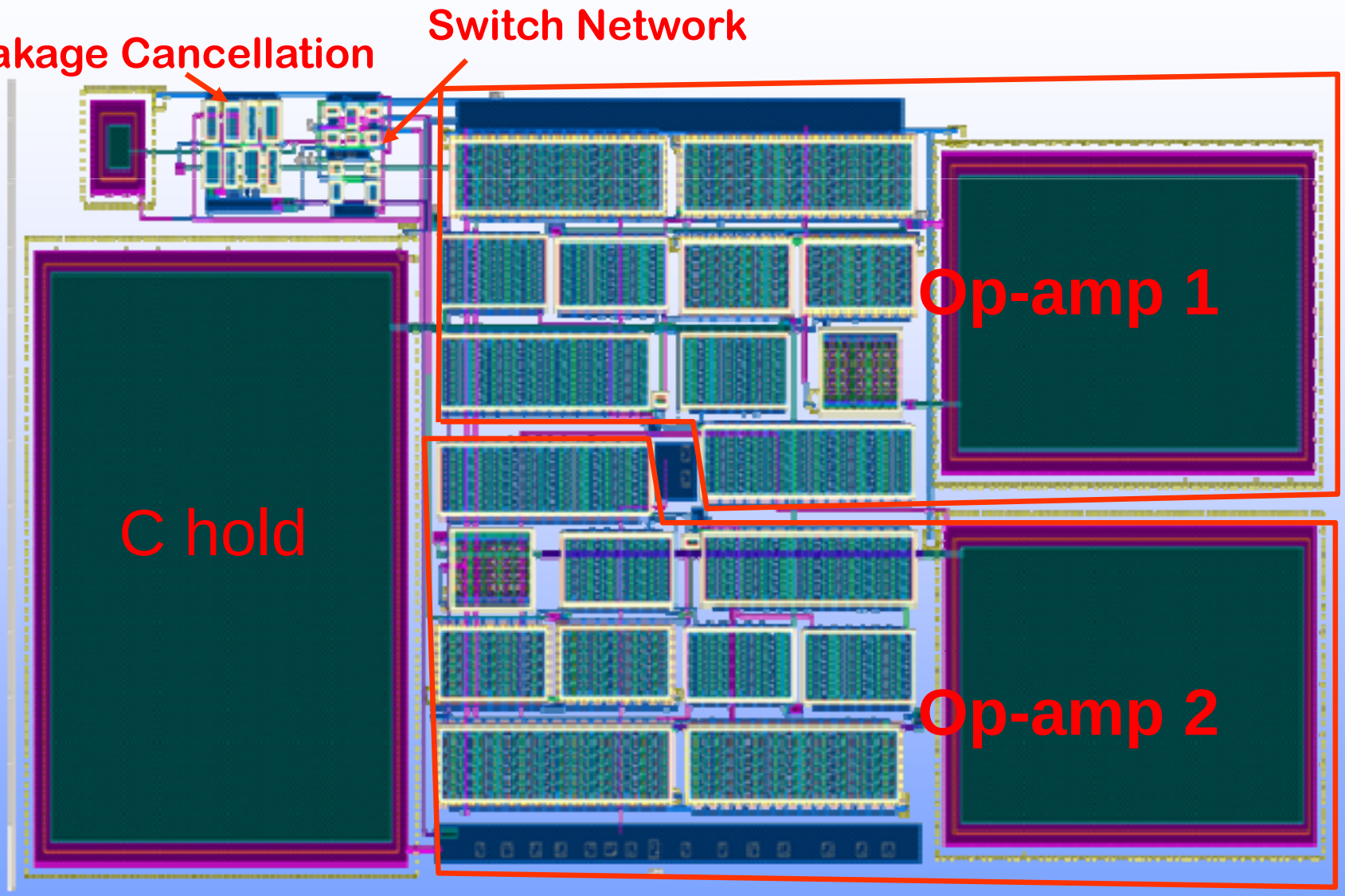




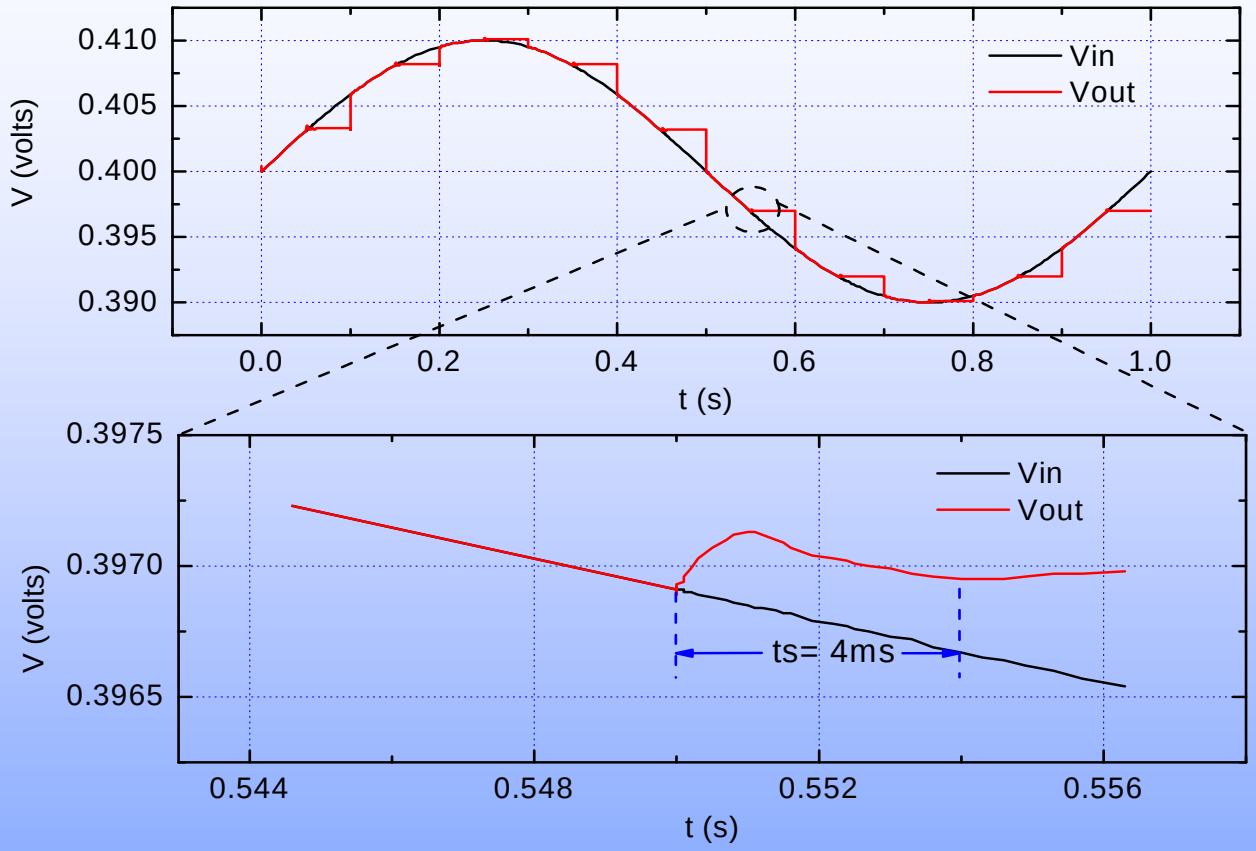
Hold time Starts (switch turns off)

The variation of voltages on Crep and Chold during hold mode (left)

Layout

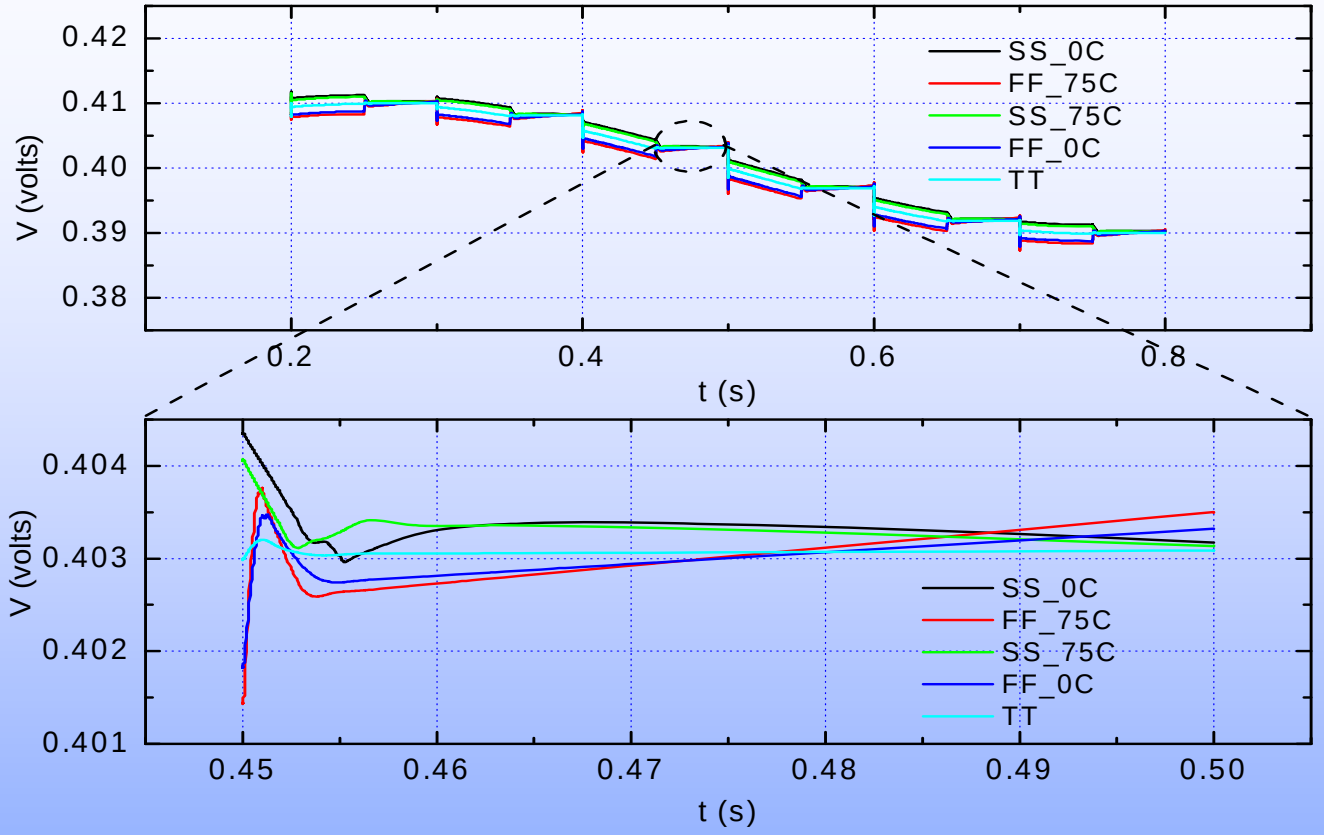


Simulation Results



Output of S/H circuit at 37C (upper) and zoom-in plot of hold period showing the settling time (bottom)

Simulation Results



Corner simulation of the S/H circuit over 32˚C to 42 ˚C

Conclusion

Specification	Our work	Other's work
Power	92.9nW	~150nW
Leakage current after cancellation	4fA	10fA
Settling time	4ms	??
Hold capacitor	10pF	1pF

Thank you!

Questions?