A Digitally-Controlled CMOS Variable Gain Amplifier for Ultrasound Imaging

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Motivation – Gain Compression for Ultrasound

- Typical dynamic range for ultrasound signal is ~ 110dB
- Ultrasound ADCs typically have dynamic range of 70dB
- Use VGA with dynamic range of 40dB to compress the dynamic range of the received signal
- $V_{BE}$ of BJT has a negative TC
- Difference in $V_{BE}$ between BJTs of different current densities has a positive TC
- Positive TC scales by $\ln(n)$ if $M_{11}$ and $M_{12}$ have the same $W/L$ ratio
- Reduce size by scaling $W/L$ of $M_{12}$ rather than adding more BJTs
- Scale $M_{16}$ relative to $M_{15}$ to meet current spec
Process Variations

- Performance of VGA over process variations relies on the accuracy of the reference current
- Sacrifice TC for improvement in process variation
- Changing M13 from an NFET to a PFET reduces the effect of process variations
\[ I_{in}^+ = I_{M1} - I_{M5} = I_{M2} - I_{M6} = I_R; \]
\[ I_{in}^- = I_{M4} - I_{M8} = I_{M3} - I_{M7} = -I_R \]

\[ I_{Id} = I_{in}^+ - I_{in}^- = 2I_R = \frac{(V_A - V_B)}{R} = \frac{V_{Id}}{R} \]
\[ I_{\text{out}} = I_{\text{in}} (1 + d_0 + 2d_1 + 4d_2 + \ldots + 2^m d_m) = 2^{(m+1)} = 6(m+1) \text{dB} \]
Advantages of multi cell implementation

- Low power Consumption
- Higher Bandwidth

Each $d_n$ stage = 6 dB gain
2 $d_n$ stages / cell (12 dB / cell)
4 Cells needed to achieve > 40 dB gain
Output Stage (Current to Voltage)

\[ V_{OD} = V_0^+ - V_0^- \]
\[ = (I_{OUT}^+ - I_{OUT}^-)R_2 \]
\[ = I_{OD}R_2 \]
\[ = (-1)^n A_1 A_2 \ldots A_n V_{ID} R_2 / R \]

Can fine tune gain by manipulating value of R2!!
Output Stage variable resistor for 1 dB fine control

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R21</td>
<td>R*</td>
</tr>
<tr>
<td>R22</td>
<td>0.148 R</td>
</tr>
<tr>
<td>R23</td>
<td>0.168 R</td>
</tr>
<tr>
<td>R24</td>
<td>0.190 R</td>
</tr>
<tr>
<td>R25</td>
<td>0.225 R</td>
</tr>
<tr>
<td>R26</td>
<td>0.155 R</td>
</tr>
</tbody>
</table>

* R is the load resistor in the input stage
• Systematic variations due to resistor mismatches in fine-tuning stage
Results! Total Bandwidth

- Peaking caused by parasitic capacitances of bias points
- < 0.5 dB peaking in BW
- 3 dB peak @ ~25 MHz (BW = 2-15 MHz)
Results! Gain with Process Variations

- Meet ± 0.5 dB accuracy at all corners except SS75
- ± 0.6 dB at max gain (40 dB)
- ± 1.2 dB at min gain (-13 dB)
### Parameter Specification Design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Design</th>
<th>MAX2037</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>&lt;150</td>
<td>47.53</td>
<td>120</td>
<td>mW</td>
</tr>
<tr>
<td>Operating Range</td>
<td>2-15</td>
<td>2-15</td>
<td>&lt; 29</td>
<td>MHz</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>40 (-13 to 40)</td>
<td>53 (-12.5 to 29.5)</td>
<td>42 (-12.5 to 29.5)</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Accuracy (over process corners)</td>
<td>±0.5 (±0.5)</td>
<td>±0.2 (±1.2)</td>
<td>±0.25 (±1.0)</td>
<td>dB</td>
</tr>
<tr>
<td>Reference Current</td>
<td>50±3%</td>
<td>50±2.4%</td>
<td>--</td>
<td>μA</td>
</tr>
</tbody>
</table>

- **Tradeoff:** Decrease gain to increase operating range
• Propagation modes are equal and attenuation constants have equal magnitude and opposite sign.

• Symmetric mode is cutoff.

• Anti-symmetric mode exhibits backward-wave behavior.
Bonus Footage: Layout ahoy!

- Total size: 480 µm x 235 µm = .113 mm²
- Rectangular(ish) in shape.
• $A(s) \sim g_m(r_o/2)$
• $\beta = 1$
• Loop gain $\sim g_m(r_o/2)$
• Phase margin $\sim 134$ deg
• Stable operation