A Digitally-Controlled CMOS Variable Gain Amplifier for Ultrasound Imaging

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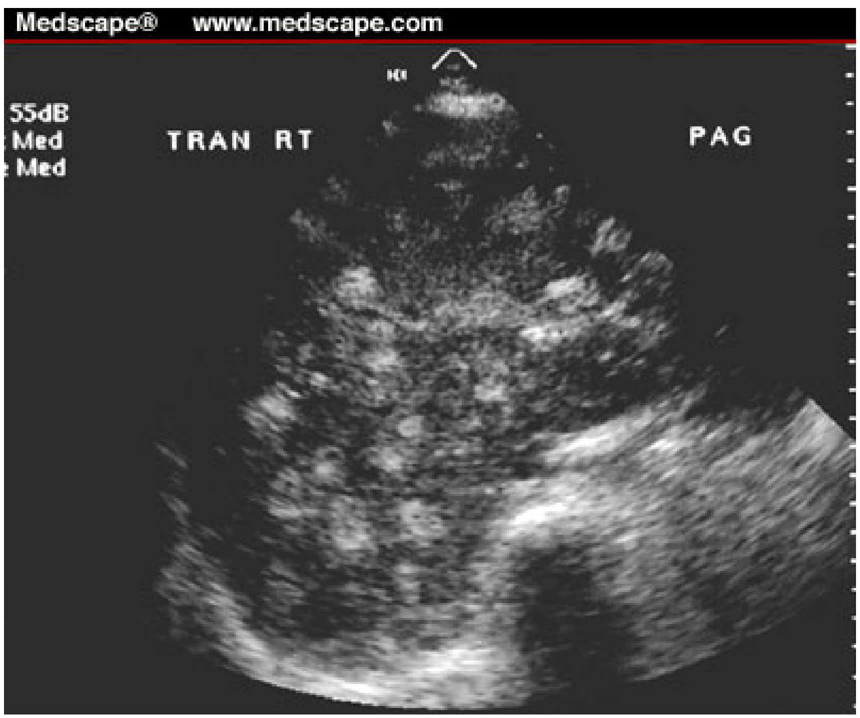
December 5, 2007

Motivation – Gain Compression for Ultrasound

- Typical dynamic range for ultrasound signal is ~ 110dB
- Ultrasound ADCs typically have dynamic range of 70dB
- Use VGA with dynamic range of 40dB to compress the dynamic range of the received signal

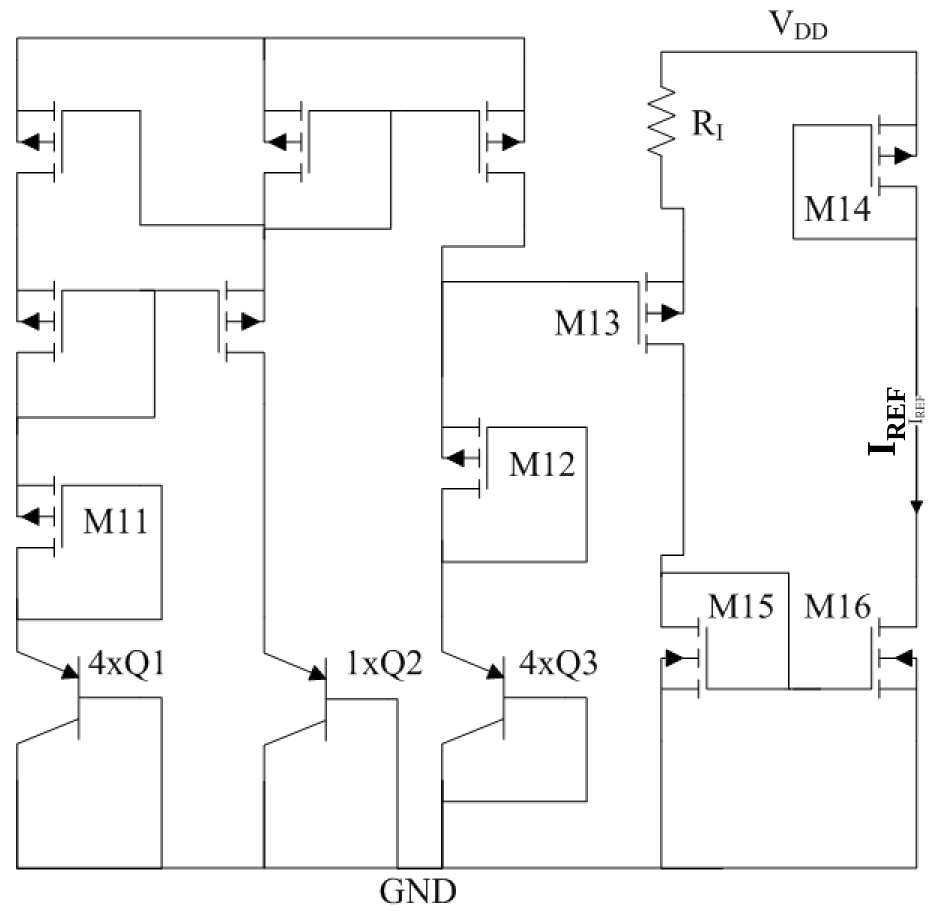


www. medscape.com

http://chrisnolan.ca/photos_loc/blog/00000987/ultrasound_3.jpg

Bandgap Reference Current Source

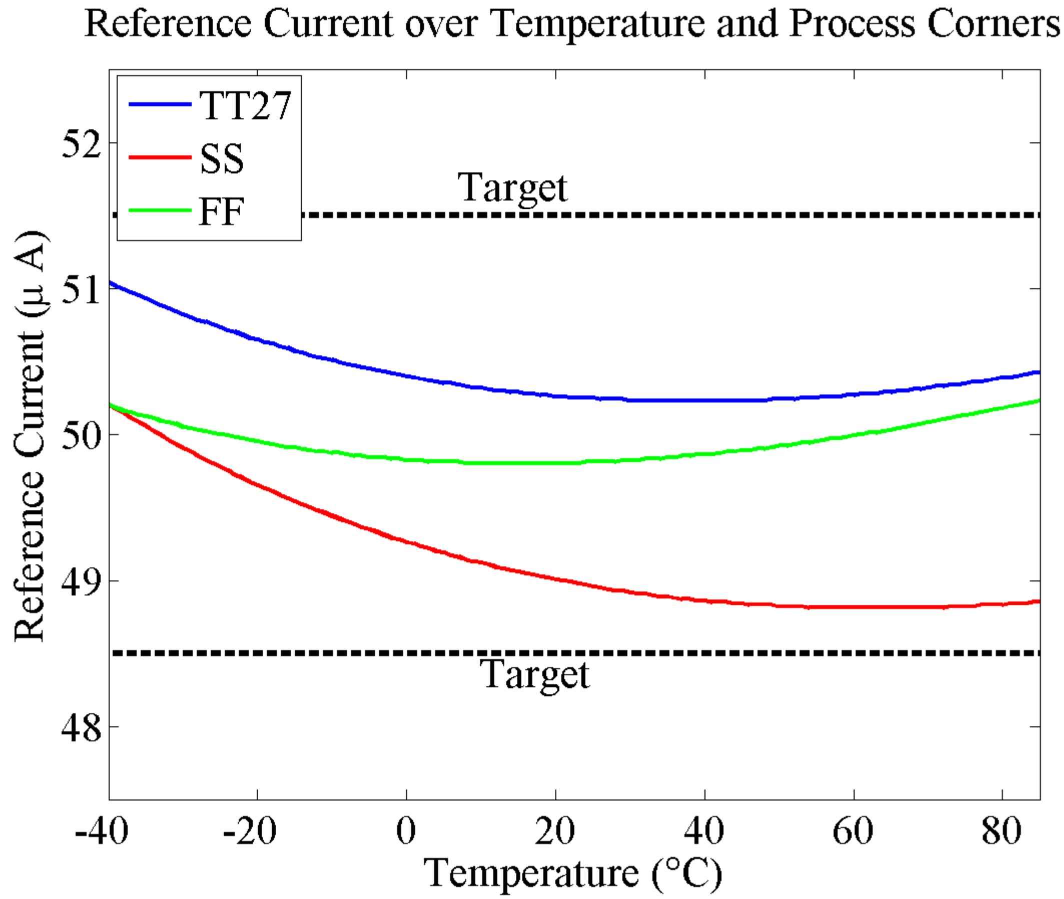
- V_{BE} of BJT has a negative TC
- Difference in V_{BE} between BJTs of different current densities has a positive TC
- Positive TC scales by ln(n) if M11 and M12 have the same W/L ratio
- Reduce size by scaling W/L of M12 rather than adding more BJTs
- Scale M16 relative to M15 to meet current spec



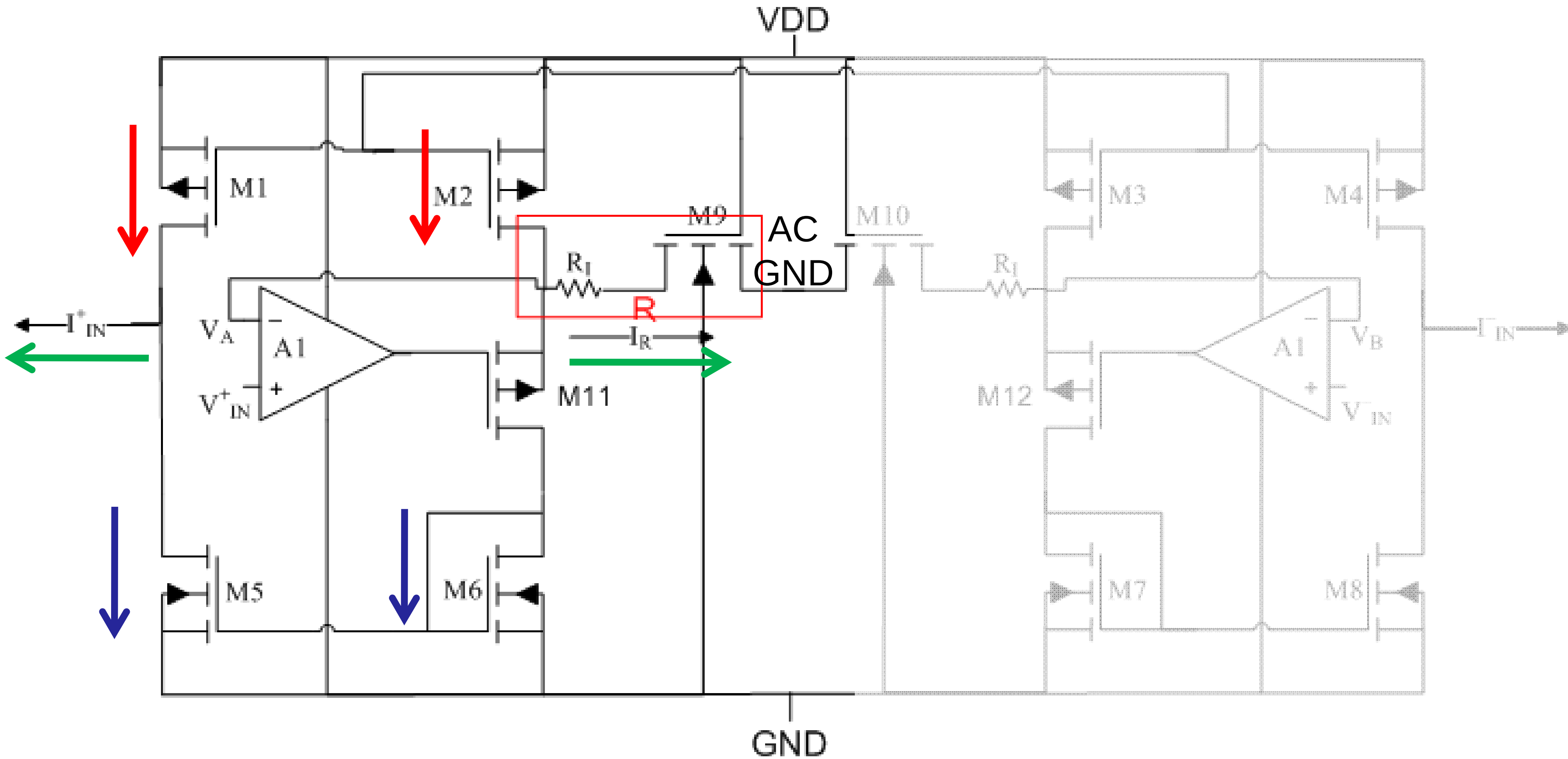
Bandgap Reference Current Source

Process Variations

- Performance of VGA over process variations relies on the accuracy of the reference current
- Sacrifice TC for improvement in process variation
- Changing M13 from an NFET to a PFET reduces the effect of process variations



Input Stage (Voltage to Current)

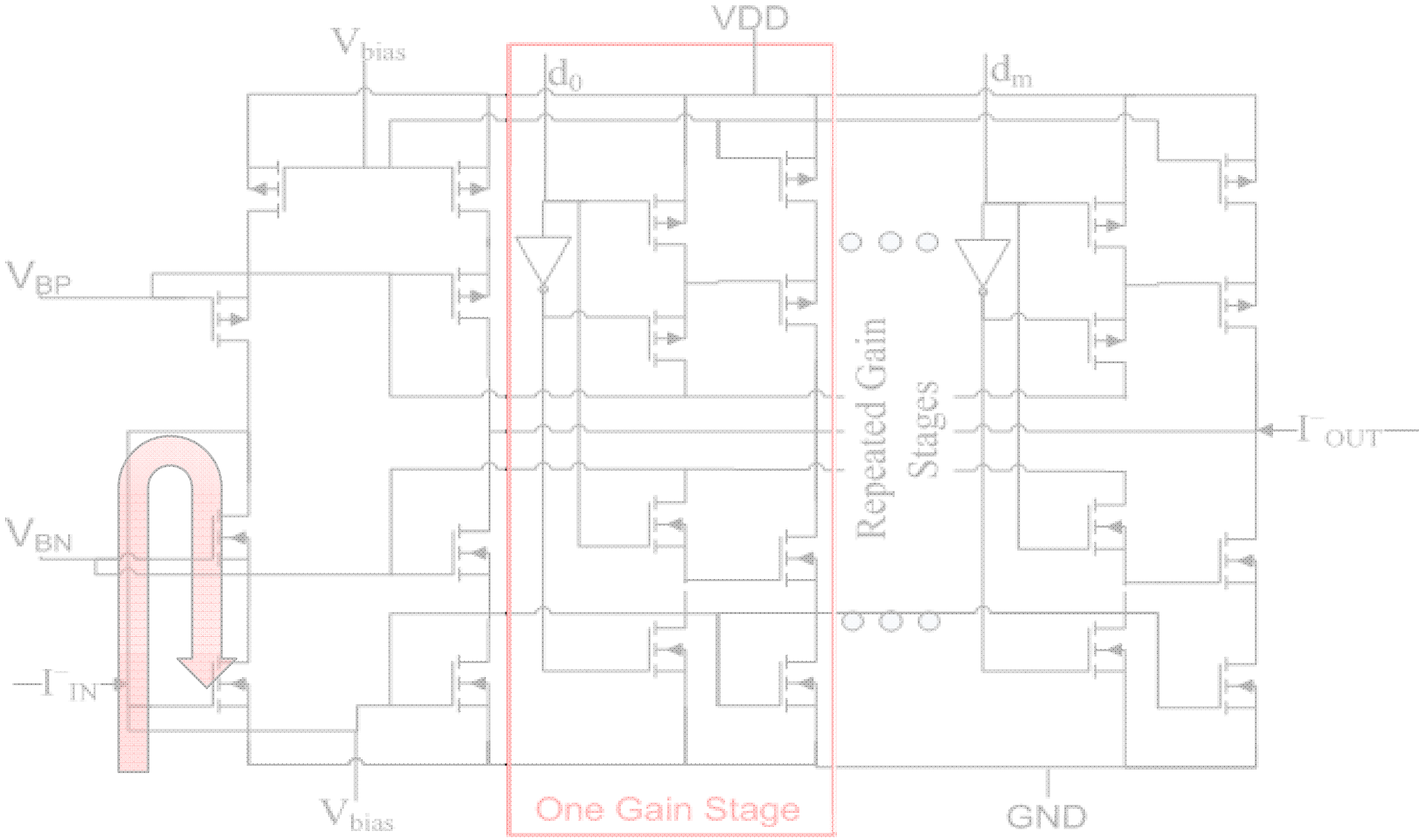


$$I^{+}_{in} = I_{M1} - I_{M5} = I_{M2} - I_{M6} = I_{R};$$

$$I^{-}_{in} = I_{M4} - I_{M8} = I_{M3} - I_{M7} = -I_{R}$$

$$I_{Id} = I^{+}_{in} - I^{-}_{in} = 2I_{R} = (V_{A}-V_{B})/R = V_{Id}/R$$

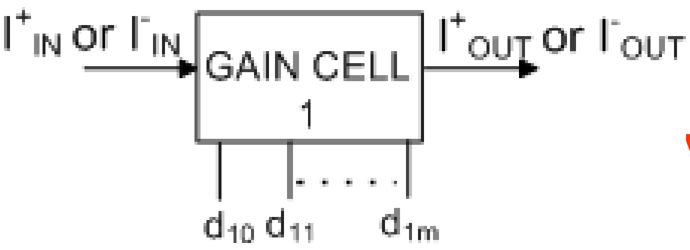
Gain Cell – Current Gain

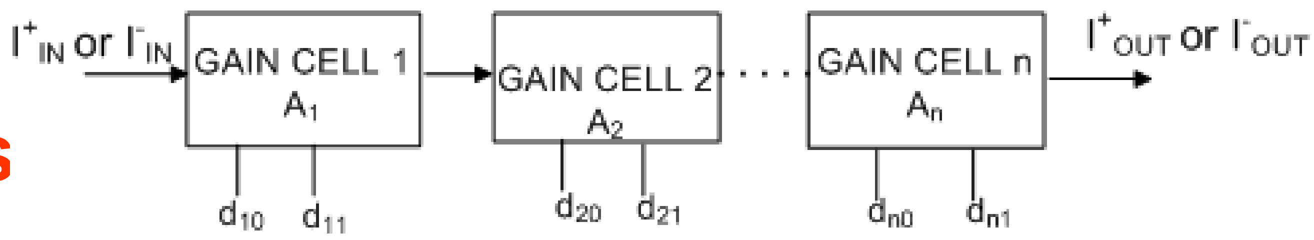


$$I_{out} = I_{In}(1+d_0+2d_1+4d_2+\ldots+2^m d_m) = 2^{(m+1)} = 6(m+1)\text{dB}$$

Gain Stage implementation

Single Cell Vs **Multi Cell**



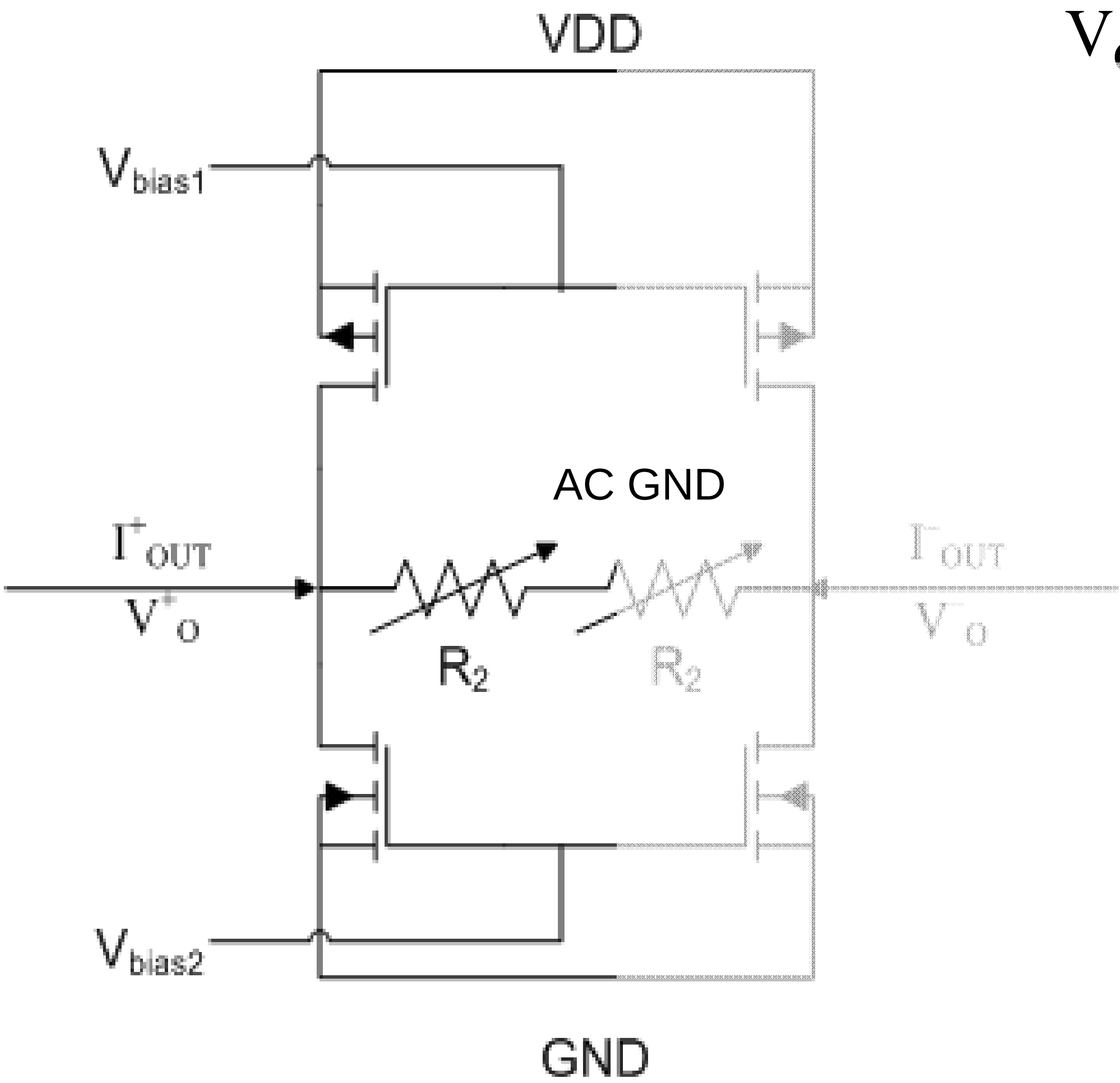


Advantages of multi cell implementation

- Low power Consumption
- Higher Bandwidth

Each d_n stage = 6 dB gain
2 d_n stages / cell (12 dB / cell)
4 Cells needed to achieve > 40 dB gain

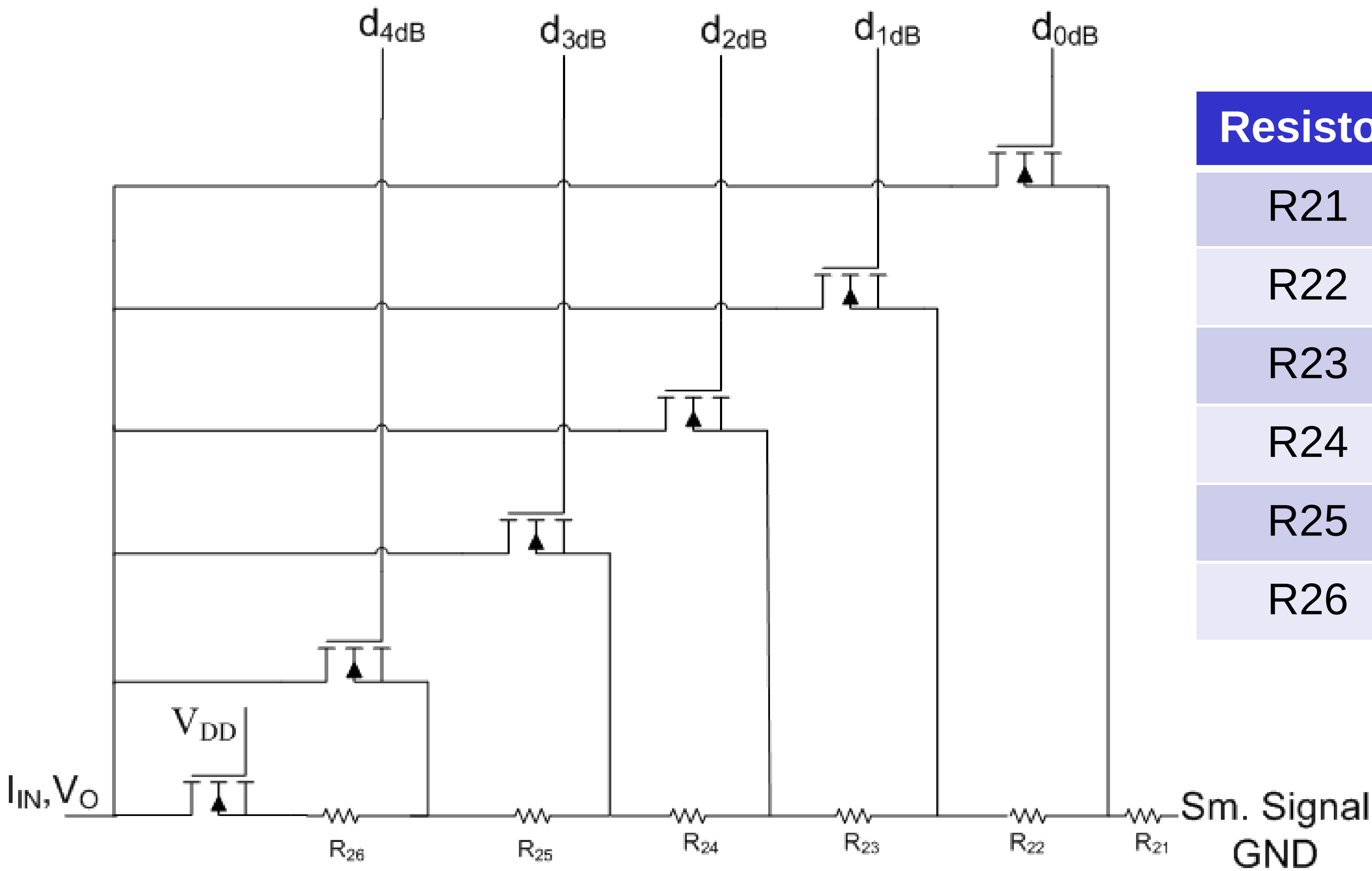
Output Stage (Current to Voltage)



$$V_{OD} = V_o^+ - V_o^-$$
$$= (I_{OUT}^+ - I_{OUT}^-)R_2$$
$$= I_{OD}R_2$$
$$= (-1)^n A_1 A_2 \ldots A_n V_{ID} R_2/R$$

Can fine tune gain by manipulating value of R2!!

Output Stage variable resistor for 1 dB fine control



Resistor	Value
R21	R*
R22	0.148 R
R23	0.168 R
R24	0.190 R
R25	0.225 R
R26	0.155 R

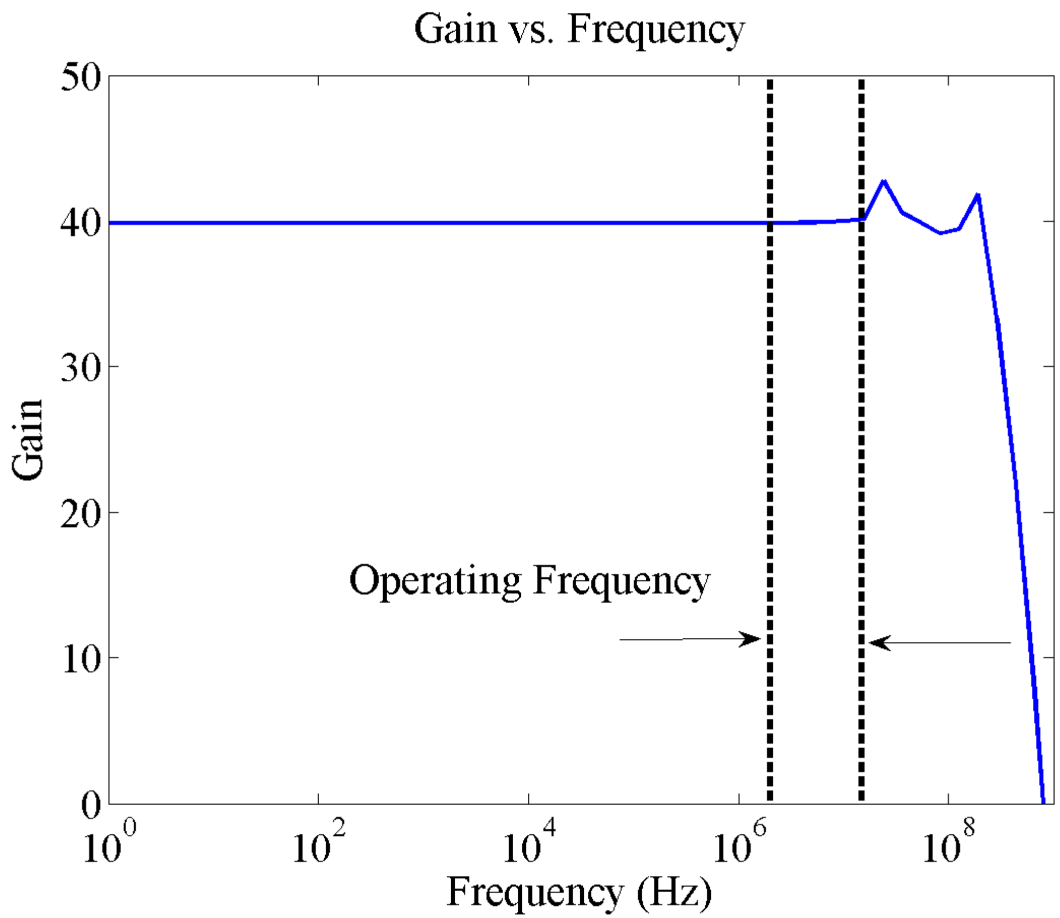
* R is the load resistor in the input stage

Results! Gain Accuracy

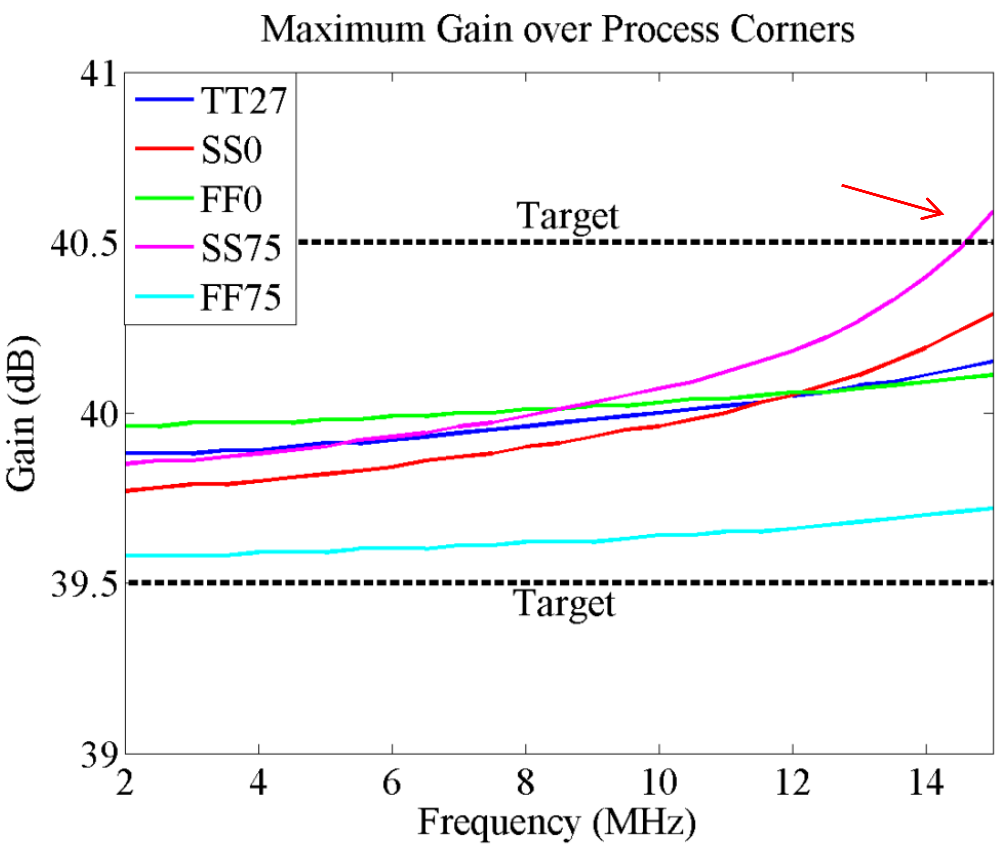
- Systematic variations due to resistor mismatches in fine-tuning stage

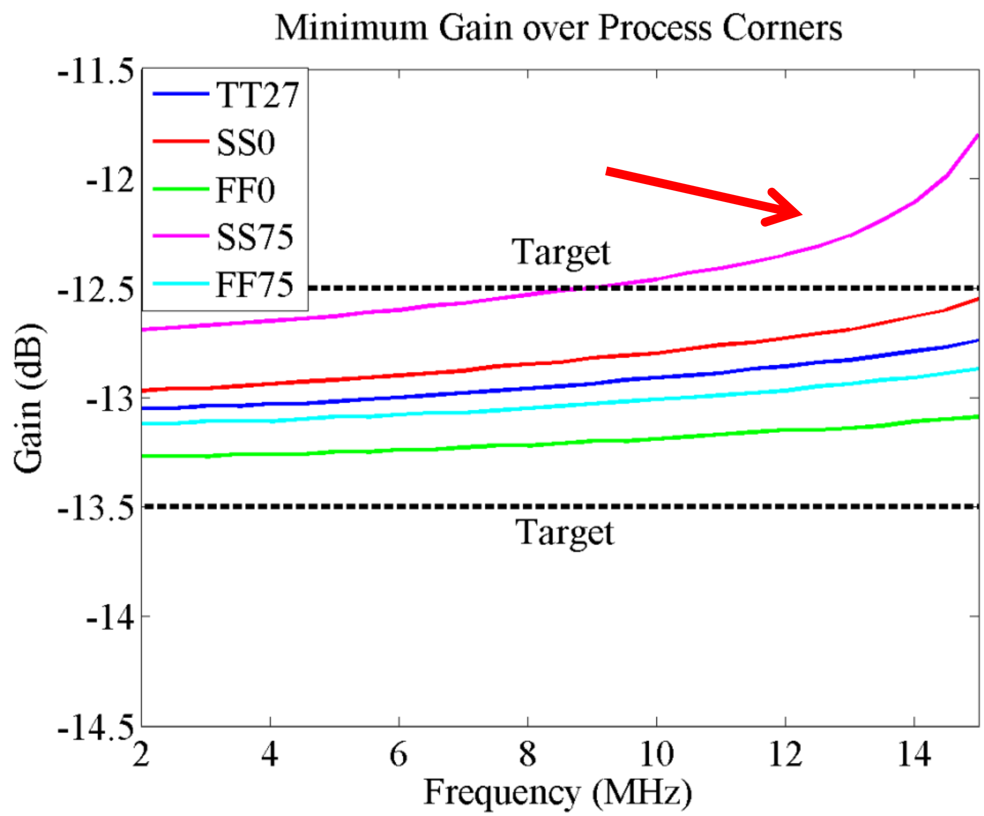
Results! Total Bandwidth

- Peaking caused by parasitic capacitances of bias points
- < 0.5 dB peaking in BW
- 3 dB peak @ ~25 MHz (BW = 2-15 MHz)



Results! Gain with Process Variations





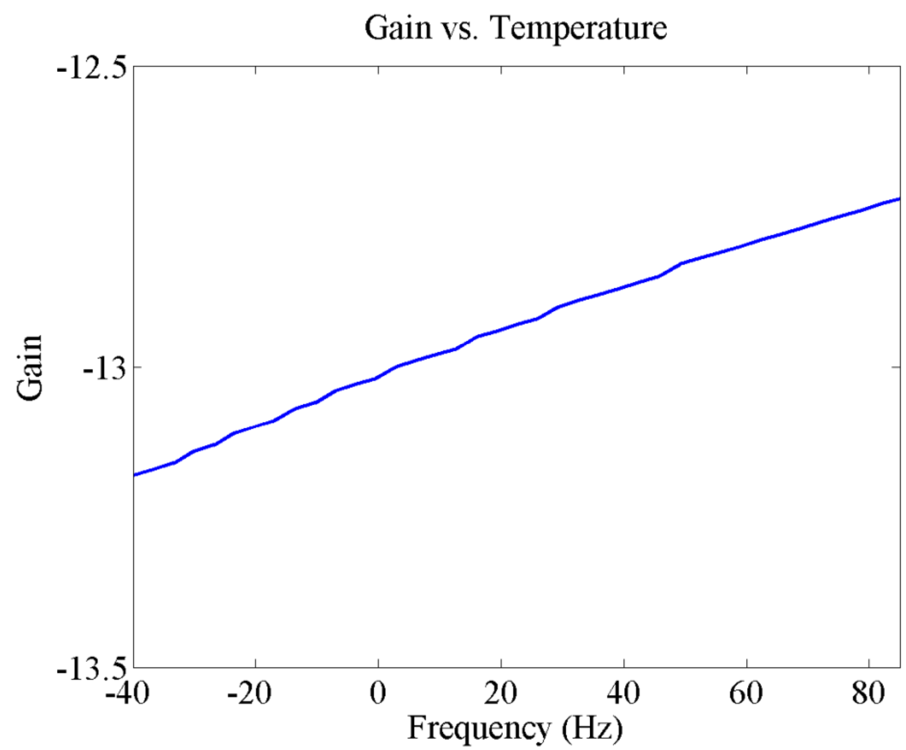
- Meet ± 0.5 dB accuracy at all corners except SS75
- ± 0.6 dB at max gain (40 dB)
- ± 1.2 dB at min gain (-13 dB)

Results! Summary and Comparison

Parameter	Specification	Design	MAX2037	Units
Power	<150	47.53	120	mW
Operating Range	2-15	2-15	< 29	MHz
Dynamic Range	40	53 (-13 to 40)	42 (-12.5 to 29.5)	dB
Gain Accuracy (over process corners)	±0.5 (±0.5)	±0.2 (±1.2)	±0.25 (±1.0)	dB
Reference Current	50±3%	50±2.4%	--	µA

•Tradeoff: Decrease gain to increase operating range

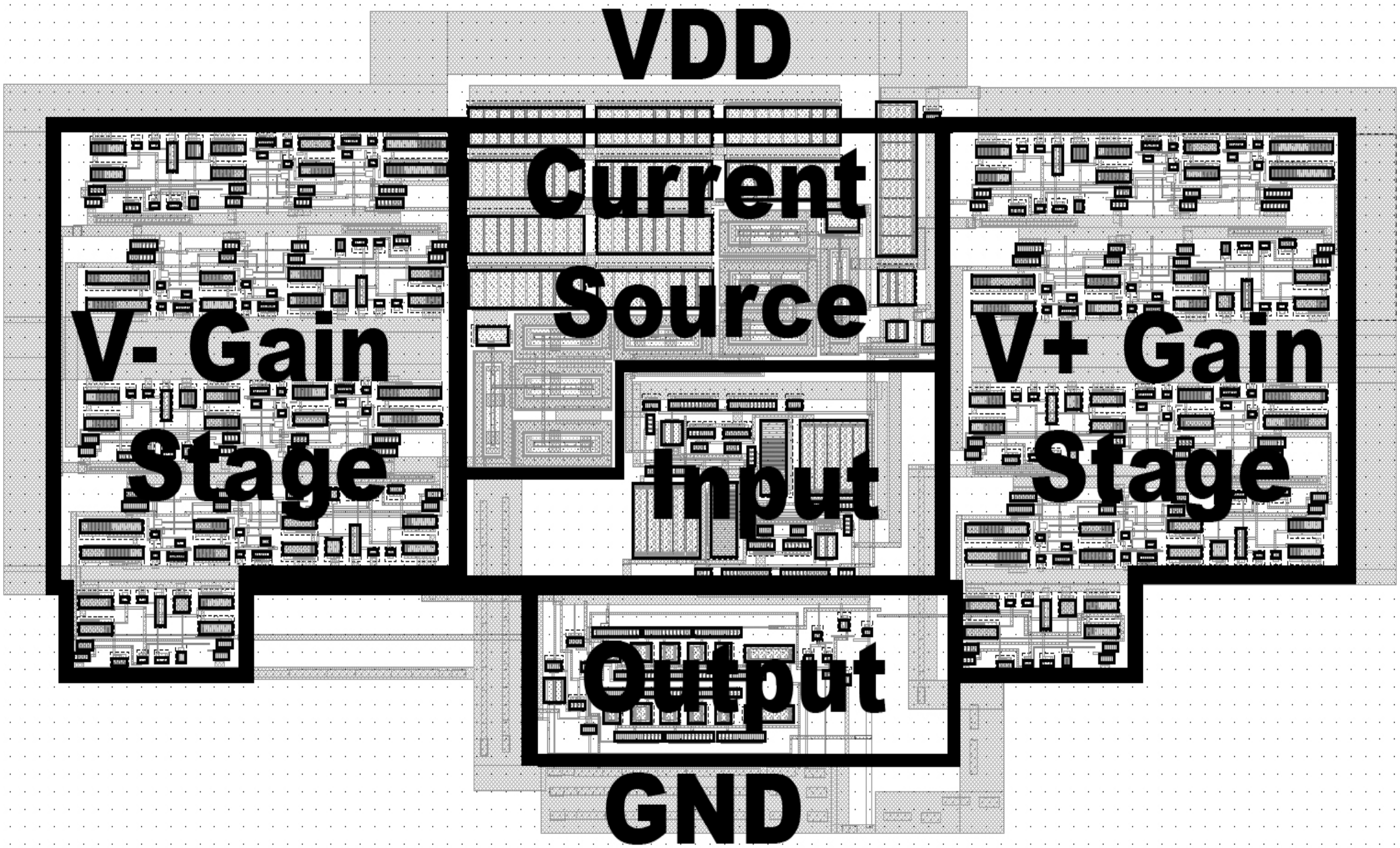
Bonus Footage: Gain Variations with Temperature



- Propagation modes are equal and attenuation constants have equal magnitude and opposite sign mnmnmn

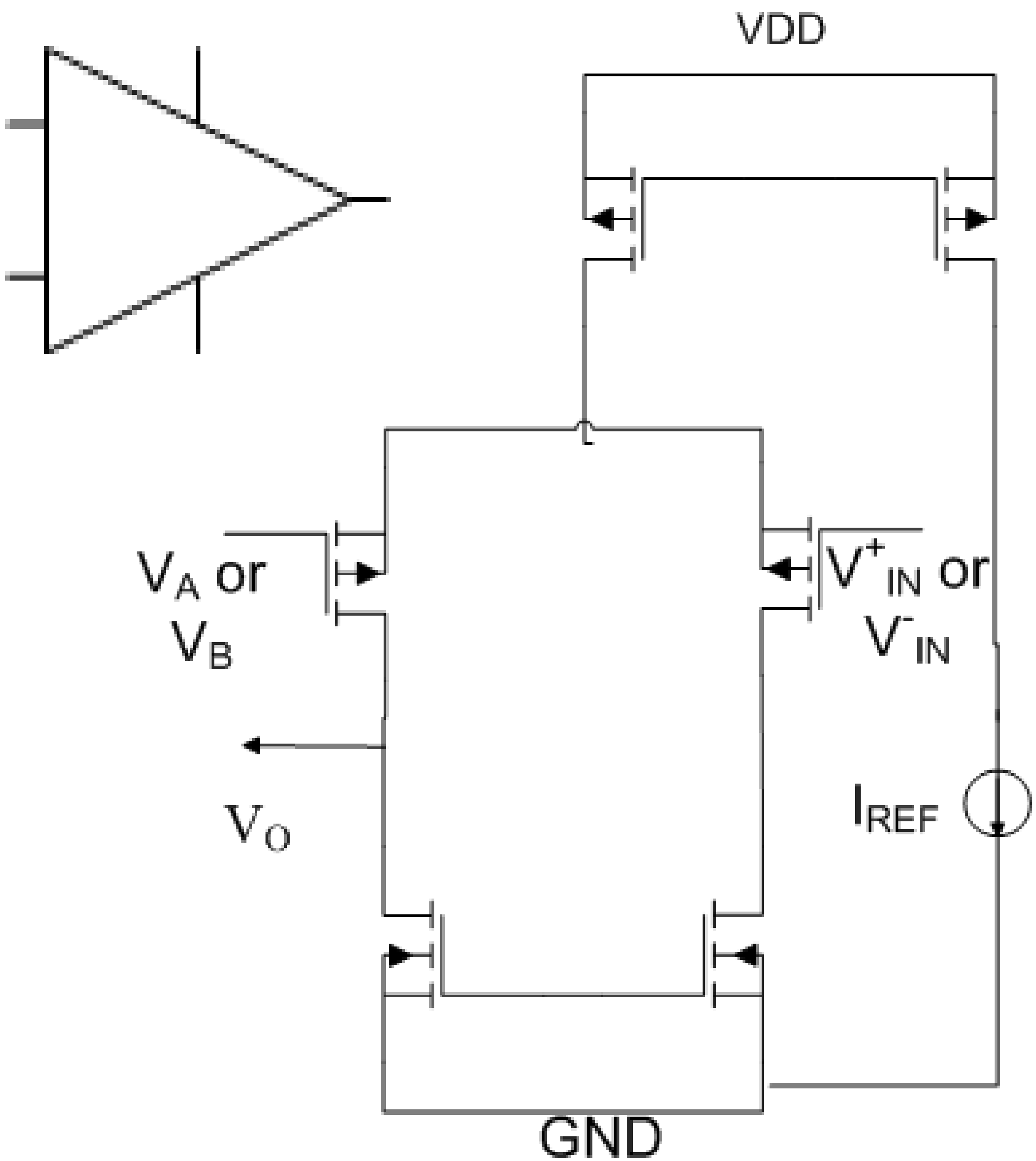
- Symmetric mode is cutoff.
- Anti-symmetric mode exhibits backward-wave behavior

Bonus Footage: Layout ahoy!



- Total size: 480 μm x 235 μm = .113 mm^2
- Rectangular(ish) in shape.

Bonus Footage: Feedback in Input Stage



- $A(s) \sim g_m(r_o/2)$
- $\beta=1$
- Loop gain $\sim g_m(r_o/2)$
- Phase margin ~134 deg
- Stable operation