Low Power Inter-Chip Wireless Communication Using Inductive Coupling and Monocycle Signaling

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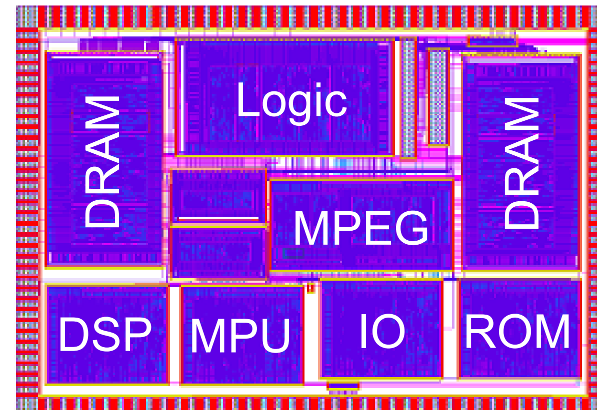
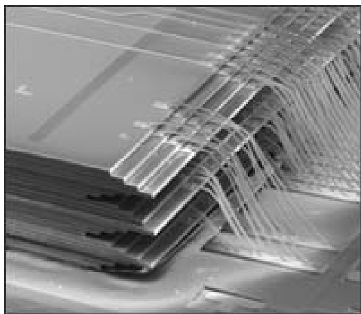
Introduction

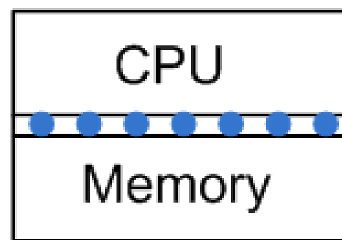
- System-on-a-chip
  - Much time to develop
  - Low yield (high cost)



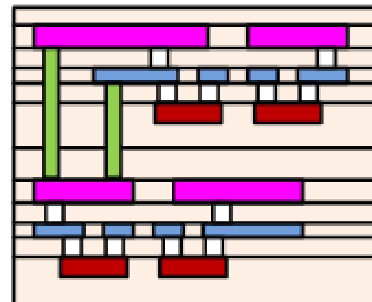
- System-in-a-package
  - Wired interconnection
  - Wireless interconnection



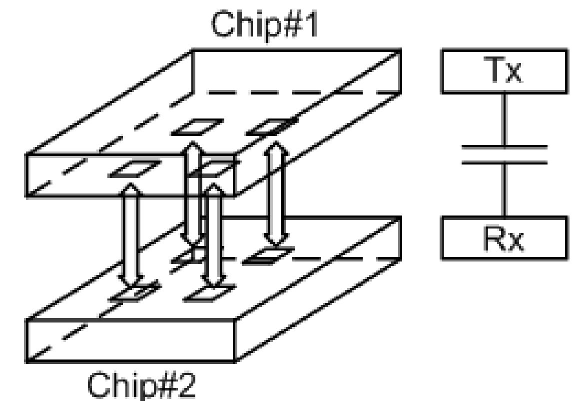
Wirebonding
(Courtesy: Hynix)



Micro-bump

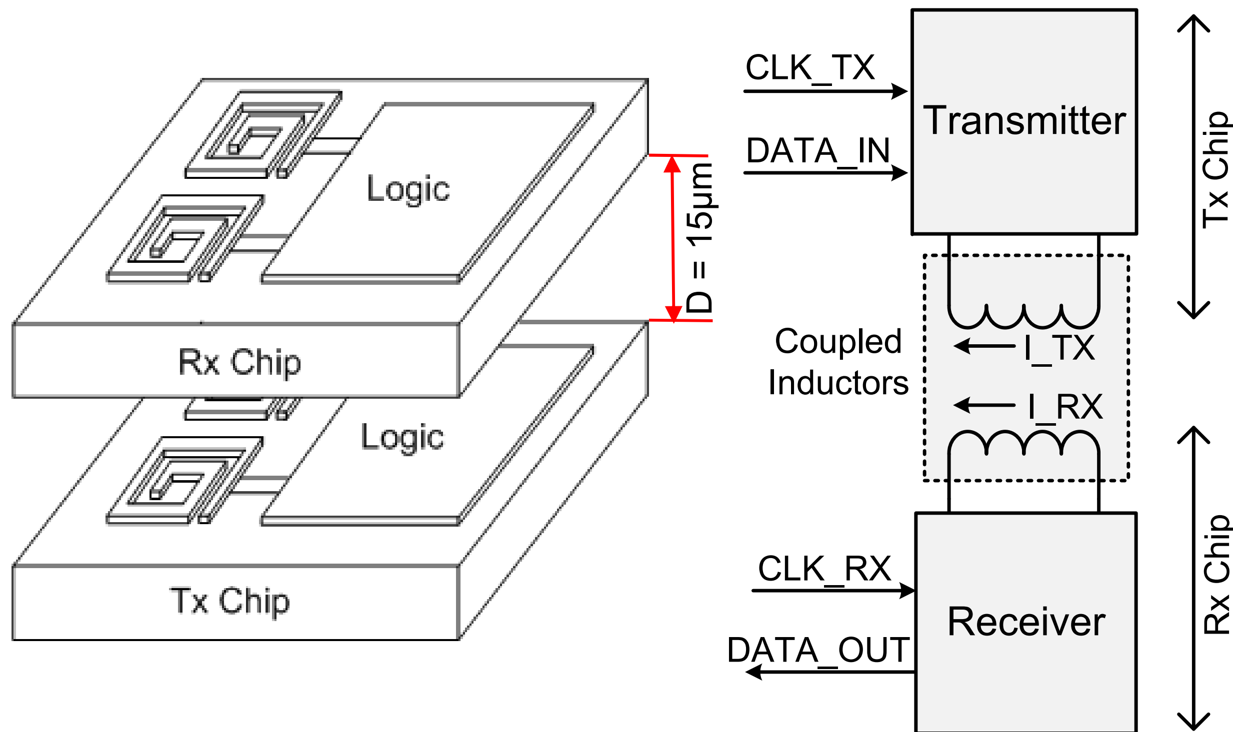


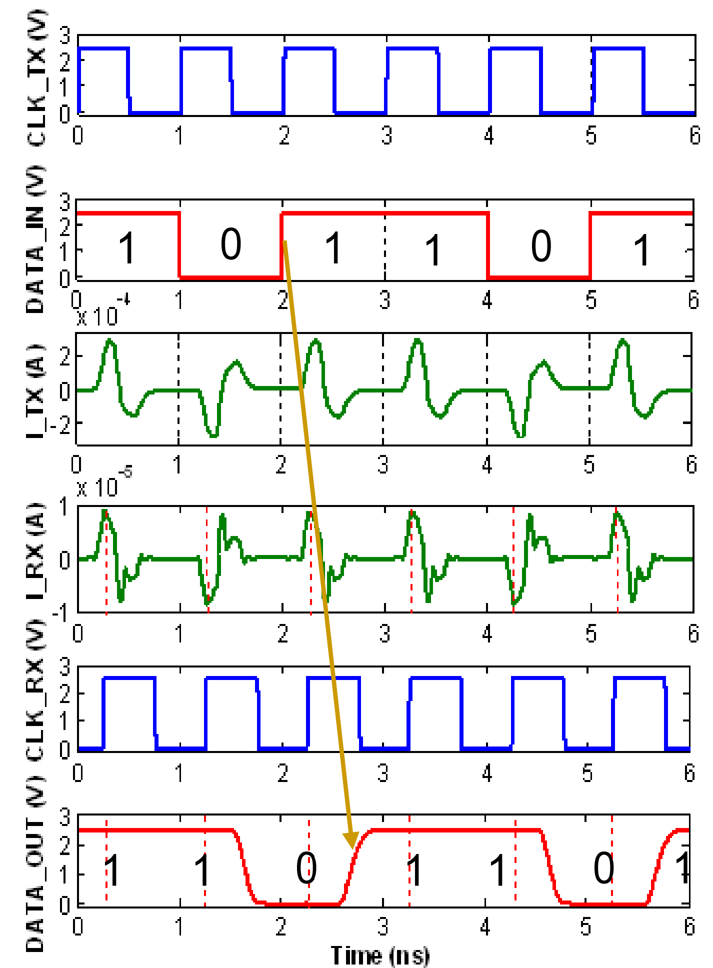
3D-via



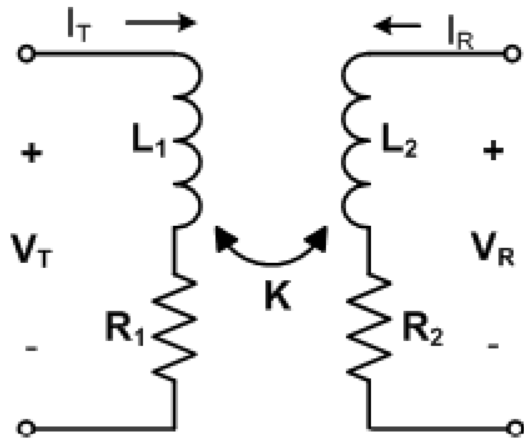
Capacitive coupling

Overall Design & Operation

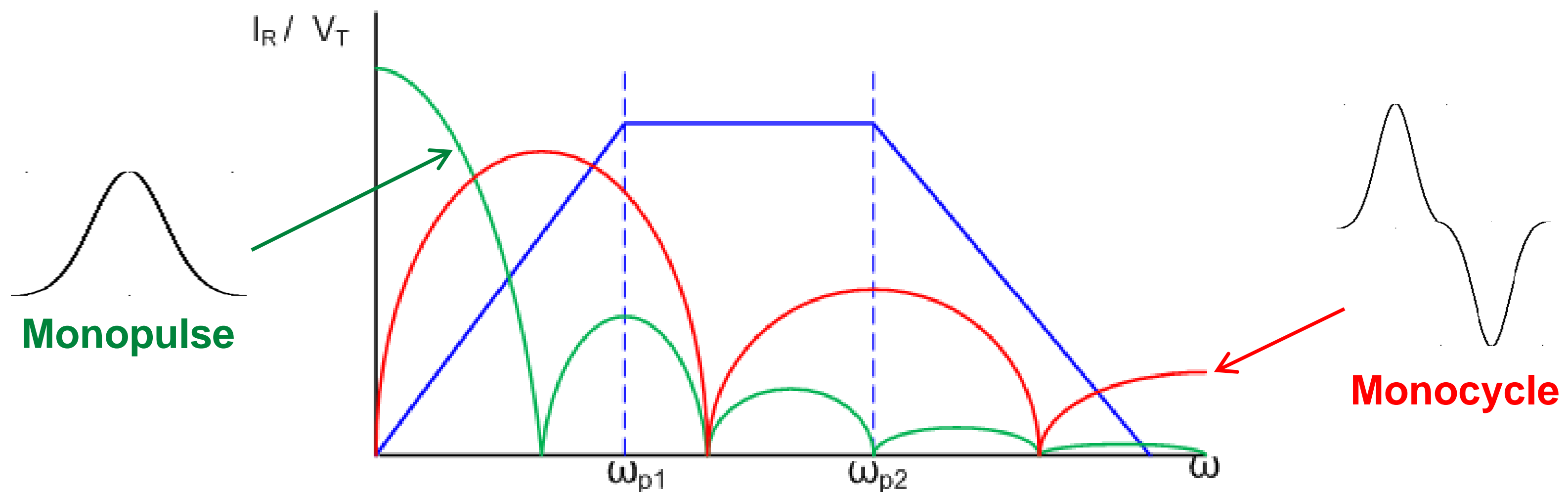




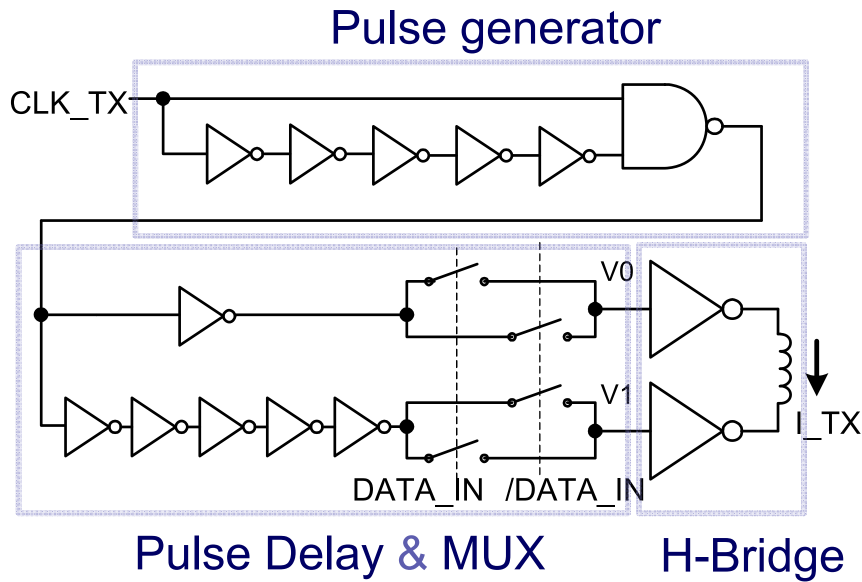
Monocycle Signaling

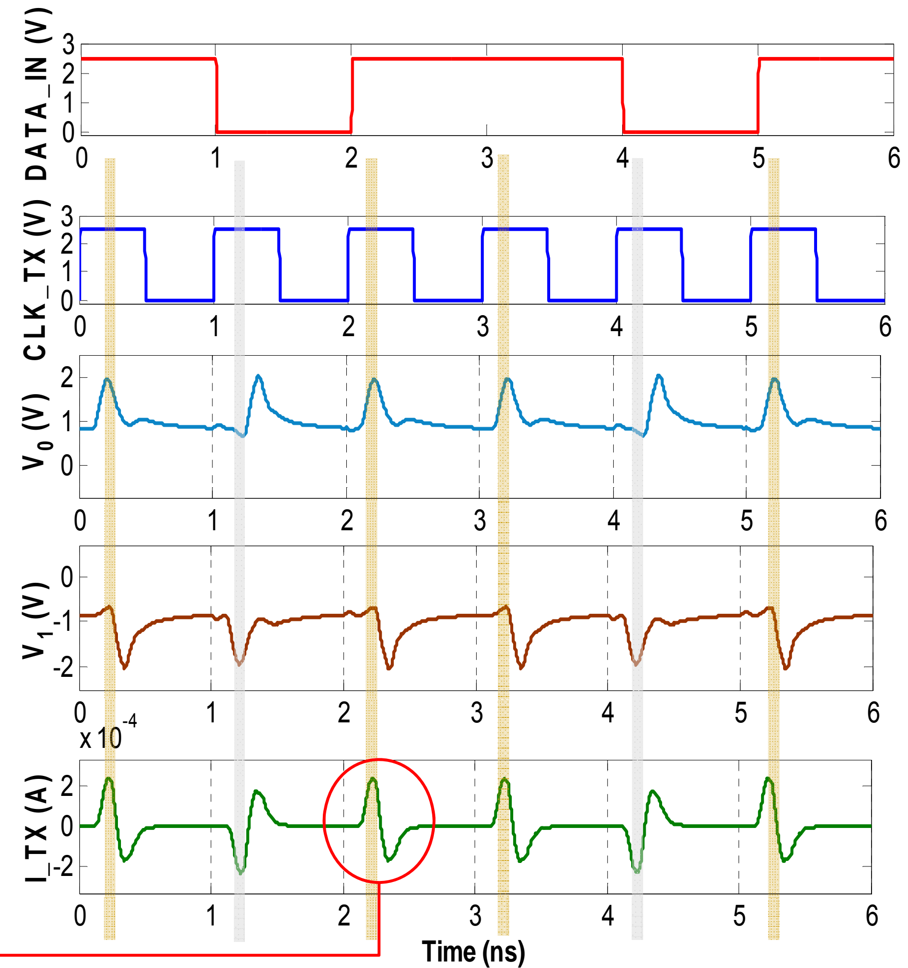


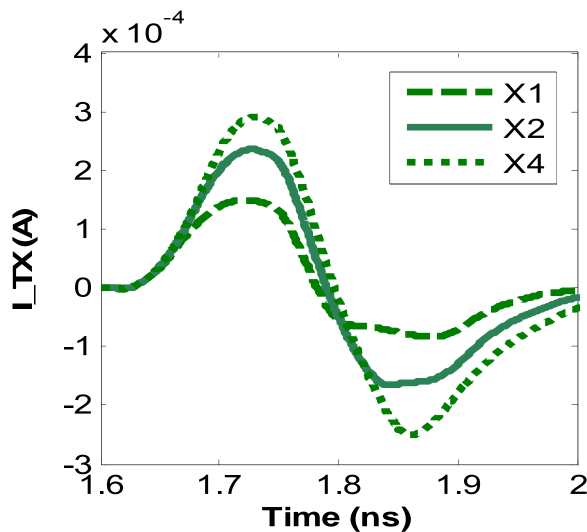
$$\frac{I_R}{V_T} = \frac{\omega k \sqrt{L_1 L_2}}{\sqrt{\left[R_1 R_2 - (1-k^2)\omega^2 L_1 L_2\right]^2 + \omega^2 (L_1 R_2 + R_1 L_2)^2}}$$



Transmitter Operation

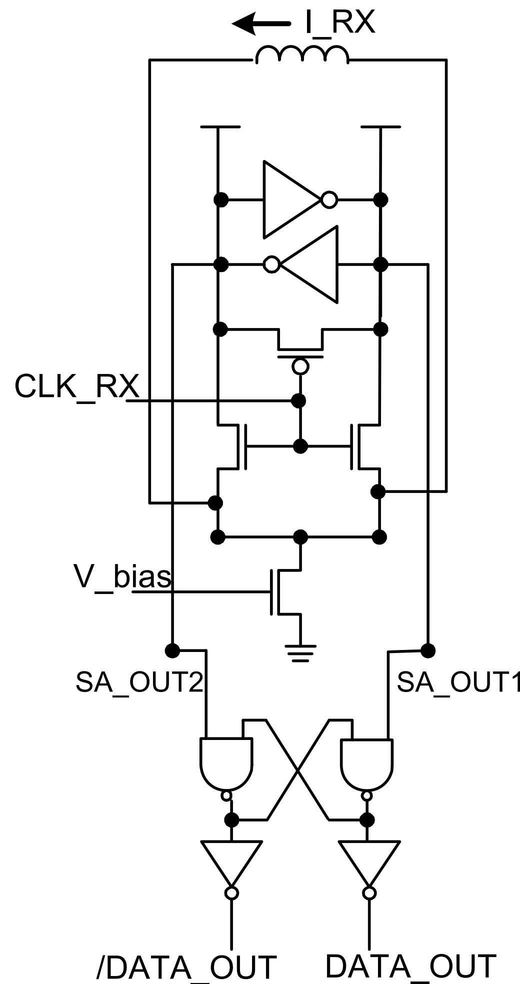


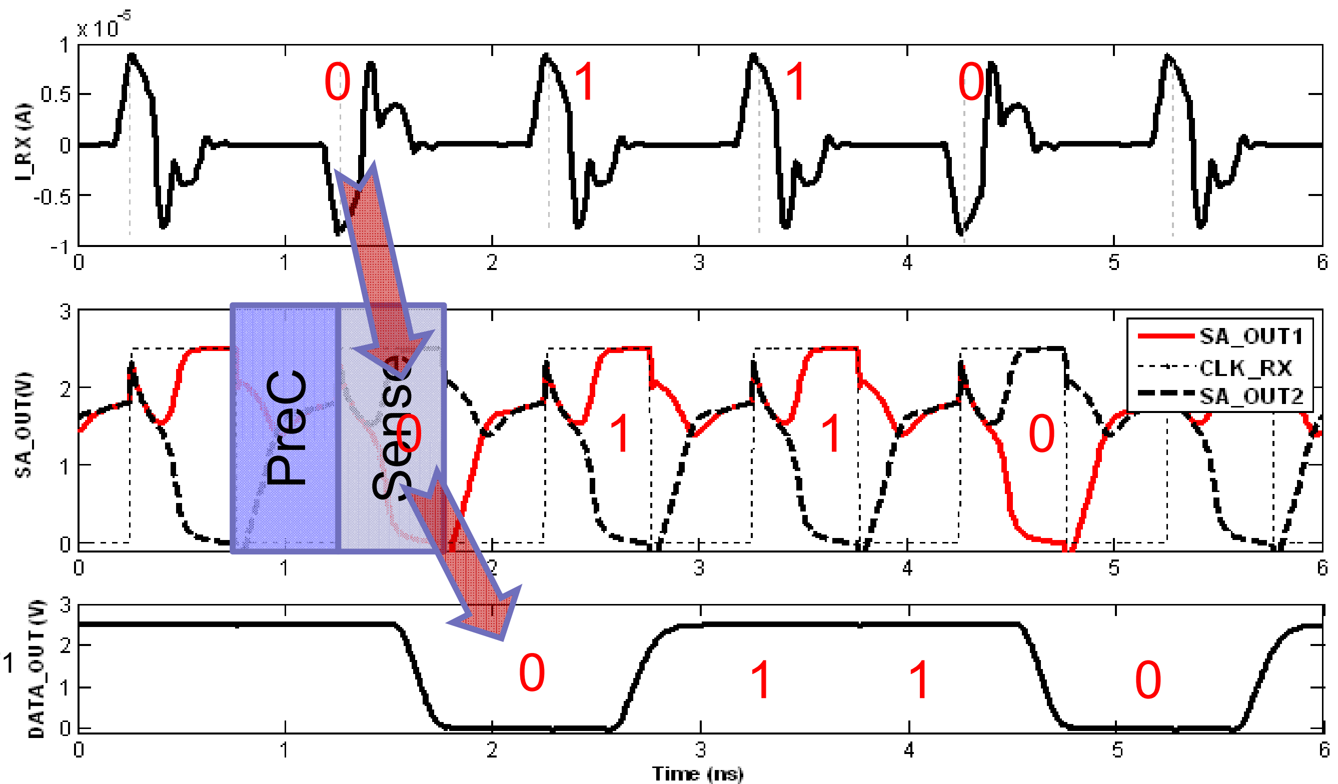




* **DATA_IN** pulse train is pseudo-randomly generated by Perl script

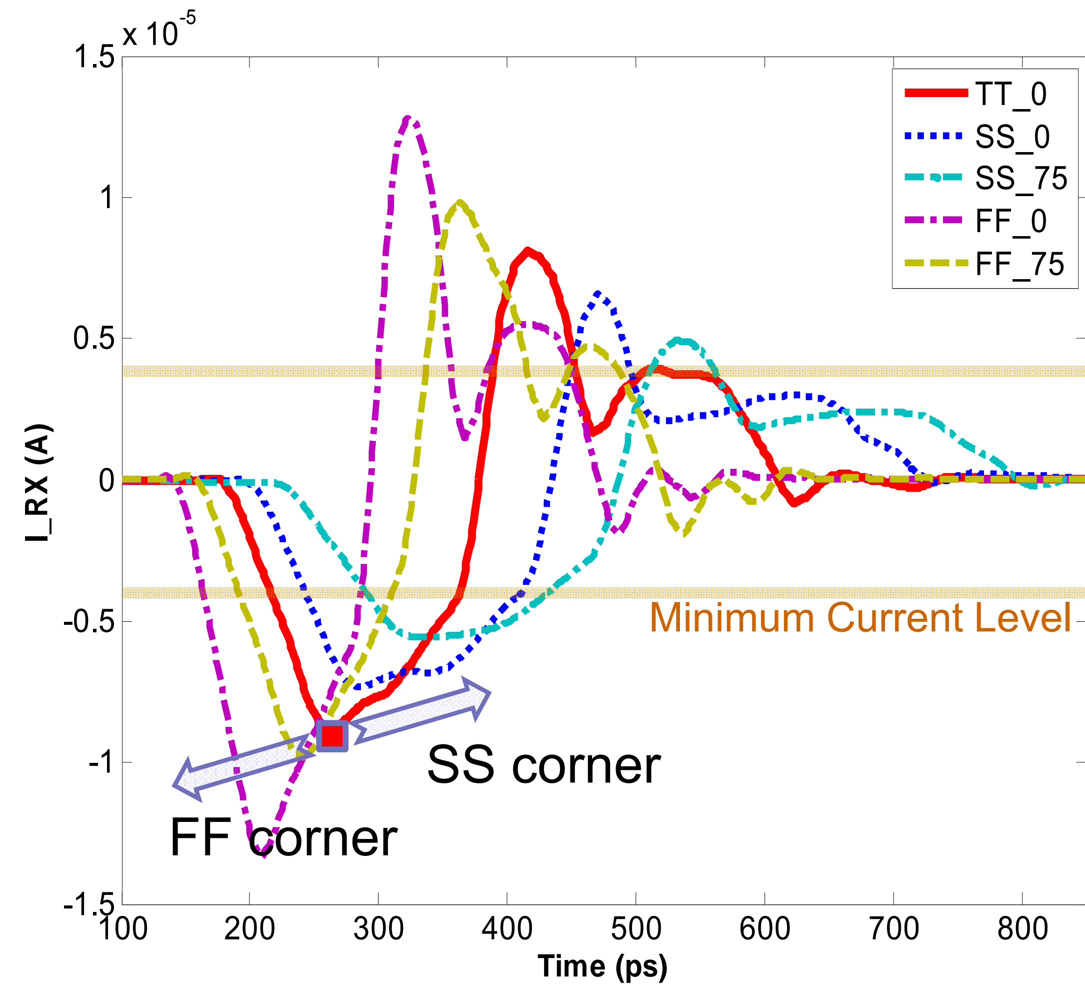
Receiver Operation

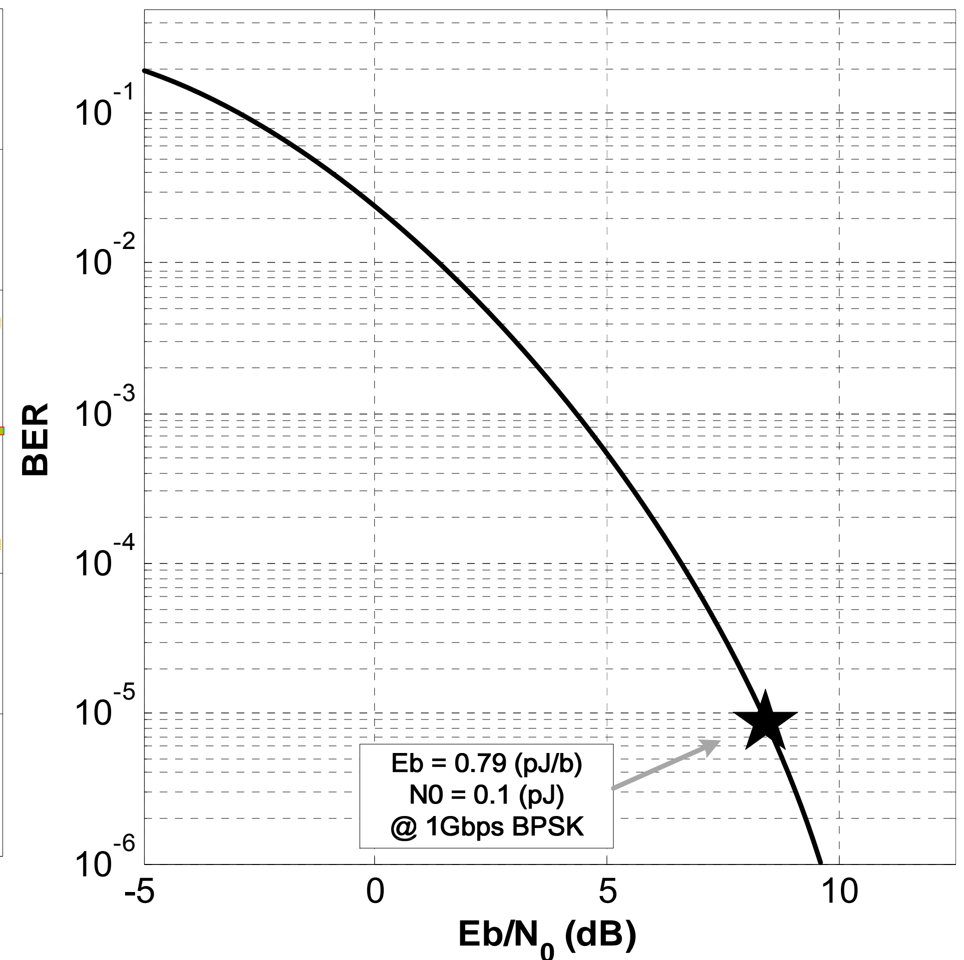




- Sensing delay : 230 ps
- Overall receiver delay :400 ps
- Min. pulse width for I_RX: 150ps

Corner simulation and BER

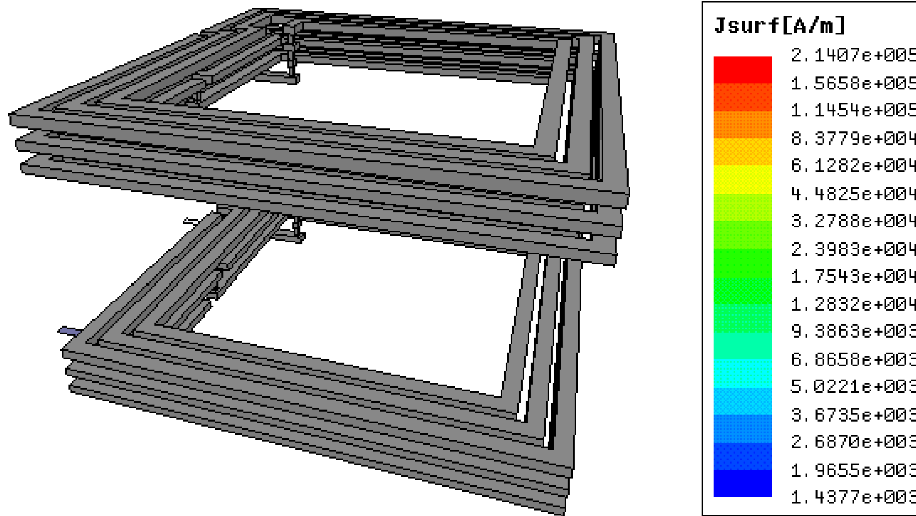




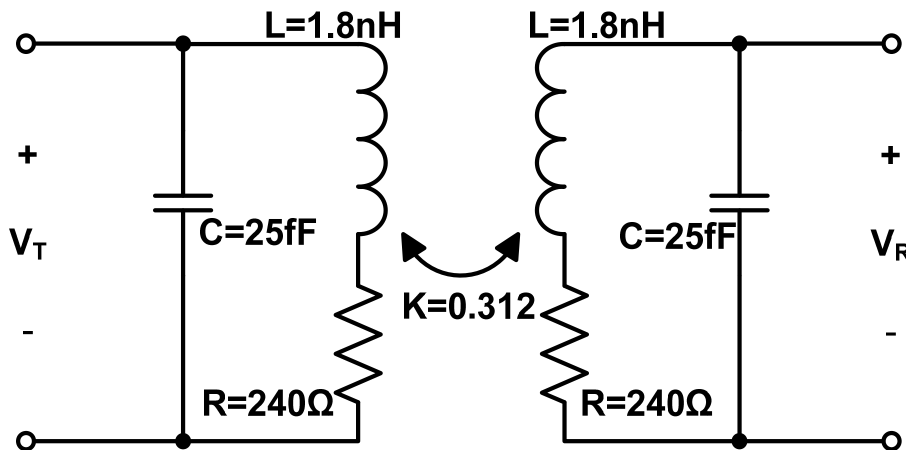
Corner simulation

Bit error rate

Coupled Inductors

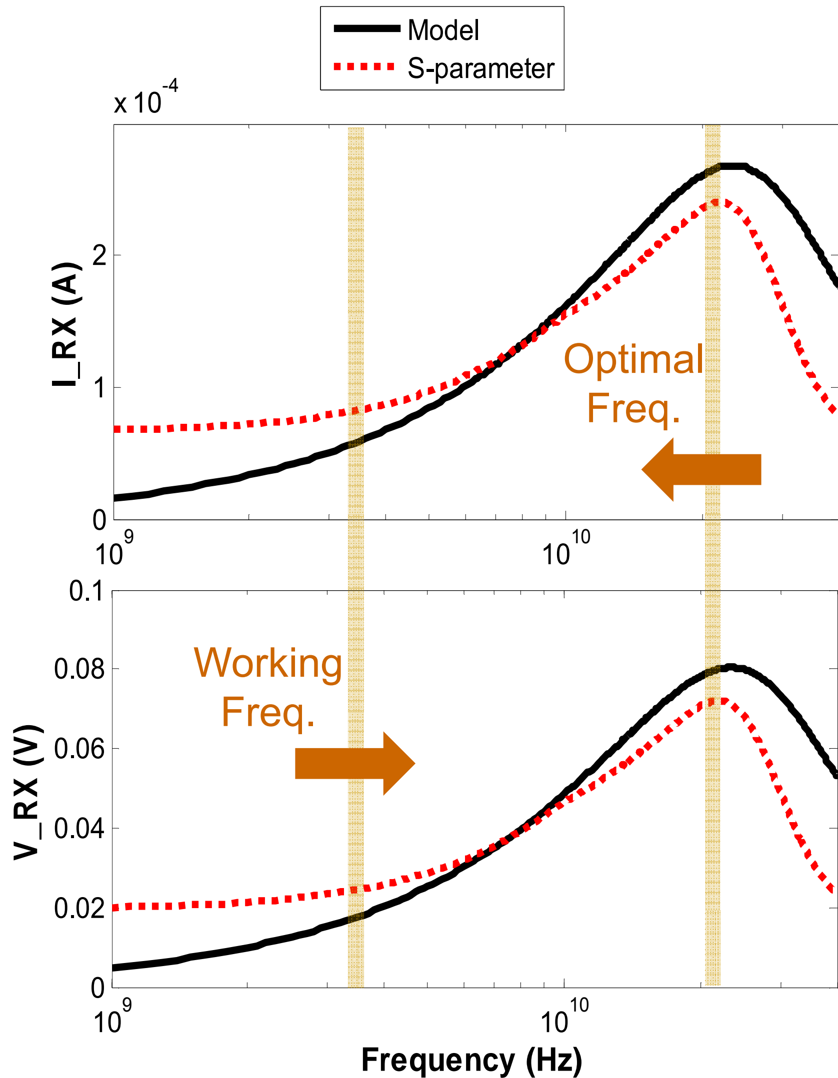


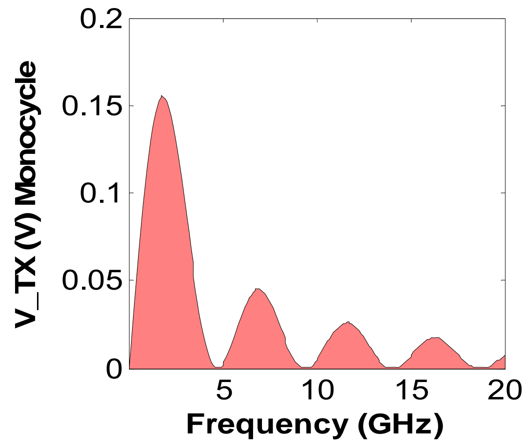
Layout Parameter	Value
Distance (d)	15μm
Wire Width (w)	1μm
Wire Space (s)	0.5μm
Diameter (l)	20μm
Turn (n)	3
Layer (m)	3

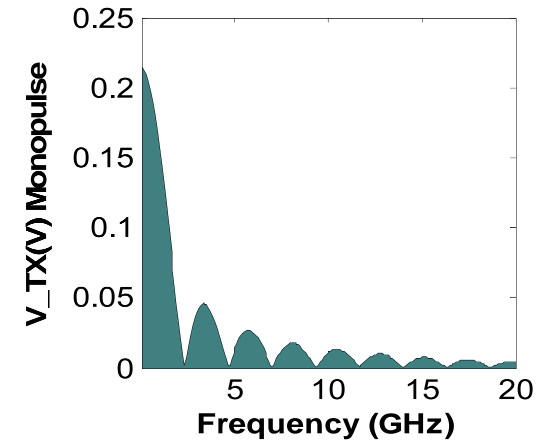


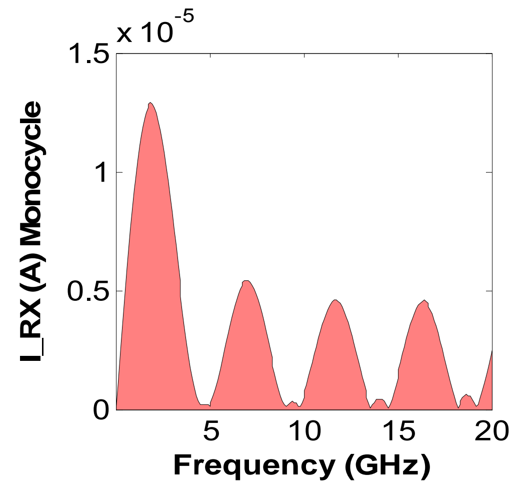
Extracted Parameters	Value
L	1.8nH
R	240Ω
C	25fF
k	0.312
M	0.542nH

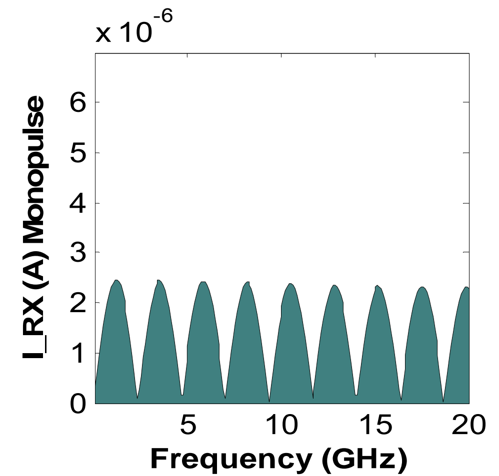
Frequency Analysis



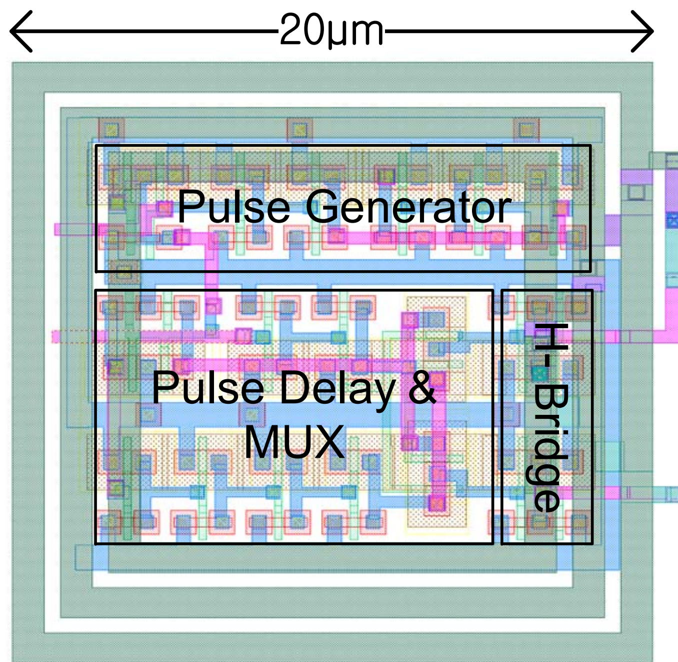




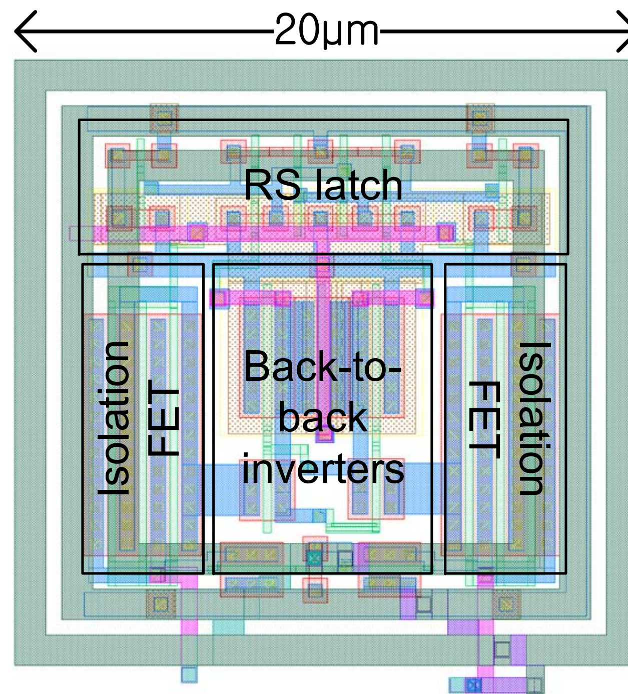




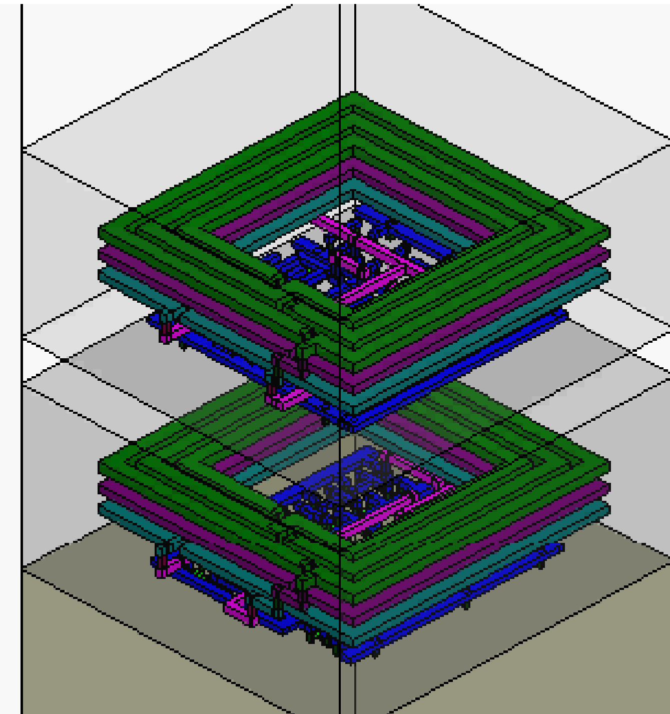
Layout



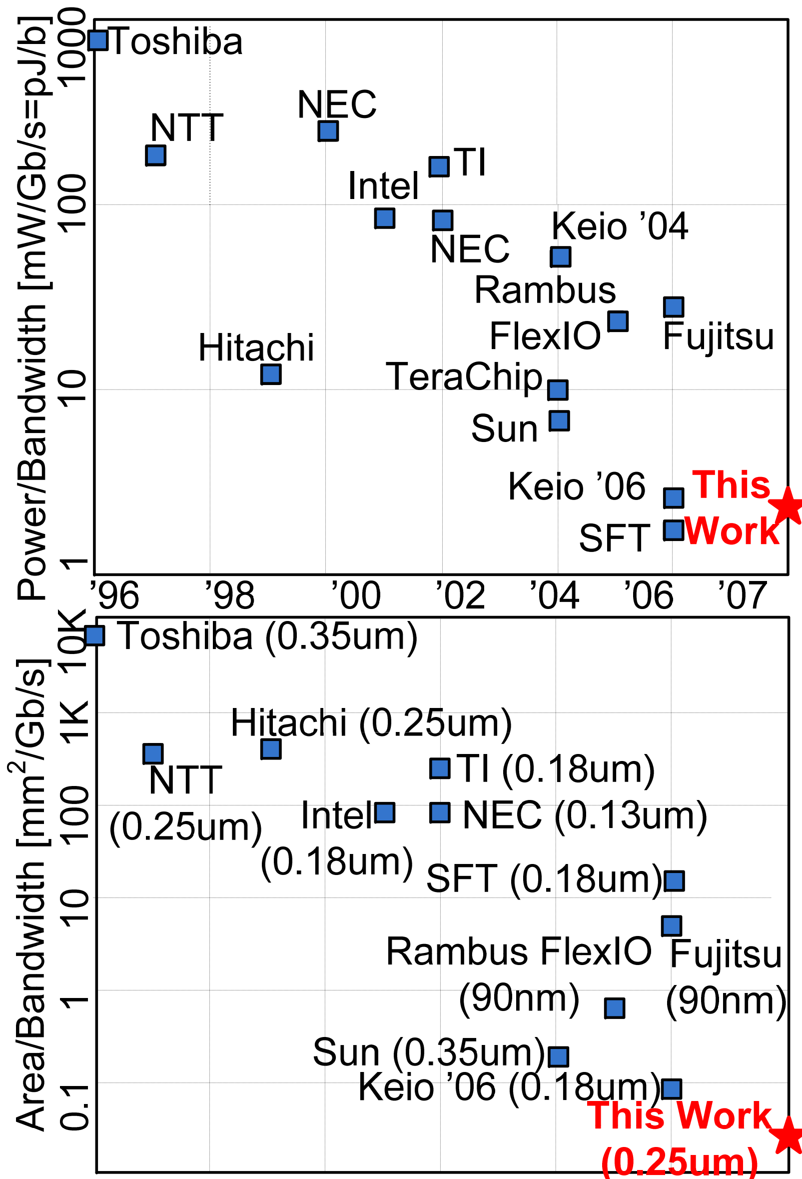
(a) Transmitter



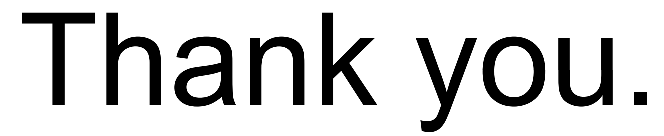
(b) Receiver



Performance



Parameter	Value
Channel Bandwidth	1Gb/s
Channel Pitch	20μm
Power Dissipation	2.18mW
-Transmitter	0.87mW
-Receiver	1.31mW
Total Area	400μm^2
Power/Bandwidth	2.18mW/Gb/s
Area/Bandwidth	400μm^2/Gb/s
LVS & DRC	clean


Thank you.