Class D High Power Audio Amplifier

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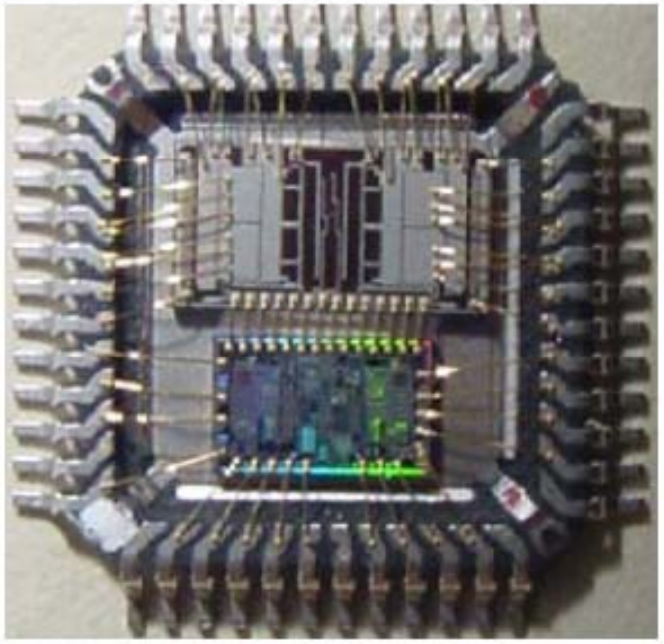
Motivation

- Why Class D?
- Class D Features
  - Switching Amplifier
  - Pulse Width Modulation (PWM)
- High Power / High Efficiency
- Driver for speakers and headphones
- Portable Audio Applications
  - Cell Phones, PDAs, GPS



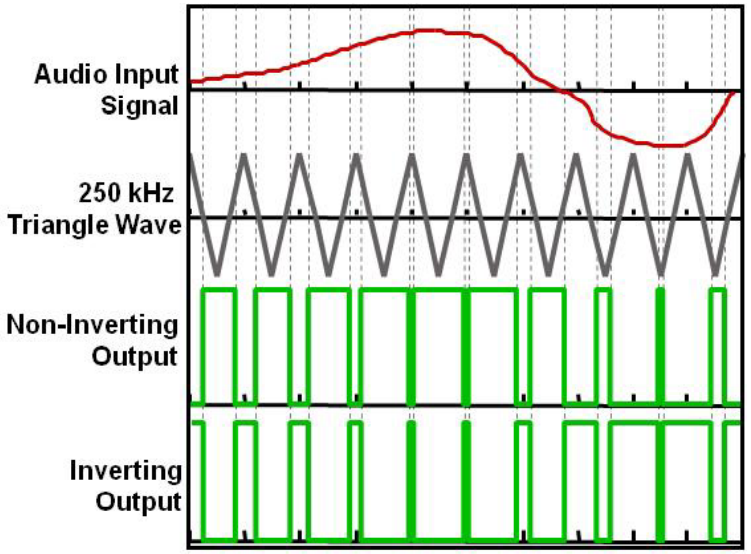
Texas Instruments Class D Amplifier

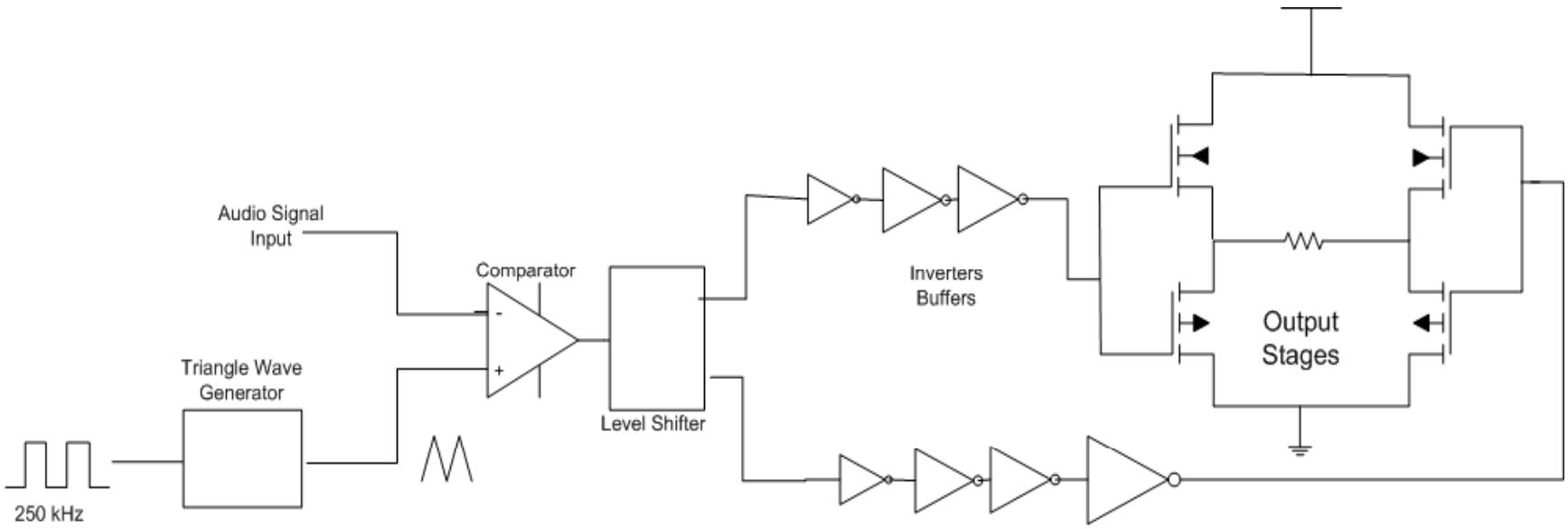
Design Goals

- Peak Output Power ≥ 1 Watt
- Efficiency ≥ 85 %
- THD ≤ 0.5 %
- Bandwidth = 20 Hz to 20 kHz
- Maximum Input Swing = 2.5 Vppk
- Maximum Output Swing = 5 Vppk
- Power Dissipation = 75 to 150 mWatts

System Overview

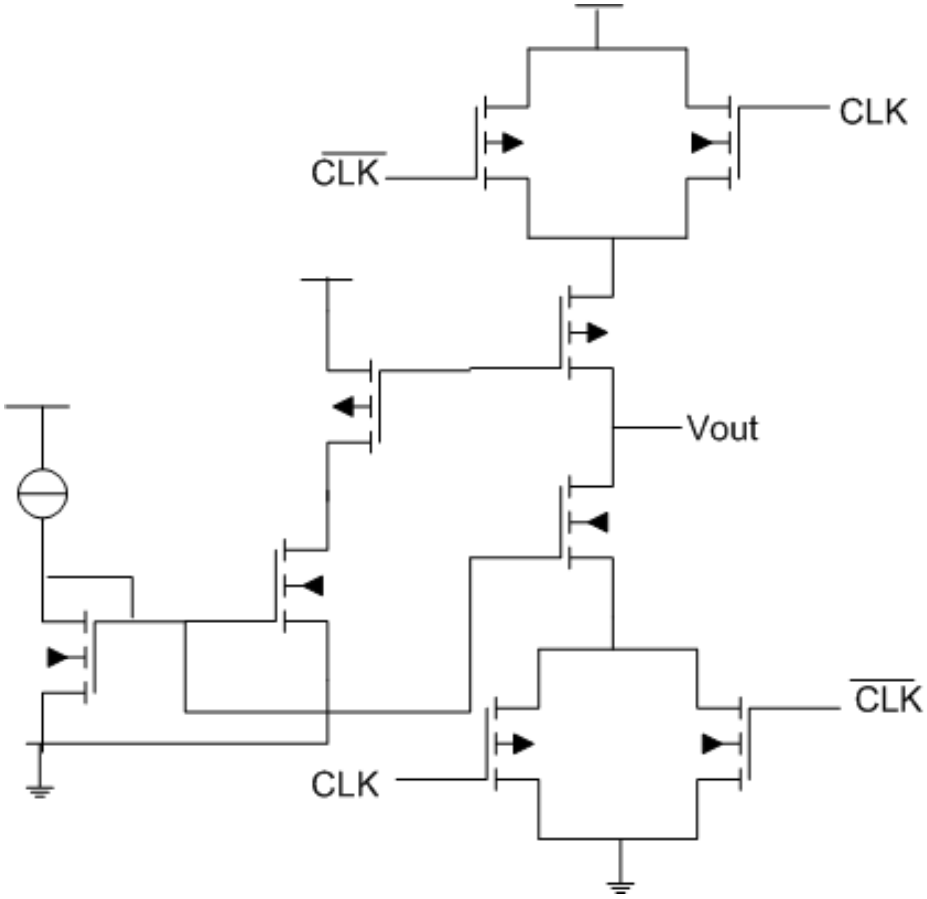
- Triangle Wave Generator
- Comparator
- Level Shifter
- Output Stages





Triangle Wave Generator

- V_{IN} = 250kHz squarewave CLK
- System of Current Mirrors
- Output Mirrors acting as Push-Pull Architecture
- Slew Rate to linearize V_{rise} & V_{fall}
- Transmission Gates to switch between charge / discharge



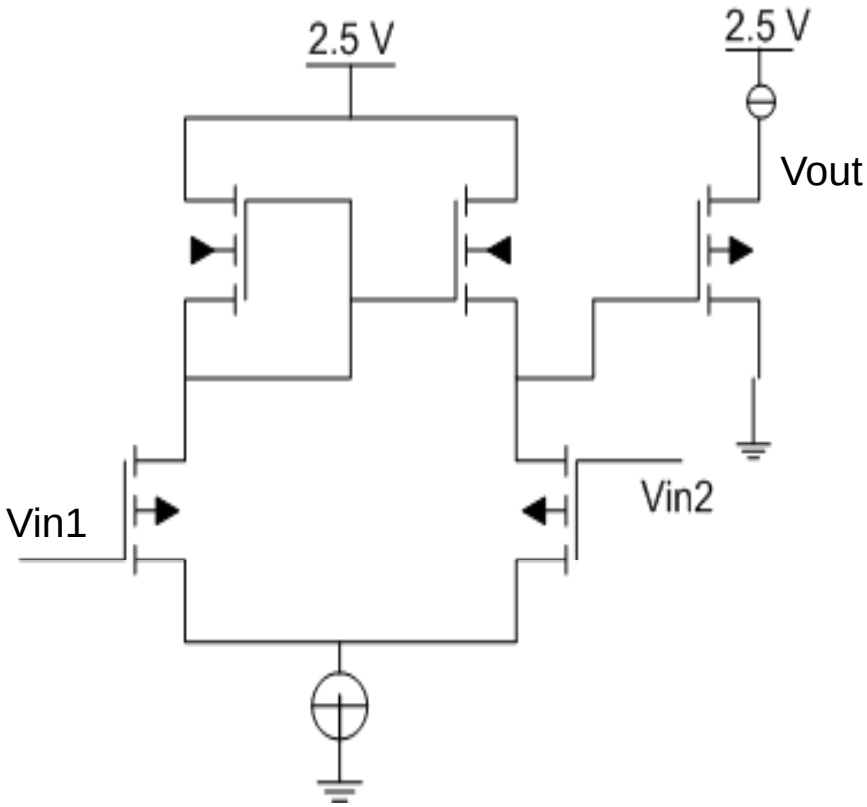
$$I_{SS} = I_C = C\ dv/dt$$

Comparator

- Multiple Potential Architectures
  - One / Two Stage
  - Telescopic / Folded Cascode
  - Gain Boosting
- Two stage design selected
  - High Gain
  - MHz range Bandwidth
  - Average Power Consumption
- Trade off between Gain – BW

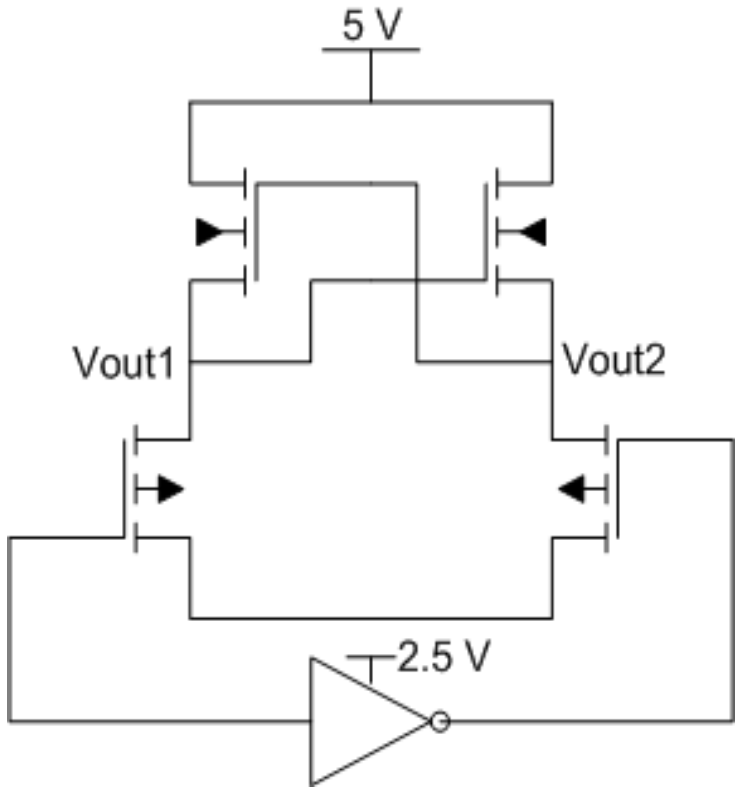
$$A_v = -g_m(r_{01}//r_{02}) \propto I_D^{-\frac{1}{2}}$$

$$r_0 = \frac{1}{\lambda I_D} \propto L$$

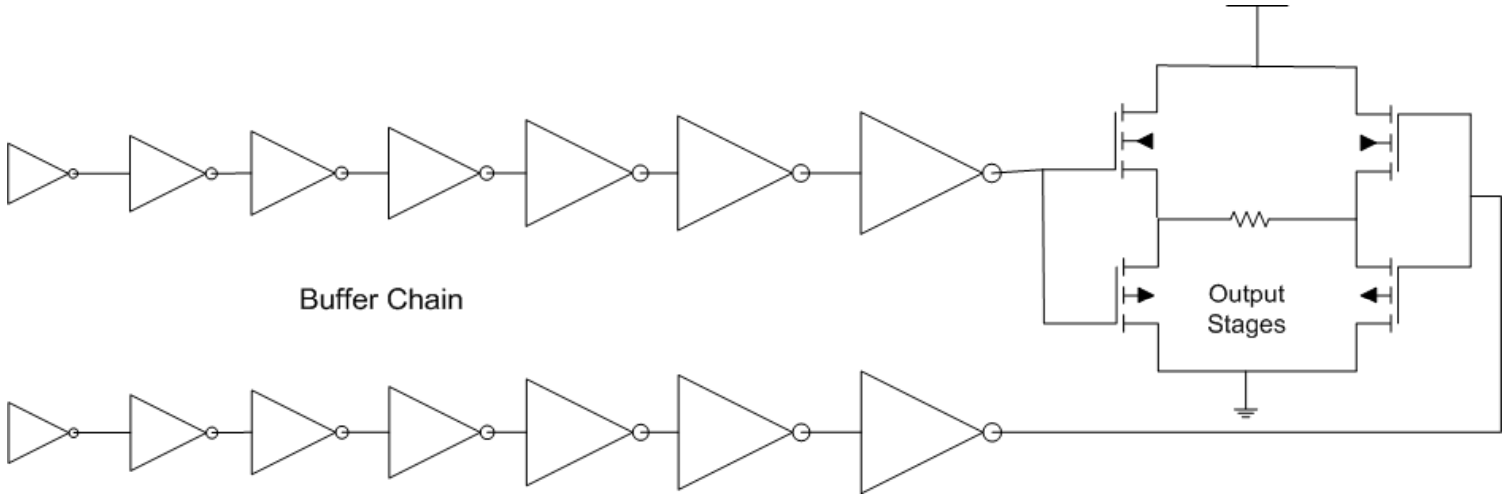


Level Shifter

- High Speed Architecture
- SE Input, Double-Ended Output
- High Dynamic Shift
- Delay ~ picoseconds
- Inverters sized for equal transitions



Output Buffer Stages

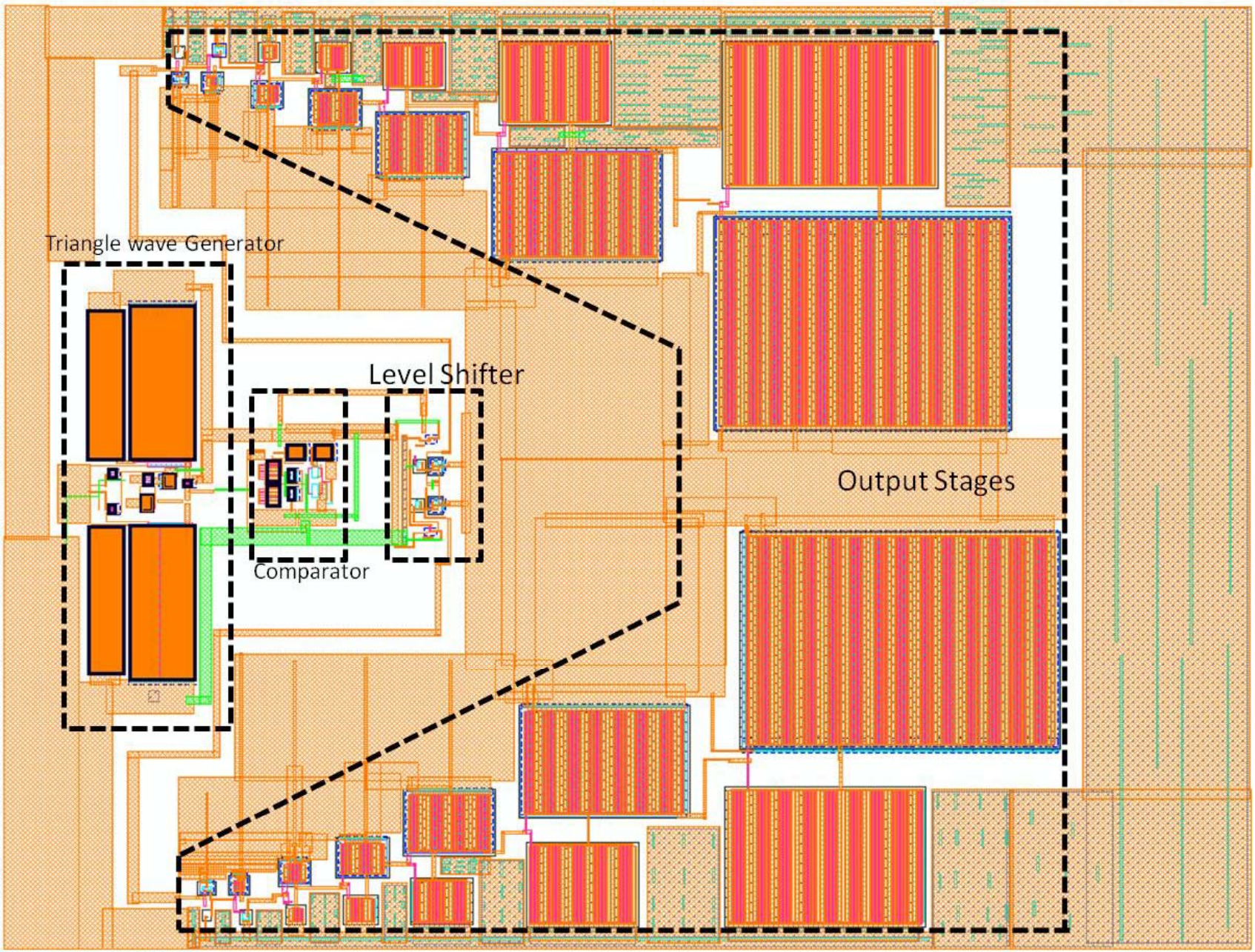


- PWM Speaker Drivers
- Inverter Chain
  - Lowest Cross Conduction
  - Minimum and equal Rise / Fall Times
  - Minimum Delay
- BTL – 2x the voltage swing

$$F = {C_{out}}/{C_{in}}$$

$$N = \frac{\log(F)}{\log(f_{opt})} \quad with \quad f_{opt} = 3.6$$

Layout


Triangle wave Generator
Level Shifter
Comparator
Output Stages

Results

Table 1: System Results

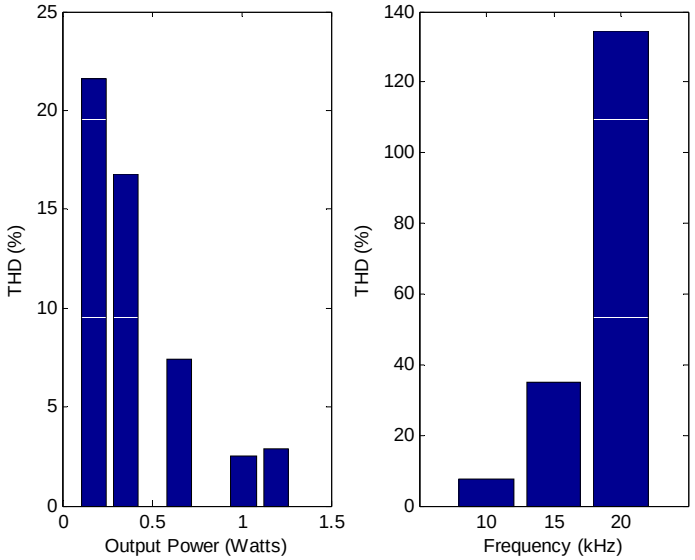
Table 2: Temperature Variation

$$THD\ (\%) = \frac{P_2 + P_3 + P_4 + \ \ldots P_N}{P_1}$$

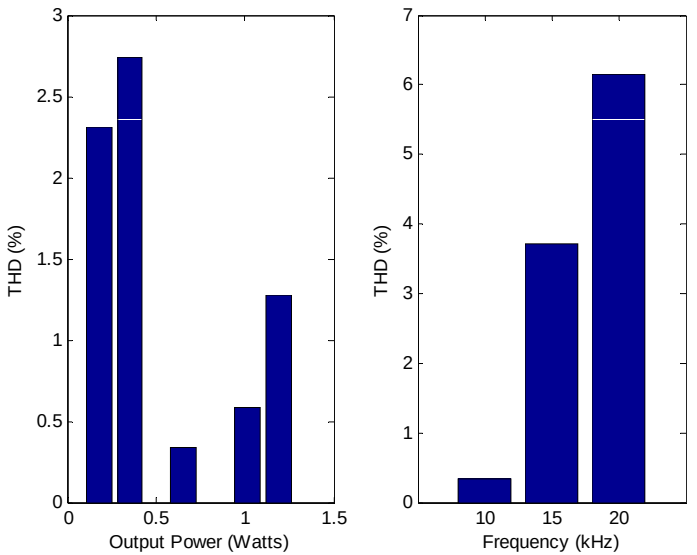
$$where\ P_1 is\ at\ the\ audio\ frequency$$

$$Eff.(\%) = \frac{P_{LOAD}}{V_{dd\,2.5} * I_{dd\,2.5} + V_{dd\,5} * I_{dd\,5}}$$

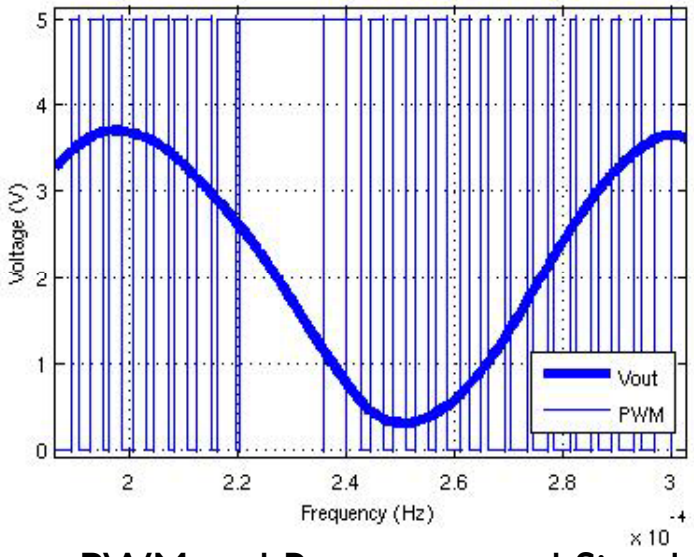
Results (cont.)



THD Analysis with DC Offset



THD Analysis with out DC Offset



PWM and Reconstructed Signal

Design Challenges

- Designing for two supply rails
  - How to Level Shift?
- Triangle Wave Generator sizing
  - Intricate tweaking to minimize nonlinearity in the slewing
- Input Pre-Amplifier
  - DC bias matching and high voltage swing
- Comparator Sizing
  - Gain bandwidth compromises
- Simulation Time
  - CAEN disk quota restrictions

Questions

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