Temperature Compensated Logarithmic Amplifier for CMOS Image Sensor

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Logarithmic Amplifier

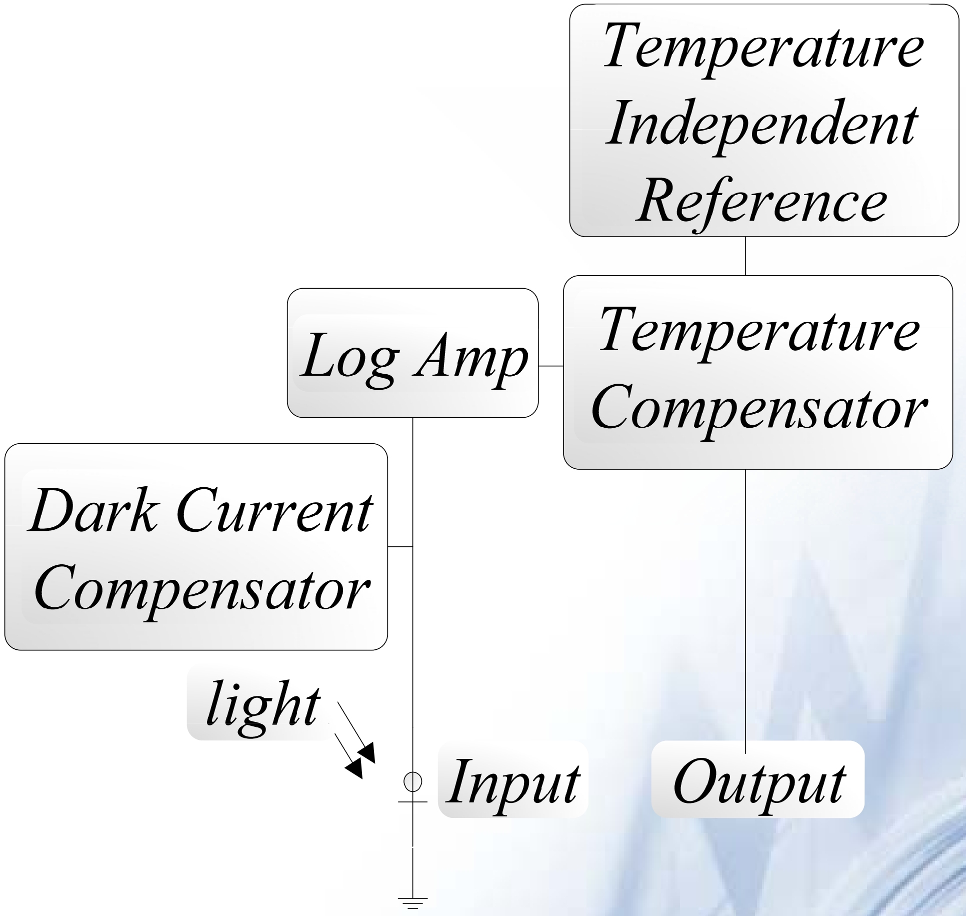
Motivation

- Sensors in nature: Eyes
- Wide Dynamic Range

Implementation

- True Logarithmic Amplifier
- Diode / BJT
- MOSFET in subthreshold region

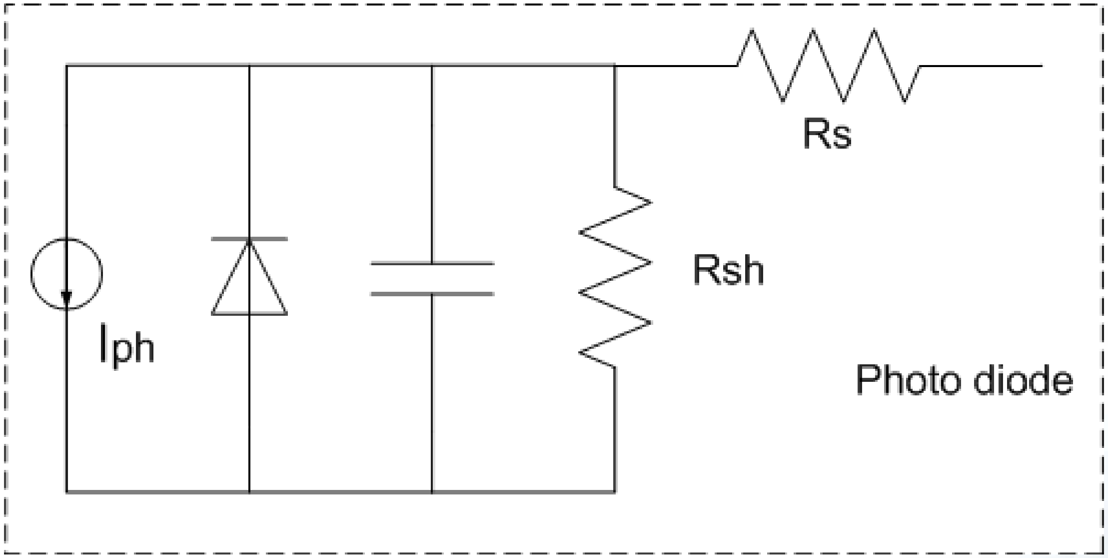
Entire System



- Figure 1. Block Diagram

Pixel & Log Amp

❖Equivalent Model of Photodiode



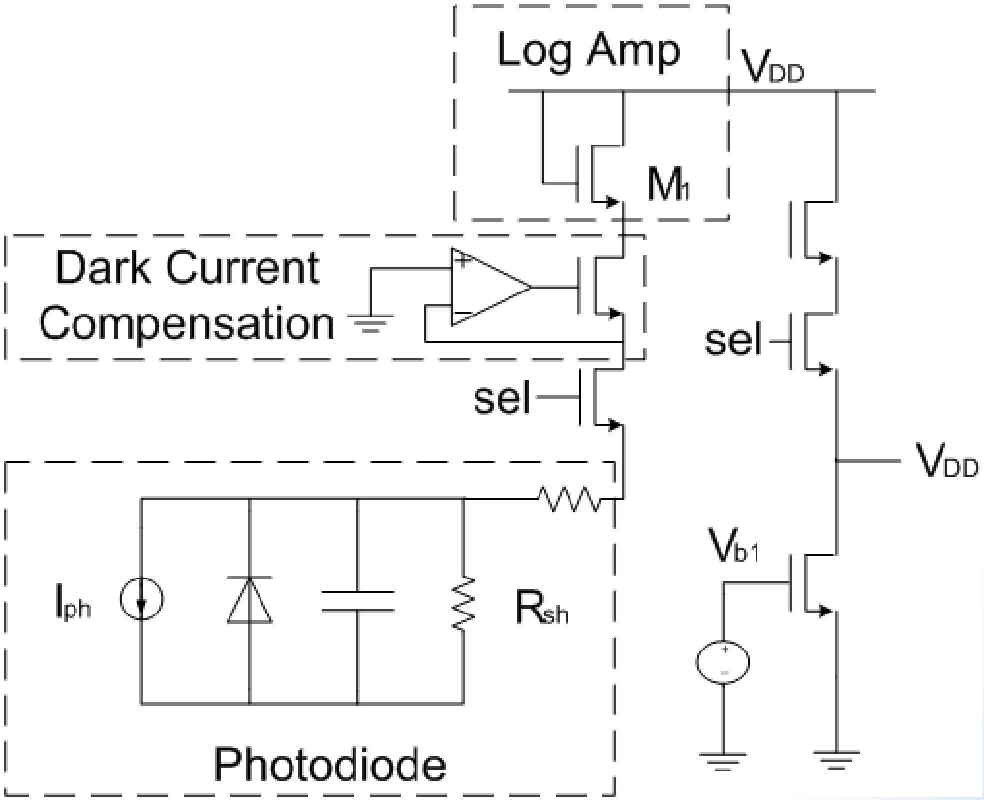
$$I_{ph} = q\lambda\eta P_0 A / hc$$

$$R_{sh} = \frac{R_0}{1+\delta(temp. + offest)}$$

- Figure 2. Equivalent Model of Photodiode

Pixel & Log Amp

❖ Dark Current Compensation



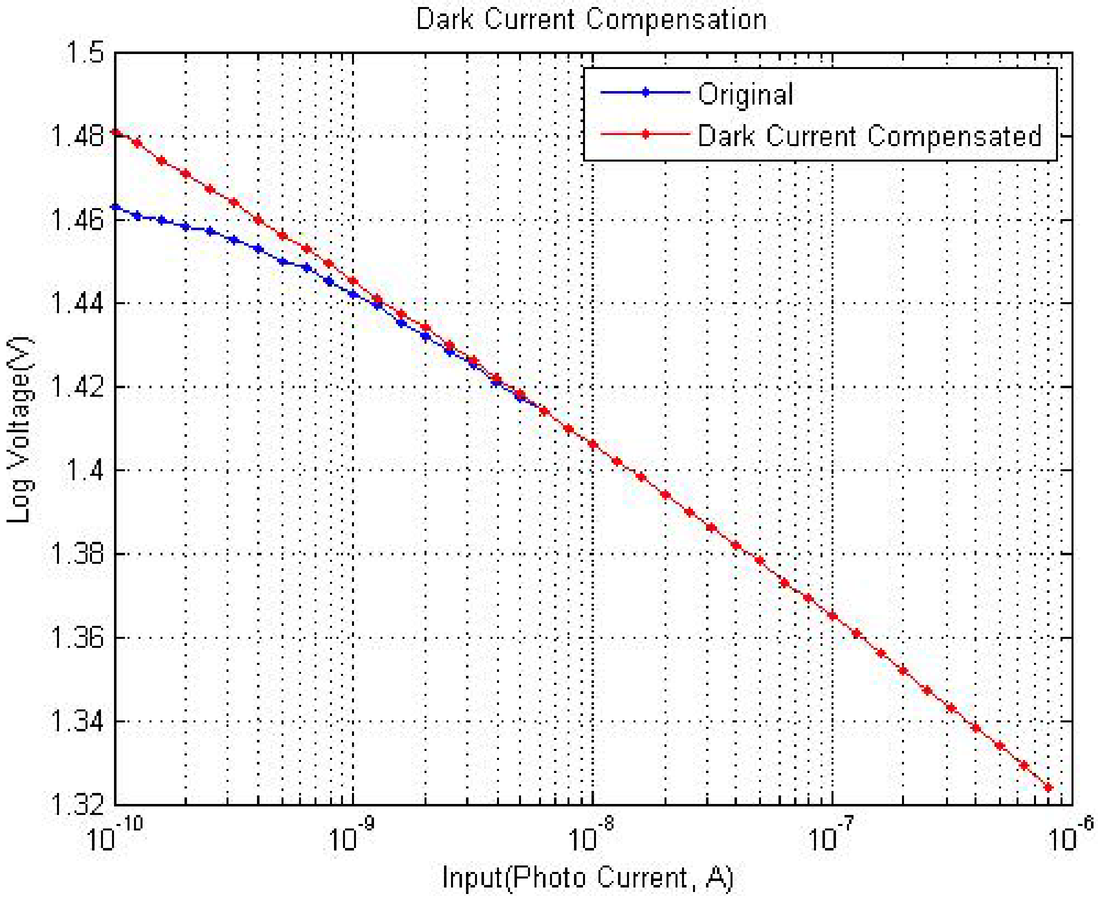
$$V_{gs} = V_T \ln[(I_{ph} + \Delta I_{ph}) / I_0]$$

$$\Delta \mathrm{I}_{\mathrm{ph}} \approx \frac{V_s - R_s \mathrm{I}_{\mathrm{ph}}}{R_{sh}} \approx \frac{V_s}{R_{sh}}$$

$$V_{bias} \rightarrow 0$$

- Figure 3. Schematic of Pixel

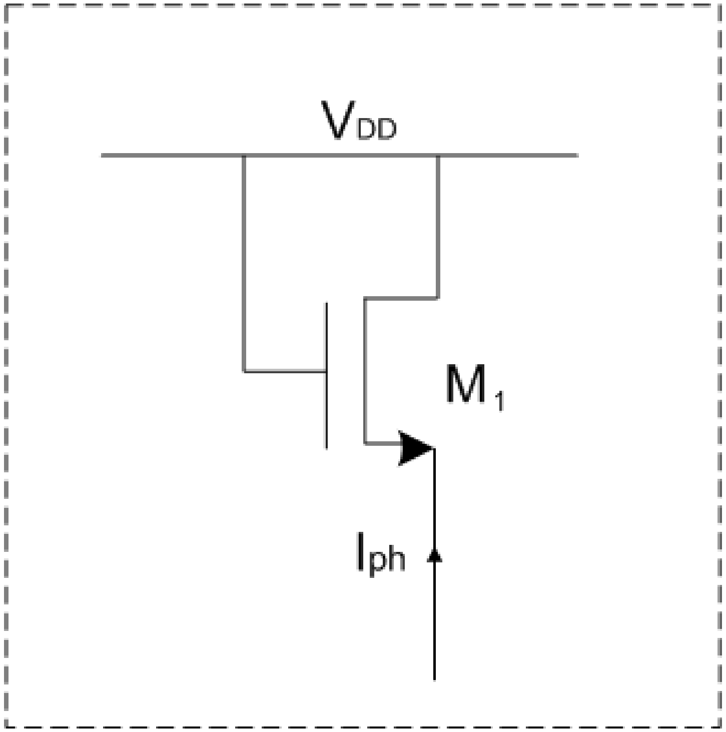
Pixel & Log Amp



- Figure 5. Effect of Dark Current Compensation

Pixel & Log Amp

❖Logarithmic Relation



Subthreshold Condition: $V_{gs} < V_{th}$

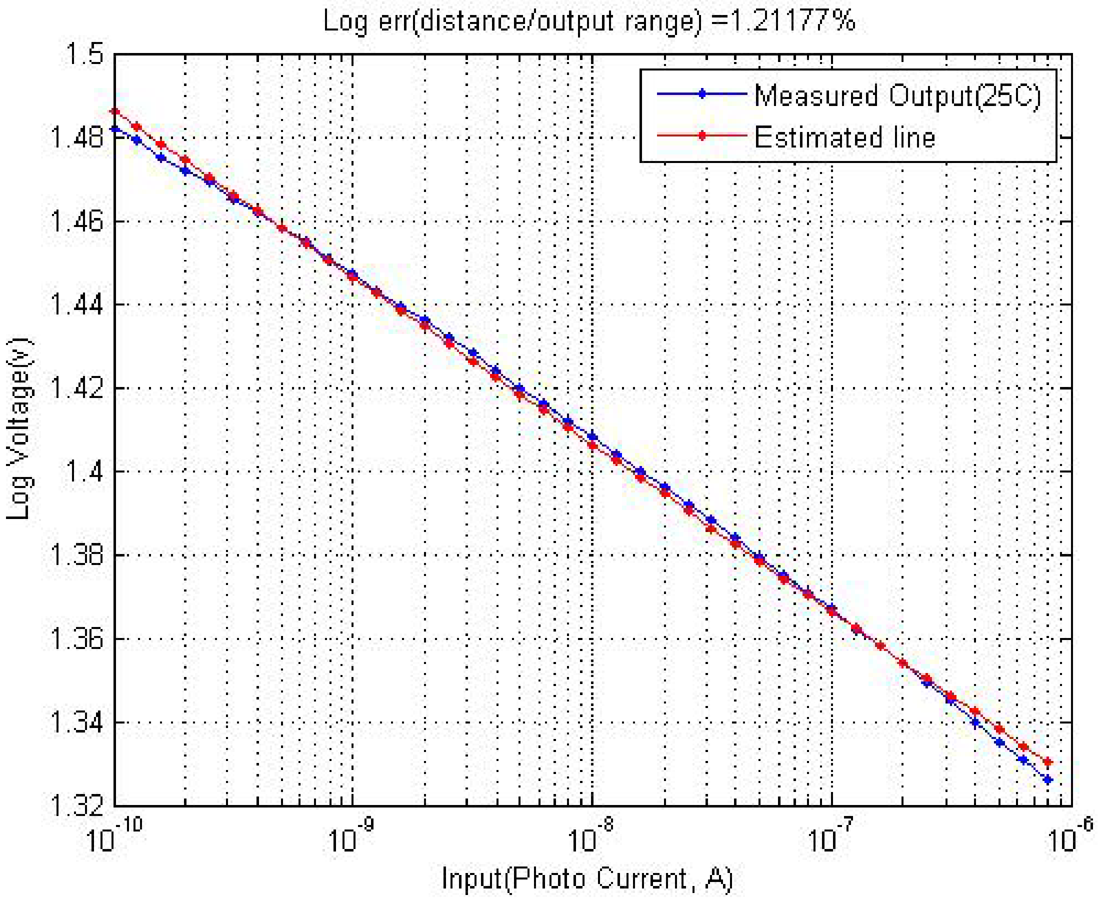
$I_{ph}: 100\,pA \sim 1\mu A$

$$V_{gs} = \zeta V_T \ln[I_{ph} / I_0]$$

$$I_0 \approx \frac{W}{L} qXD_n n_{po} \exp(\frac{-V_{th}}{\zeta V_t})\,(1+\frac{V_{ds}}{V_A})$$

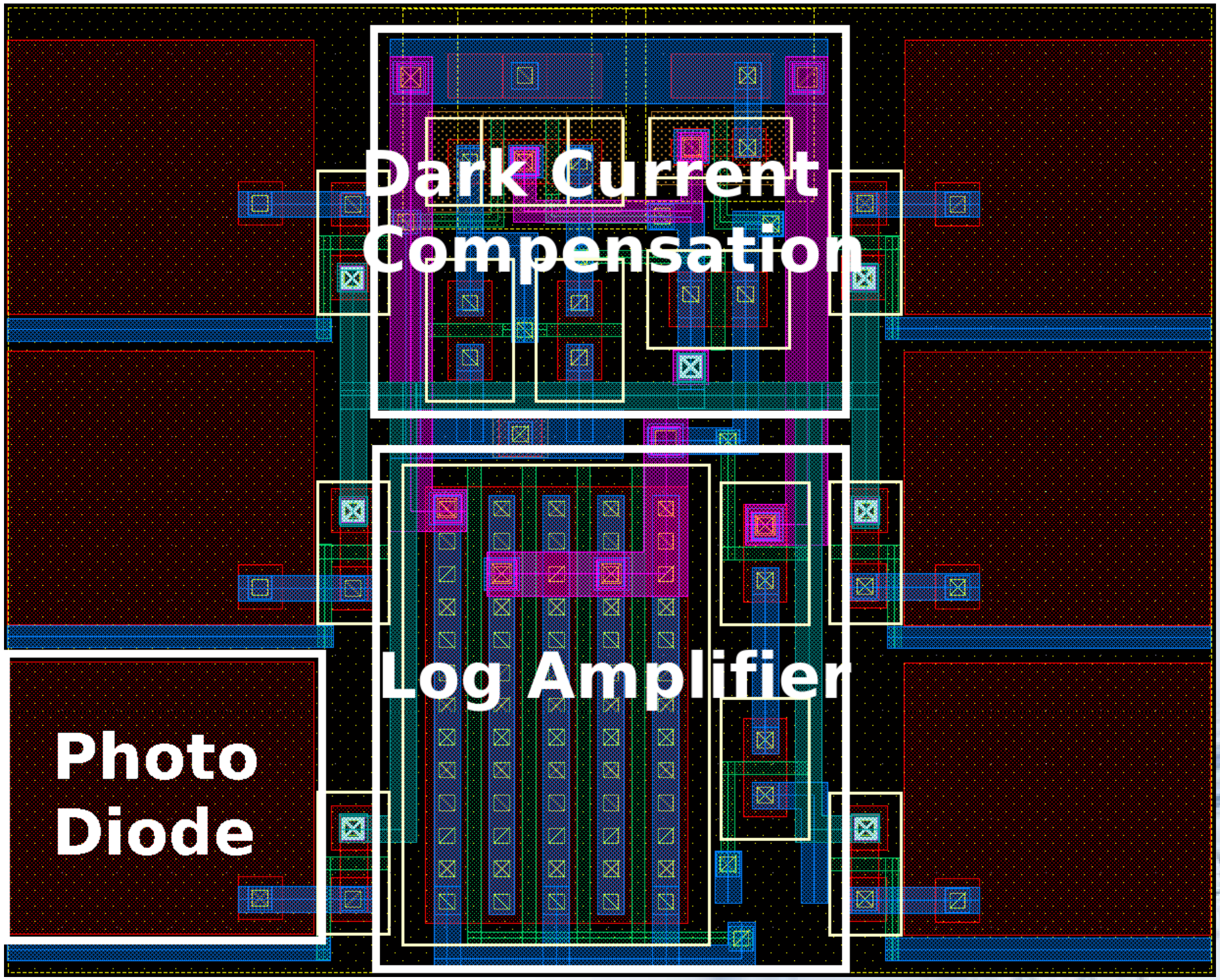
- Figure 3. NMOS in subthreshold region

Pixel & Log Amp



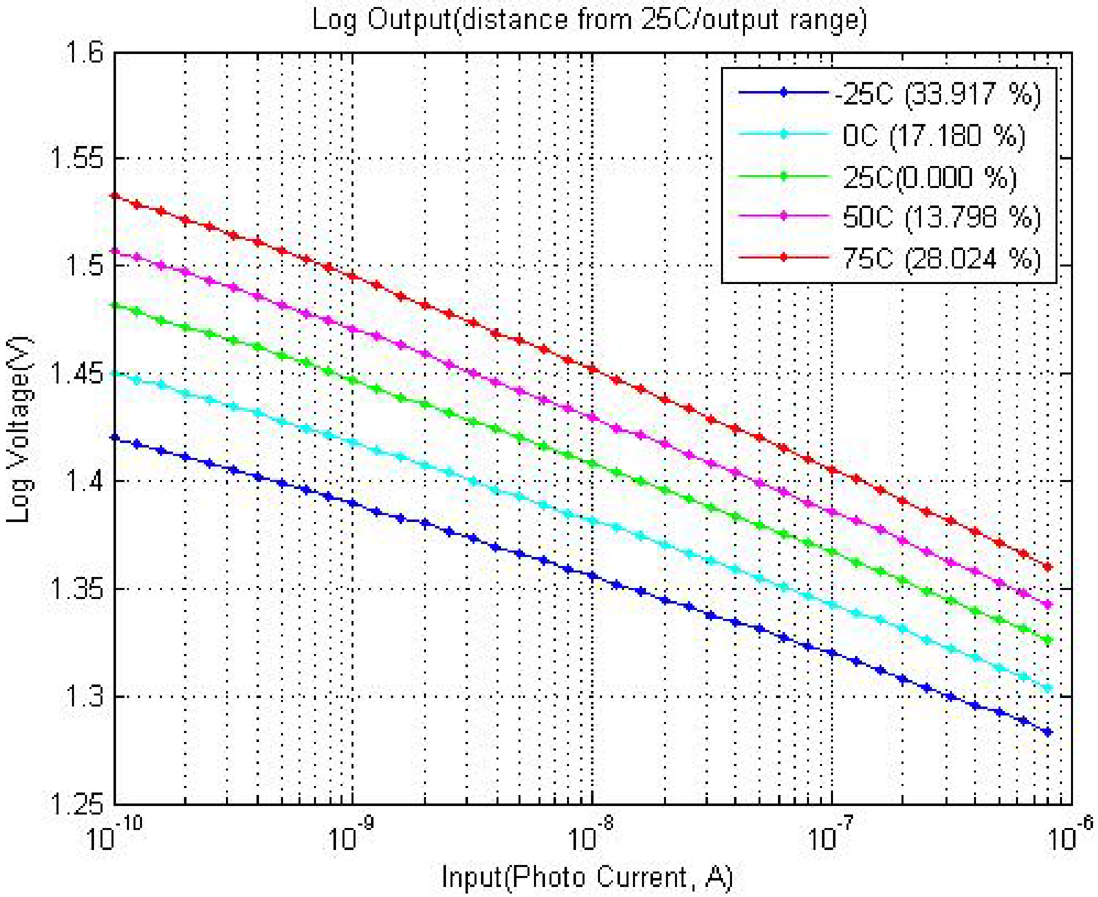
- Figure 6. Comparison with Ideal Logarithmic Response

Pixel & Log Amp



- Figure 4. Layout of Pixels and Log Amp (Six Imaginary photodiodes)

Pixel & Log Amp



- Figure 7. Temperature Dependence of Output Response

Ideal Reference

❖ Necessity of Ideal reference

- Temperature variation
  - Temperature Coefficient
- Process variation
  - Mobility, junction depth, etc
- Supply variation

Ideal Reference

❖ Bandgap voltage reference

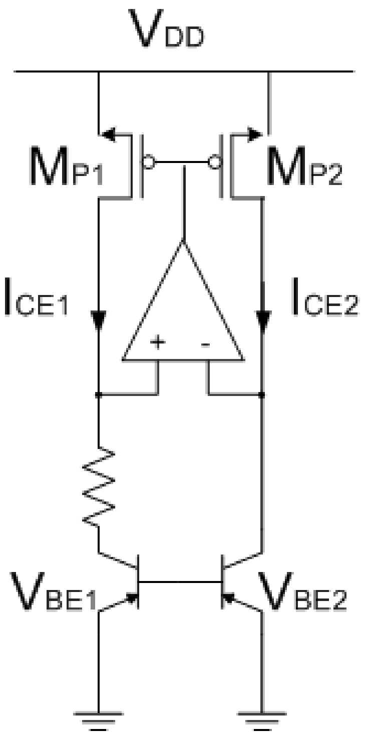
- To generate current reference, use Bandgap reference voltage
- Use bipolar transistor
  - Well defined quantities for temperature
  - Exponential V-I relation

$$I_{CE} = I_S\left(e^{V_{BE}/V_T} - 1\right)$$

$$V_{BE} = V_T \ln\left(\frac{I_{CE}}{I_S}\right) + 1$$

Ideal Reference

❖ Implementation of Bandgap voltage



$$V_{BE1} = V_T \ln\left({}^{I_{CE1}}\!/_{I_S}\right) + 1$$

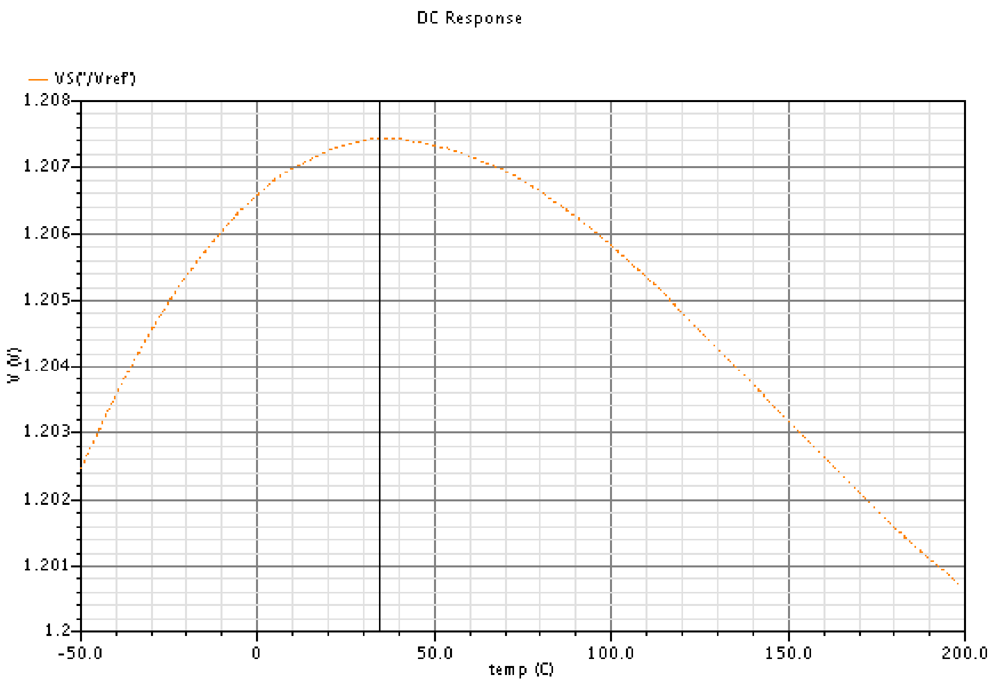
$$V_{BE2} = V_T \ln\left({}^{I_{CE2}}\!/_{I_S}\right) + 1$$

$$V_{BE2} = V_{BE1} + V_T \ln {}^{I_{CE1}}\!/_{I_{CE2}}$$

$$\frac{\partial V_{BE2}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} + \frac{k}{q}\ln n$$

Ideal Reference

❖Simulation result of Bandgap voltage



- A finite Curvature
- Shift zero TC by R, n value

Implementation of Current

❖ How to convert to current reference

- V-I conversion
  - Need to use Resistor
- Switched-capacitor Resistor
  - Need Clock signal

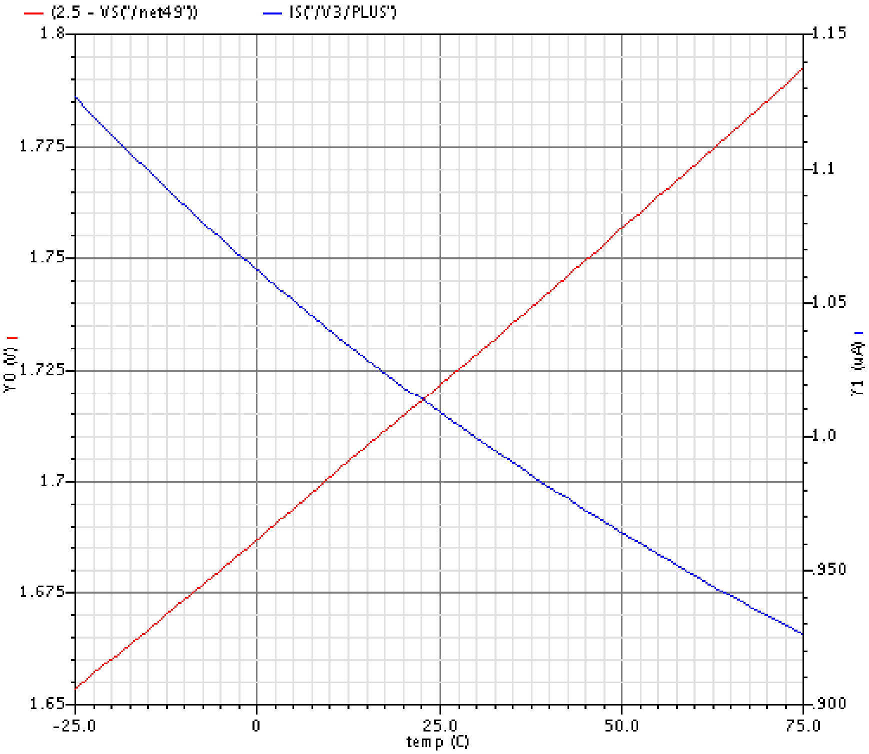
Implementation of Current

❖ How to convert to current reference

- Use the negative TC of PMOS
- Shift zero TC of bandgap voltage

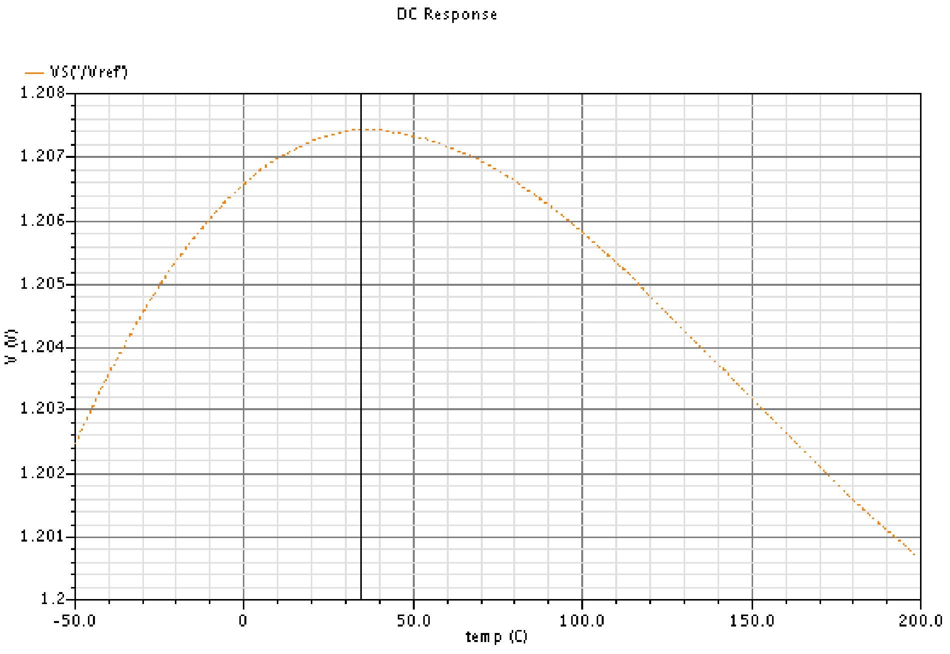
$$\frac{\partial I_{DS}}{\partial T} = \frac{1}{2}\frac{\partial \mu_P}{\partial T} C_{OX}\frac{W}{L}V_{od}{}^2 + \mu_P C_{OX}\frac{W}{L}V_{od}\frac{\partial V_{od}}{\partial T}$$

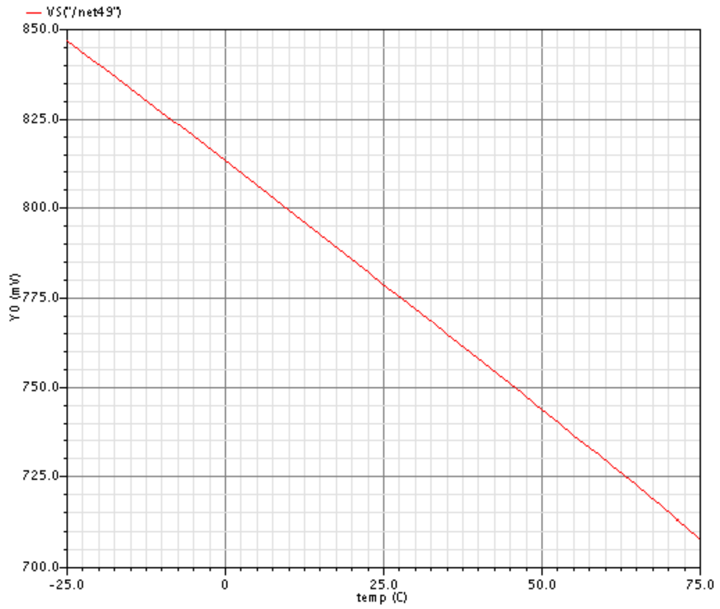
$$V_{od} = V_{DD} - V_{REF} + V_{TP}$$



Implementation of Current

❖ How to convert to current reference

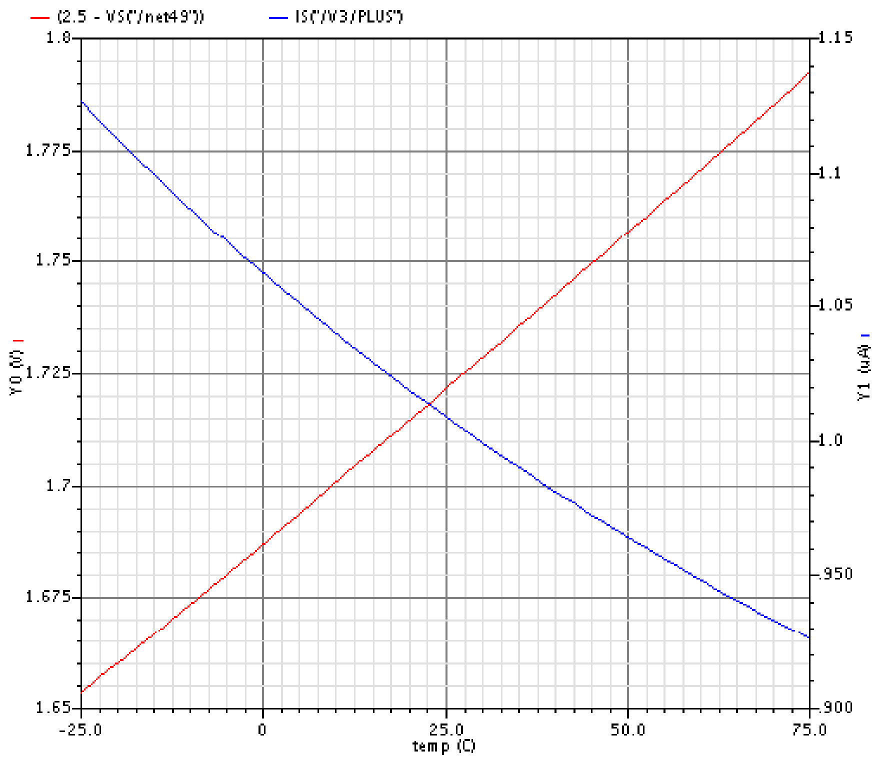


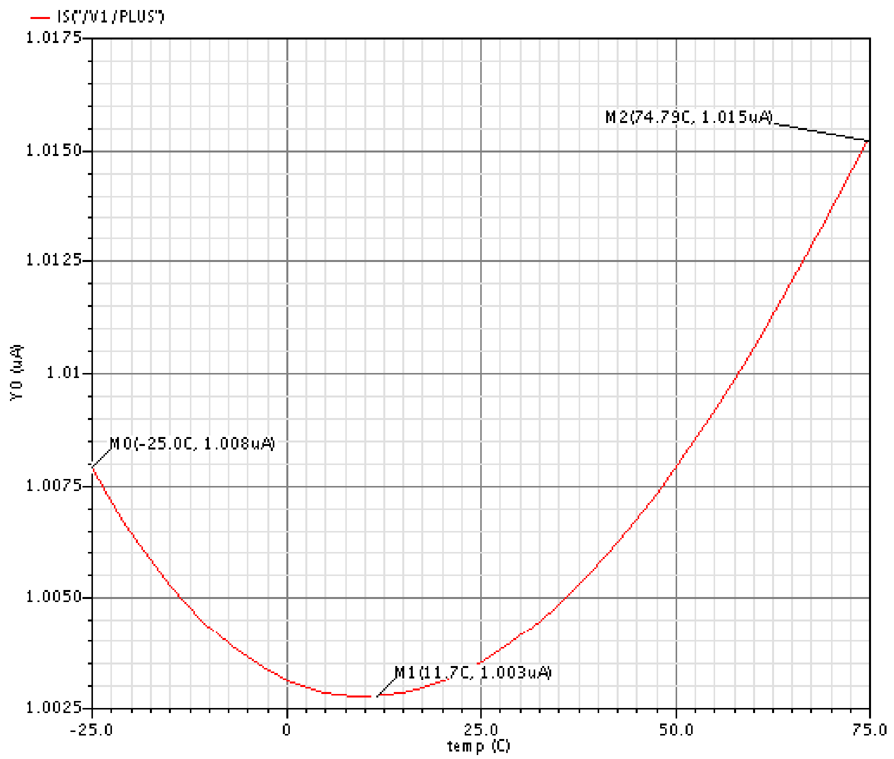


- Shifted Bandgap

Implementation of Current

❖Simulation result

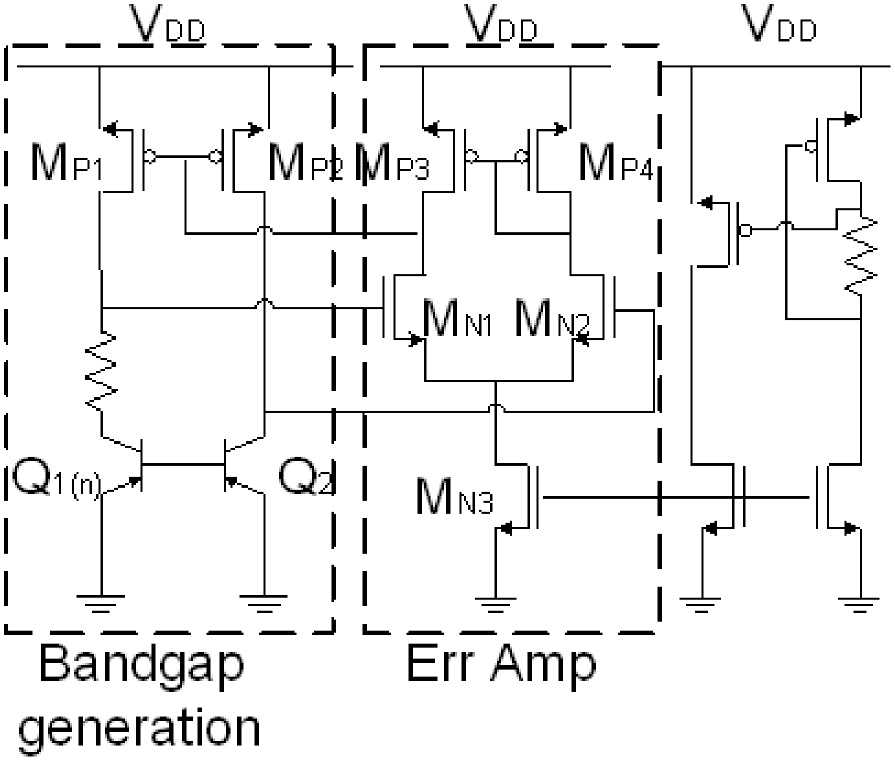


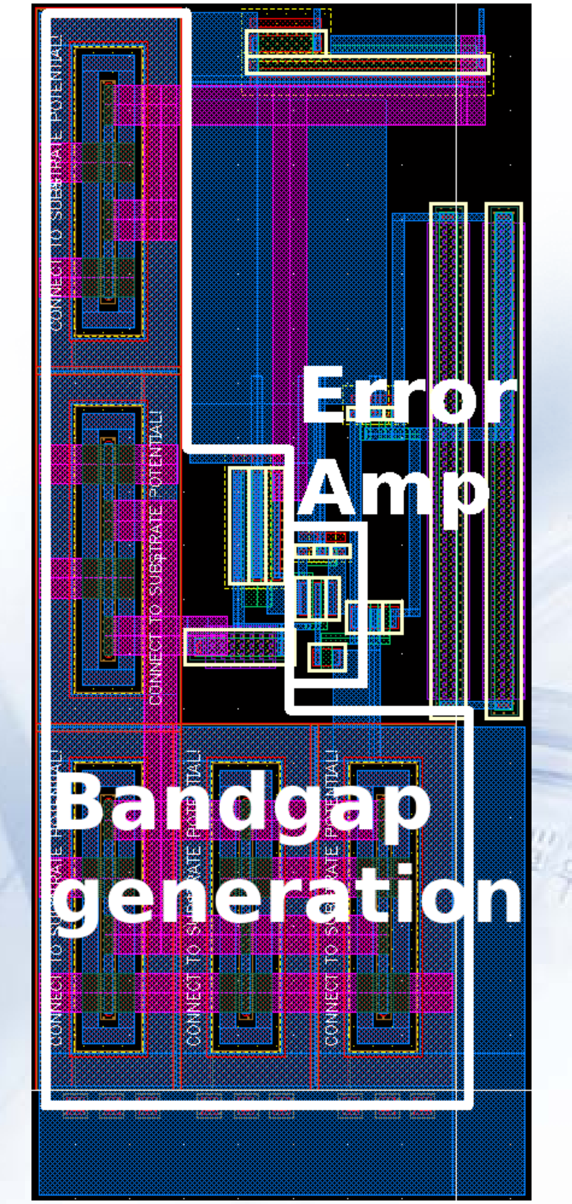


- Vod and negative TC
- Compensated current

Implementation of Current

- Schematic and Layout





Temperature Compensation

❖ How to compensate temperature?

$$V_{in} = \zeta V_T \ \ln\left(I_{in} / I_0 \right)$$

- Temperature dependent term: V_T , I_0
- $V_T \propto T$, $I_0 \propto T^3$
- Using reference current(I_{ref}), eliminate I_0
- Using bias current(I_{ss}), eliminate V_T

Temperature Compensation

❖ Elimination I_0

$$V_{in} = \zeta V_T \ \ln\left({}^{I_{in}}\!/_{I_0} \right) \qquad V_{ref} = \zeta V_T \ \ln\left({}^{I_{ref}}\!/_{I_0} \right)$$

- We can get V_{ref} from I_{ref} and subthreshold transistor.
- By subtraction, we can remove I_0.

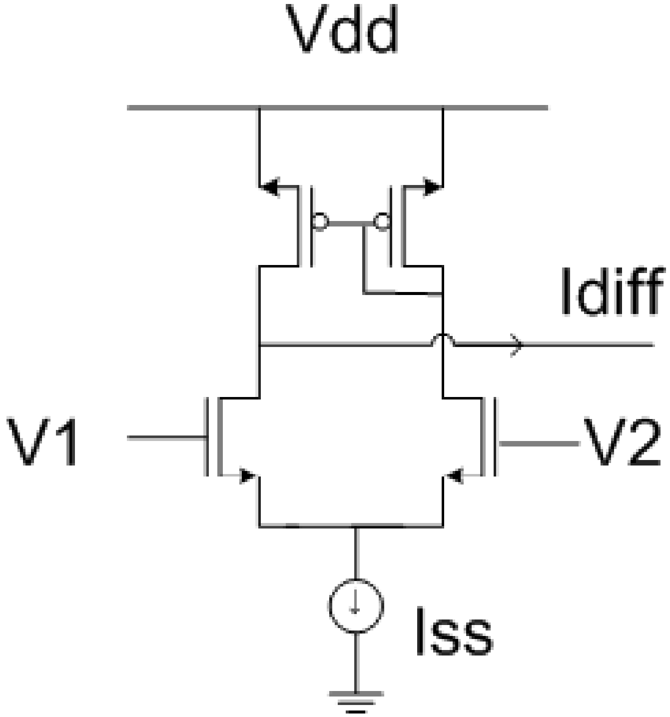
$$V_{in} - V_{ref} = \zeta V_T \ \ln\left({}^{I_{in}}\!/_{I_{ref}} \right)$$

- To do subtraction, we use differential amp.

Temperature Compensation

❖ Differential Amplifier(DC operation)

$$I_{diff} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1\text{-}V_2)\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - (V_1\text{-}V_2)^2}$$



- If $\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} \gg (V_1\text{-}V_2)^2$,

then,

$$I_{diff} \approx \sqrt{\mu_n C_{ox}\frac{W}{L}I_{ss}}\,(V_1\text{-}V_2)$$

$$I_{diff} \propto (V_1\text{-}V_2)$$

Temperature Compensation

❖ Elimination V_T

$$I_{\mathrm{diff}} \approx \sqrt{\mu_n C_{\mathrm{ox}} \frac{W}{L} I_{ss}}\,(V_1 - V_2) \propto \sqrt{\mu_n I_{ss}}\, V_T$$

- If we can make $I_{\mathrm{ss}} \propto \mu_n T$, $I_{\mathrm{diff}} \propto \mu_n T^{\frac{3}{2}}$
- In general, $\mu_n \propto T^{-\frac{3}{2}}$

$$\therefore I_{\mathrm{diff}} \propto T^0$$

Temperature Compensation

❖ I_{ss} Generation

- Object: $\mathrm{I_{ss}} \propto \mu_n \mathrm{T}$
- Use differential amplifier again.

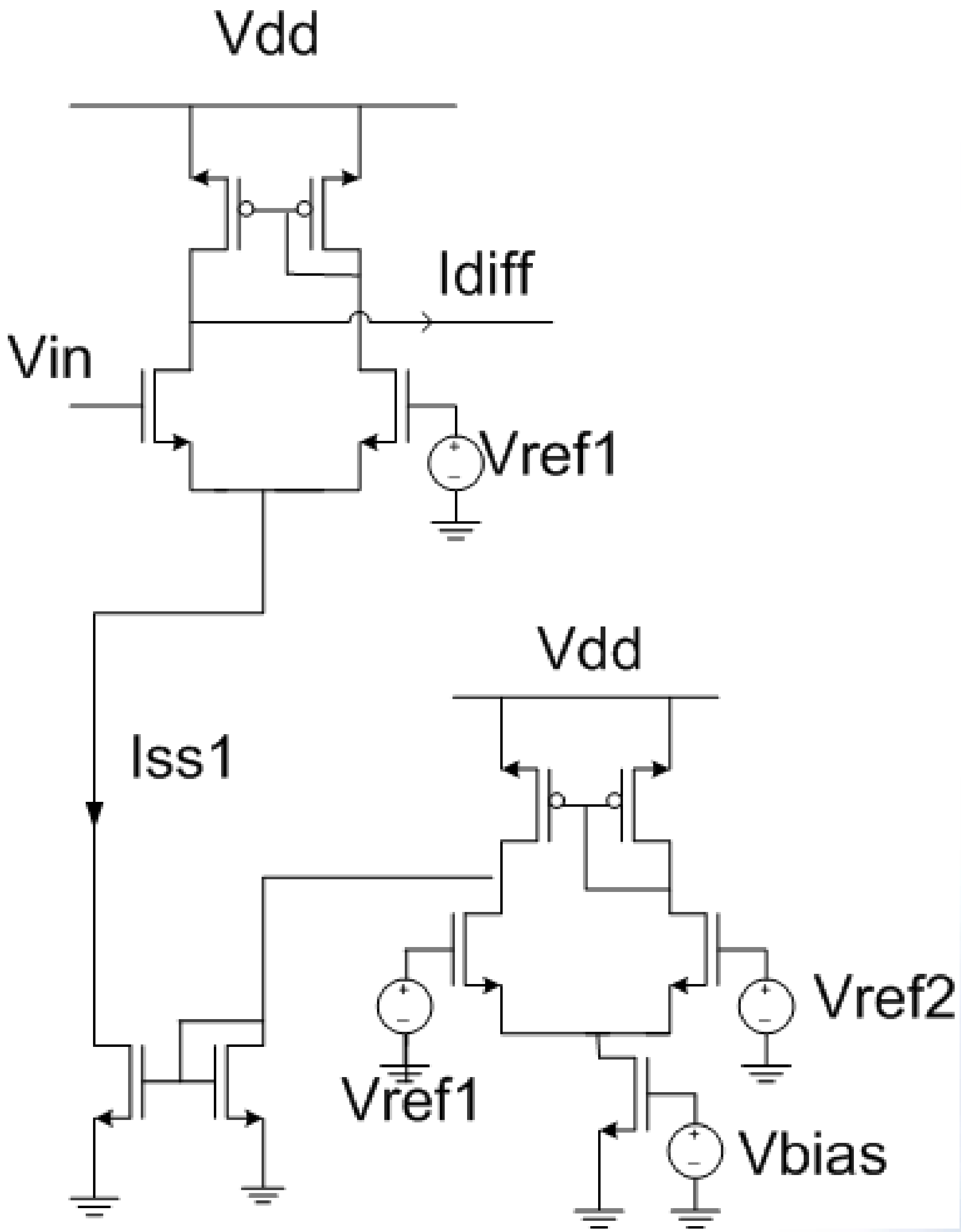
$$\mathrm{I_{ss}} \approx \sqrt{\mu_n \mathrm{C_{ox}} \frac{\mathrm{W}}{\mathrm{L}} I_{ss2} (\mathrm{V_3}\text{-}\mathrm{V_4})}$$

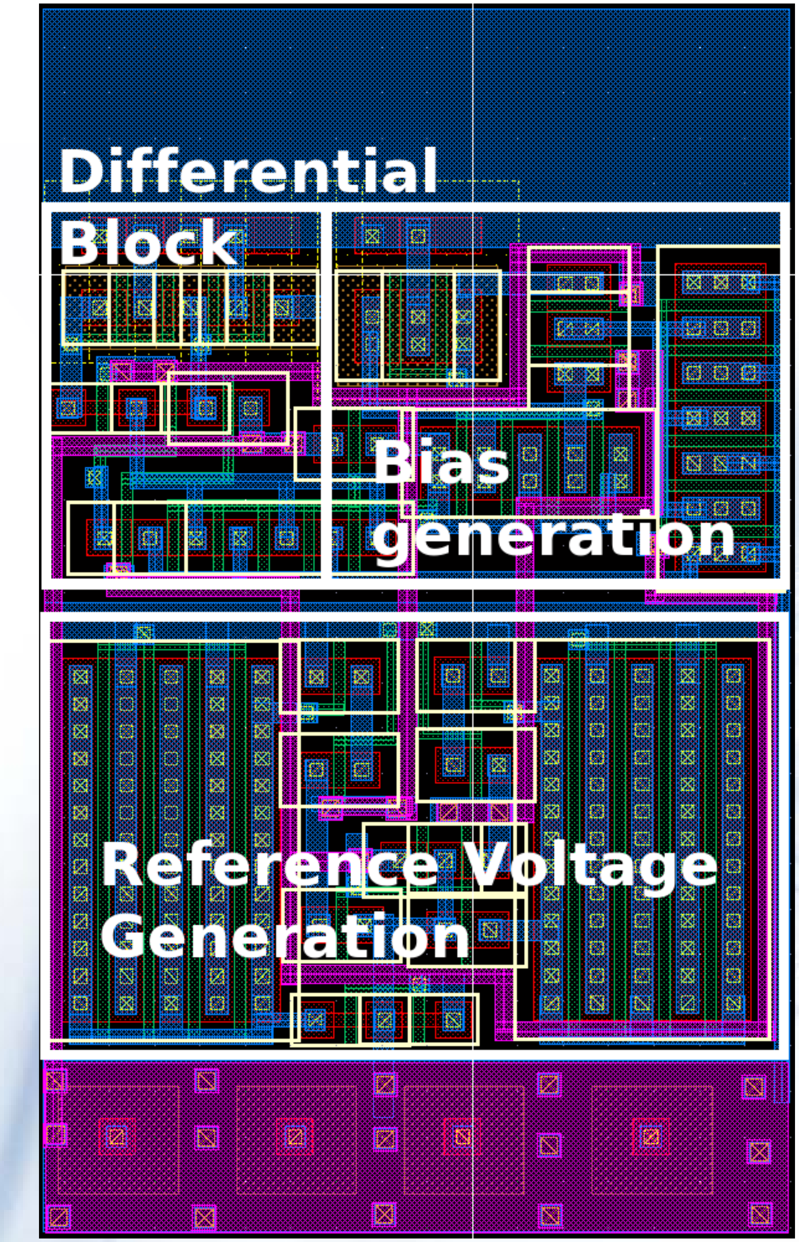
- Need to meet

$$\mathrm{I_{ss2}} \propto \mu_n,\ \mathrm{V_3}\text{-}\mathrm{V_4} \propto \mathrm{T}$$

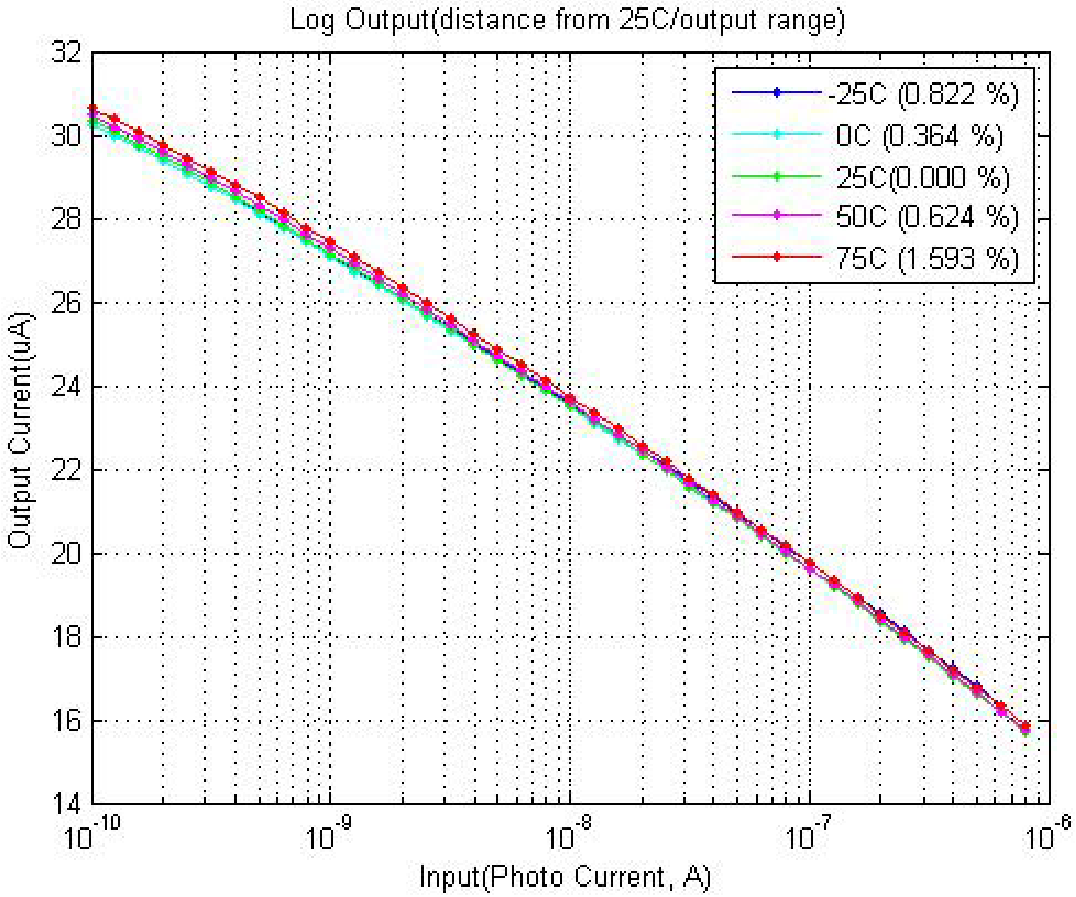
- Set $\mathrm{I_{ss2}} = \frac{1}{2}\mu_n \mathrm{C_{ox}} \frac{W}{L} (\mathrm{V_{gs}}\text{-}\mathrm{V_{th}})^2$ using NMOS.
- Set $\mathrm{V_3}\text{-}\mathrm{V_4} = \zeta V_T \ \ln(\mathrm{I_{ref}} / \mathrm{I_{ref2}})$ same as V_{in} -V_{ref}

Temperature Compensation

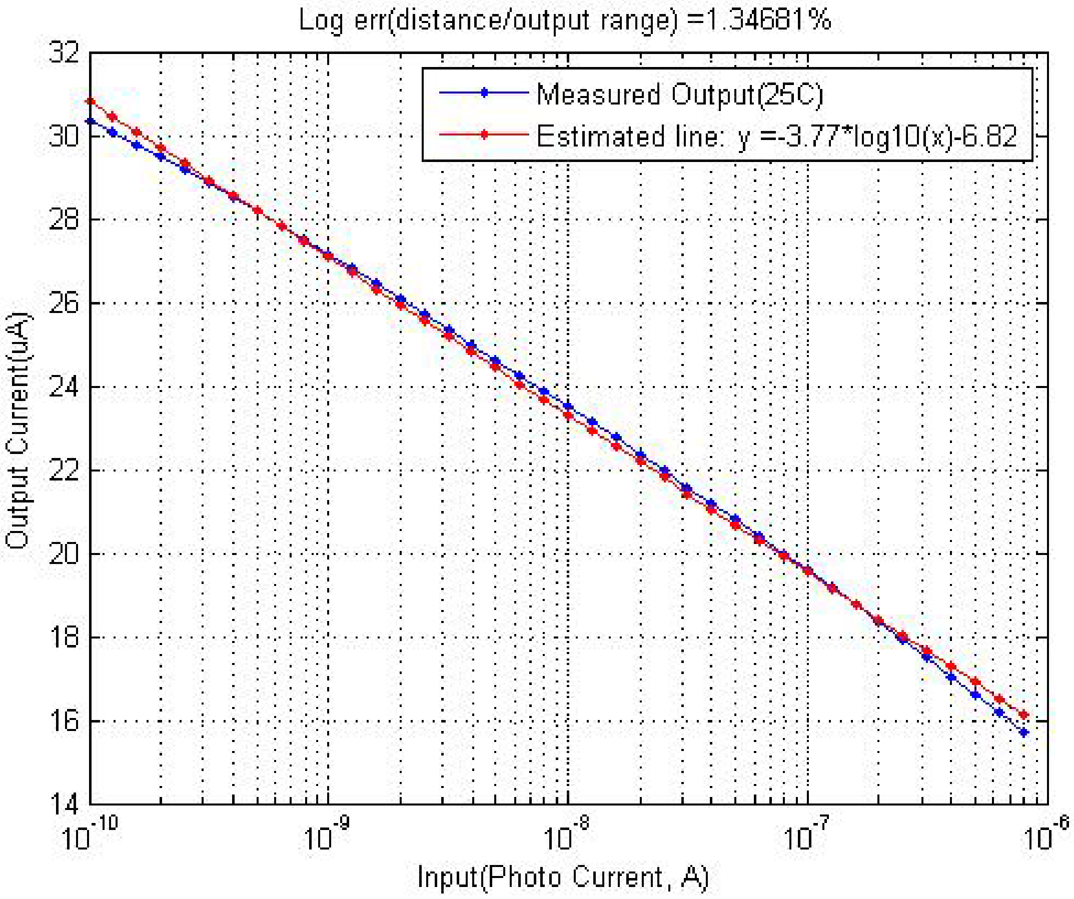




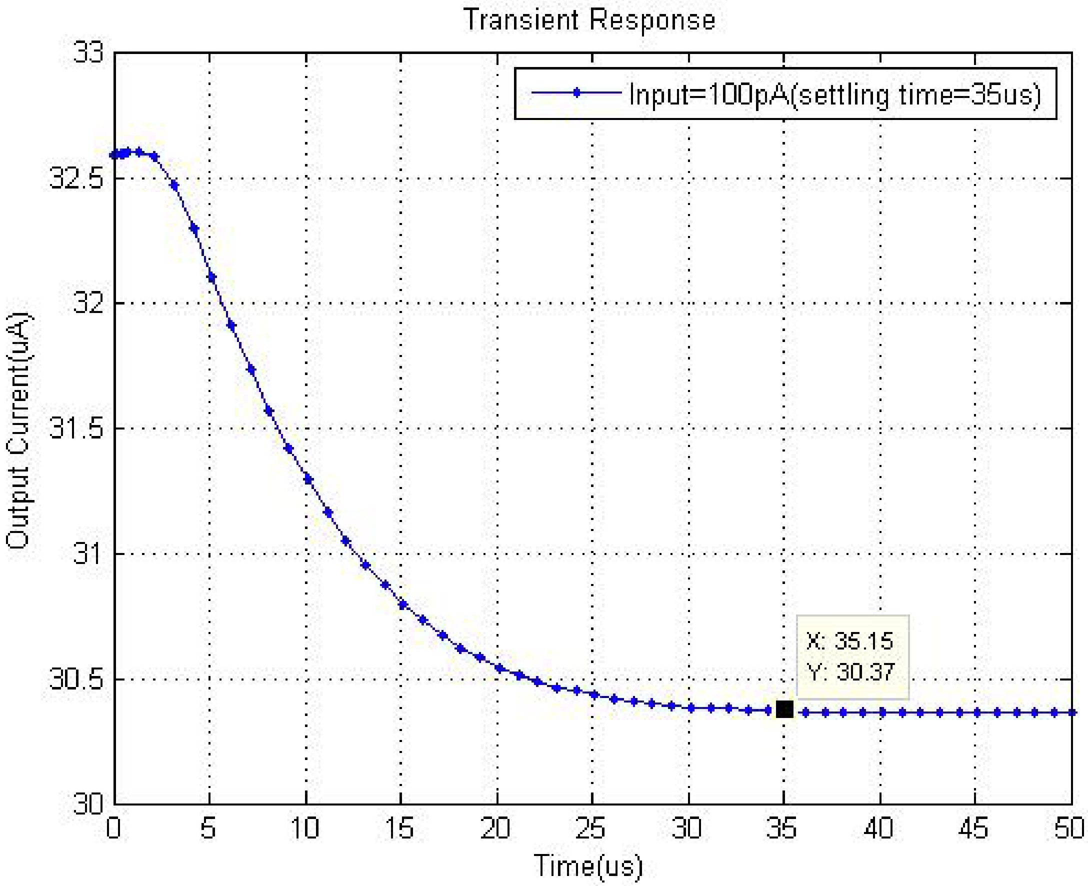
Temperature Compensation



Temperature Compensation



Transient Response



Result Table

	This work	Infineon Tec.	Koli et al.
Year	2007	2005	1997
Technology	0.240um CMOS	0.5um BiCMOS	1.2um CMOS
Dynamic Range	80 dB	68 dB	42 dB
Log Error	1.35%	3%	2 dB
Temperature Err	1.59%	1.2%	2 dB
Power Consumption	0.906 mW	1.675 mW	3 mW
Input Range	100pA ~ 1uA	2nA ~ 5uA	-50dBm~-10dBm
Output Range	15uA ~ 31uA	50uA ~ 400 uA	-0.25V ~0.01V
Pixel Size	8.5 um X 6um		
Chip Size		1.46 mm^2	3.2 mm^2

Thank You !