EECS413 Final Project

Group 7

A CMOS LNA and Mixer for FM Receivers

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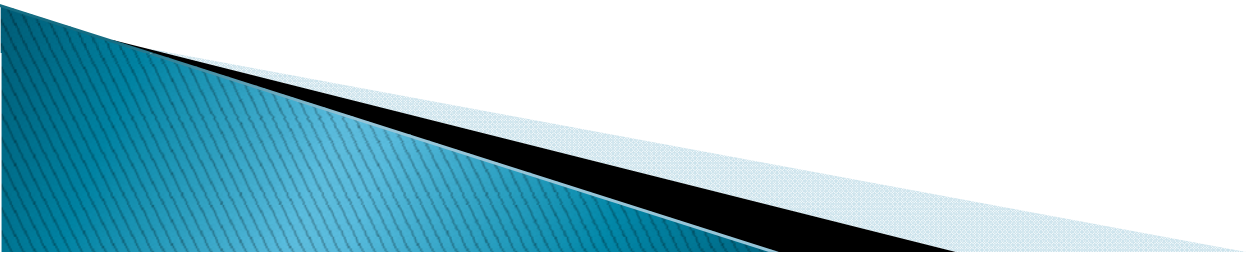
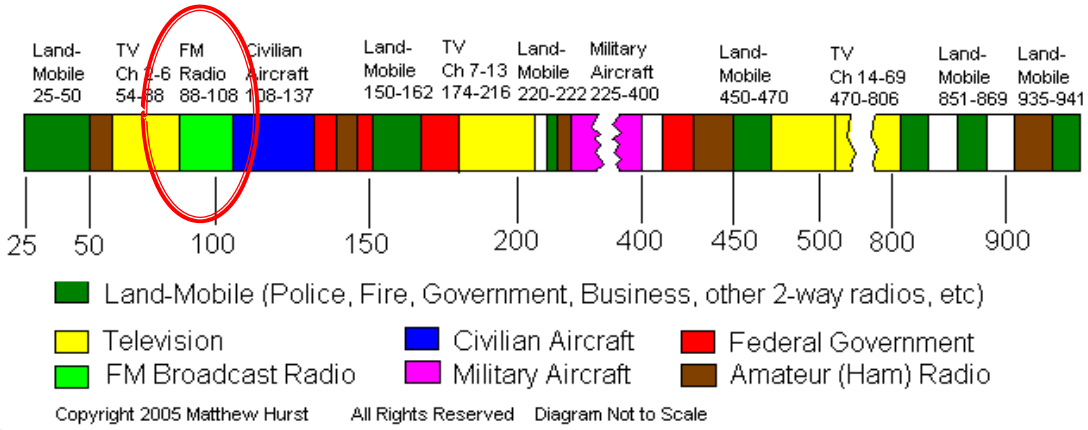


Introduction

- Continuous demand for high performance, low power RF circuits
- CMOS provides a favorable environment to integrate analog and digital on a single chip
- FM Band (88 – 108MHz)



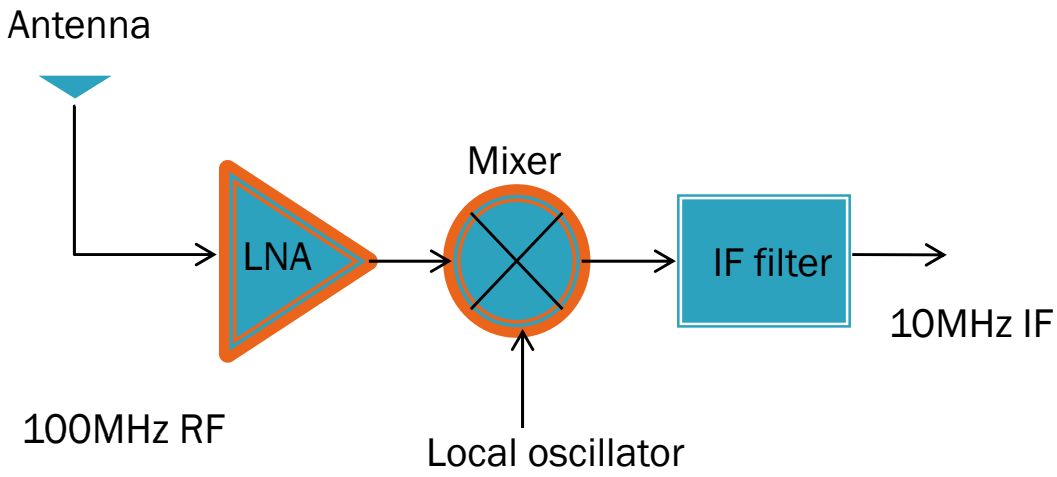
Design goals

LNA:

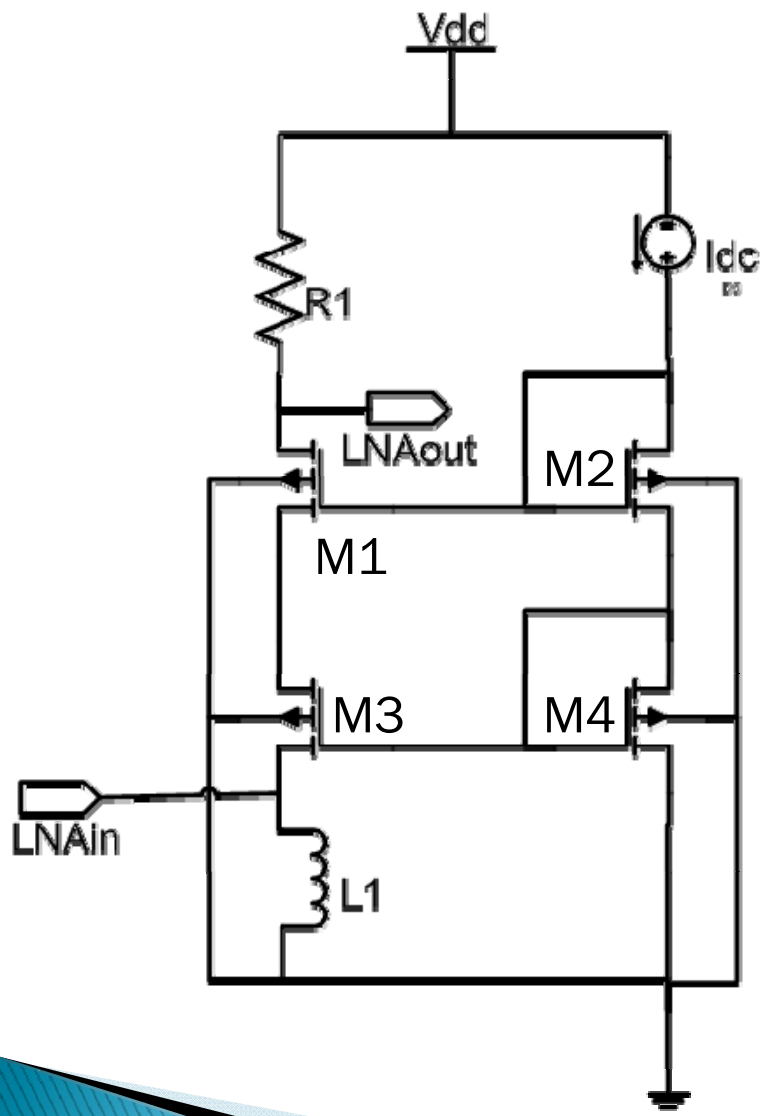
- Input matching network (50Ω)
- Enough gain to overcome noise in later stages
- Low Power
- Linearity

MIXER:

- Translate the RF signals with minimal distortion
- High gain, low power consumption

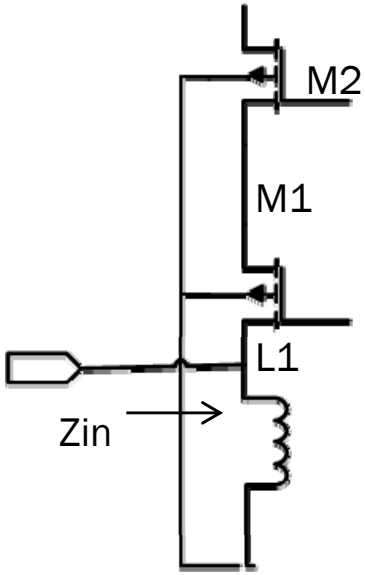


LNA– Choosing Topology



- Why 2 stage cascode common gate?
- Isolation from output to input and better power supply noise rejection
- Increase output impedance

LNA-Input impedance



- In RF applications, impedance is usually 50 Ω (matched to antenna)

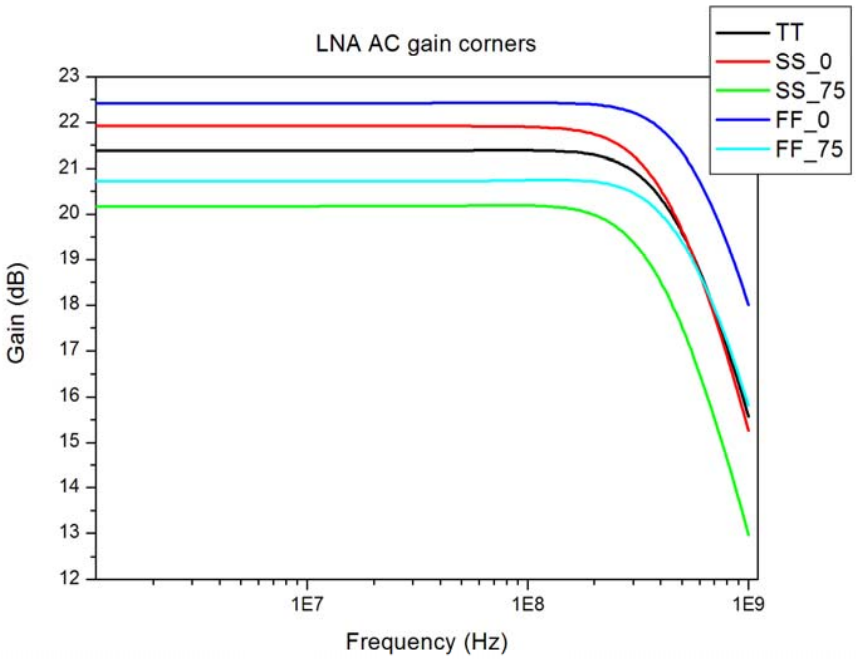
$$Z_{in} = \frac{sL}{sL(g_m + sC_{gs1}) + 1} = 50$$

- Assume Cgs equals to 10pF,

$$\omega_0^2 = \frac{1}{L_2 C_{gs}} = \frac{1}{10^{-11} \times L_2} = (2\pi \times 100 \times 10^6)^2$$

$$\Rightarrow L_2 = 253.3nH \rightarrow off - chip$$

LNA - Gain



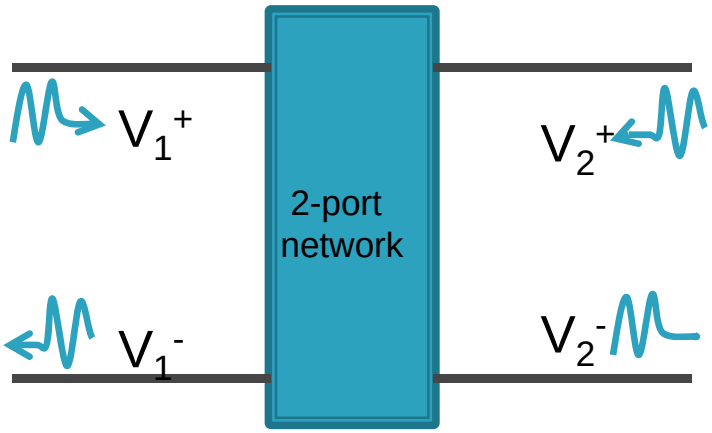
- Gain $A_v = \frac{g_{m3} g_{m1} R_1}{g_{m1} + sC_{gs1}} \approx g_{m3} R_1$

Too high: early mixer saturation and bad linearity

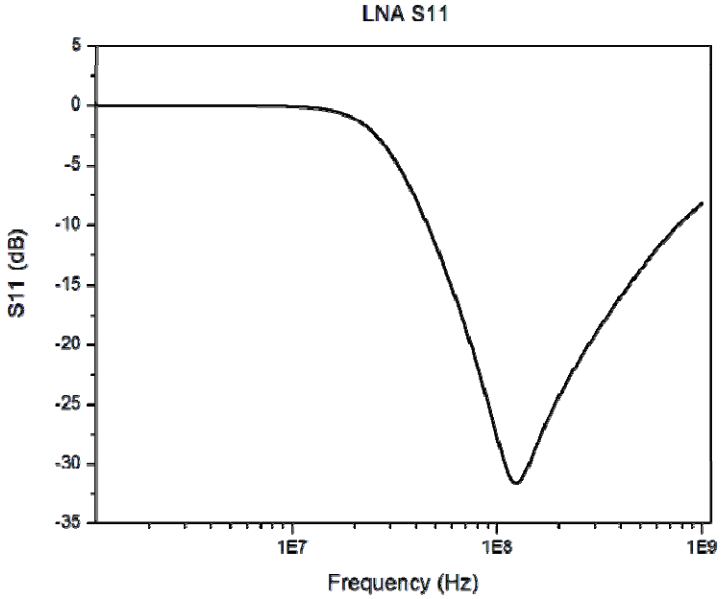
Too small: NF of whole system increase

- Ideally, $A_v = 15 \sim 20dB$
- Our design: $A_v = g_m R_l = 20\log(0.022 \times 600) = 22dB$

S-Parameter and stability



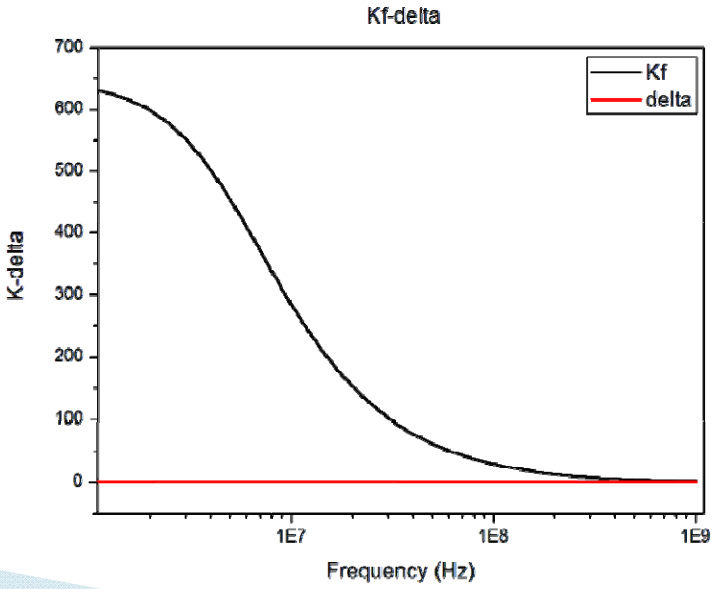
$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+ = 0 \; for \; k \neq j}$$



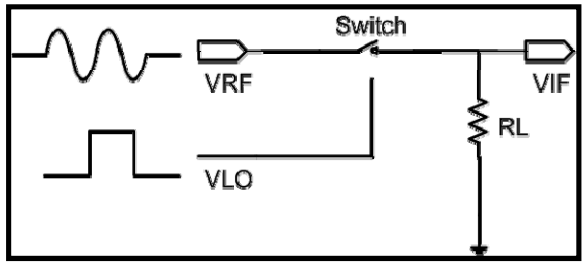
- **For unconditional stability,**

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

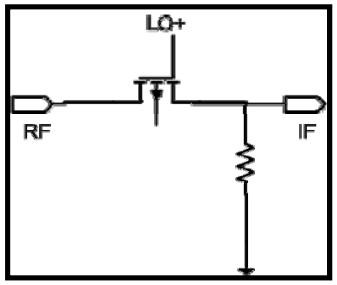
$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$



Mixer—down conversion



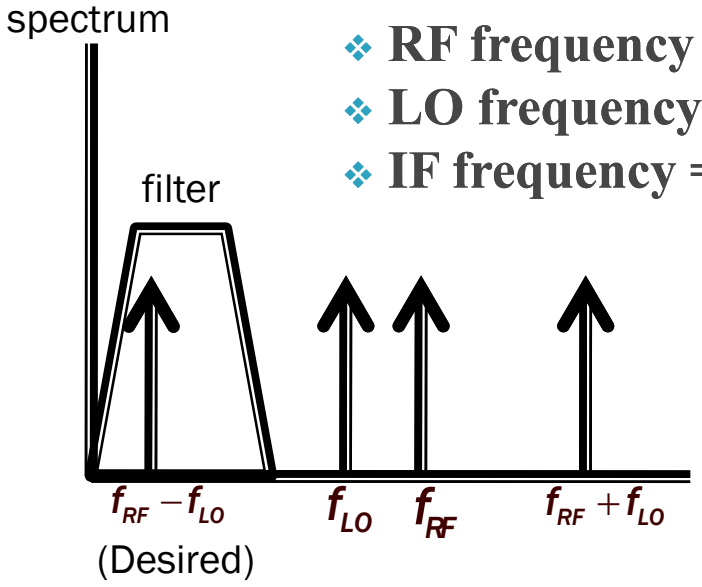
- Simple switch as a mixer



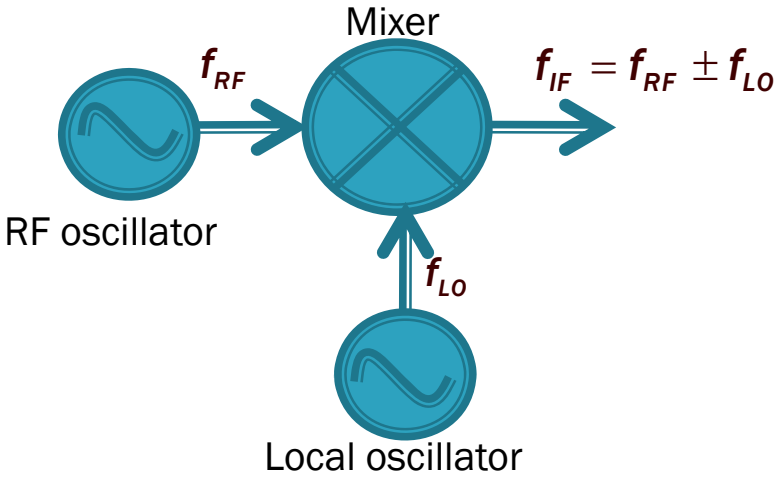
- Implementation with NMOS

$$V_{IF}(t) = KV_{RF}(t)V_{LO}(t) = K\cos 2\pi f_{RF}t \cos 2\pi f_{LO}t$$

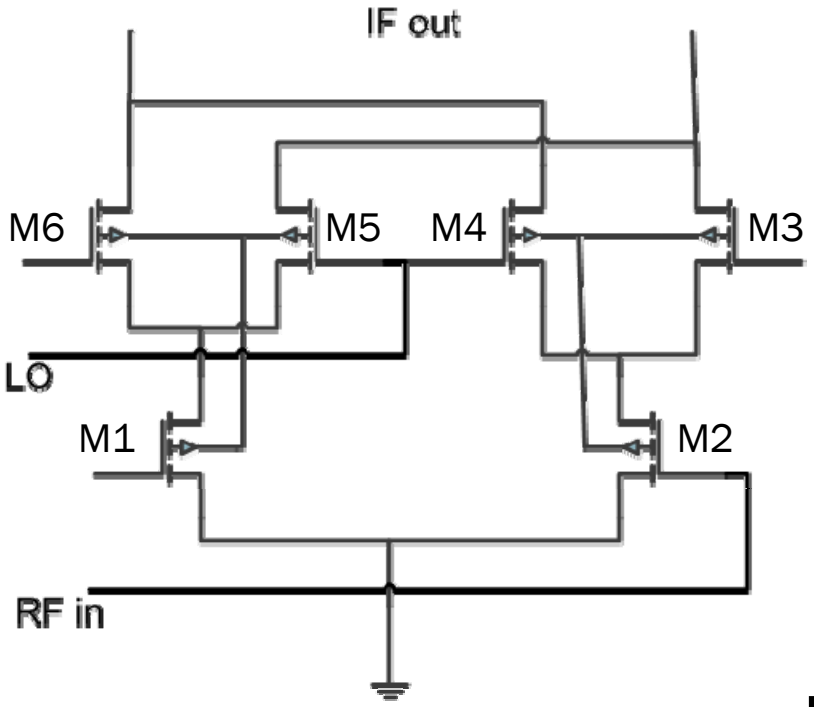
$$= \frac{K}{2}[\cos 2\pi(f_{RF} - f_{LO})t + \cos 2\pi(f_{RF} + f_{LO})t]$$



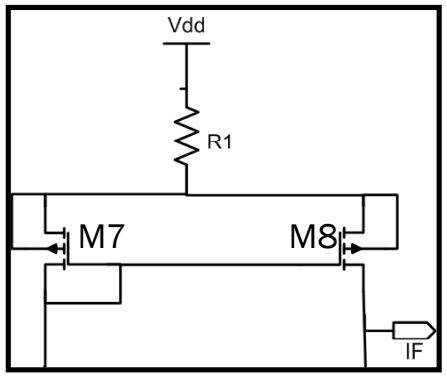
- RF frequency = 100MHz
- LO frequency = 90MHz
- IF frequency = 10MHz

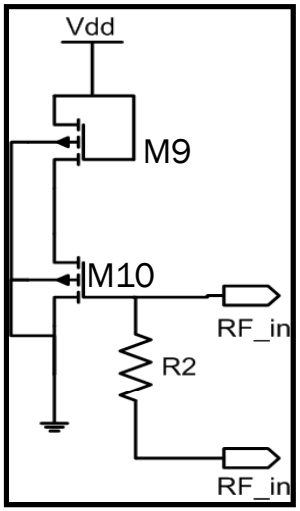


Mixer Topology



- Active double balanced mixer Gilbert Cell
- Rejection of LO coupling
- Single-ended I/O port

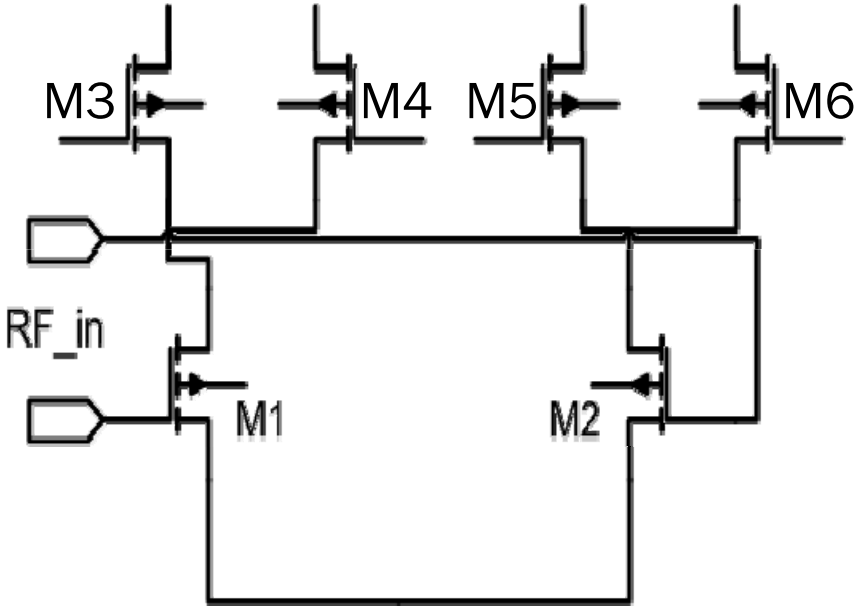




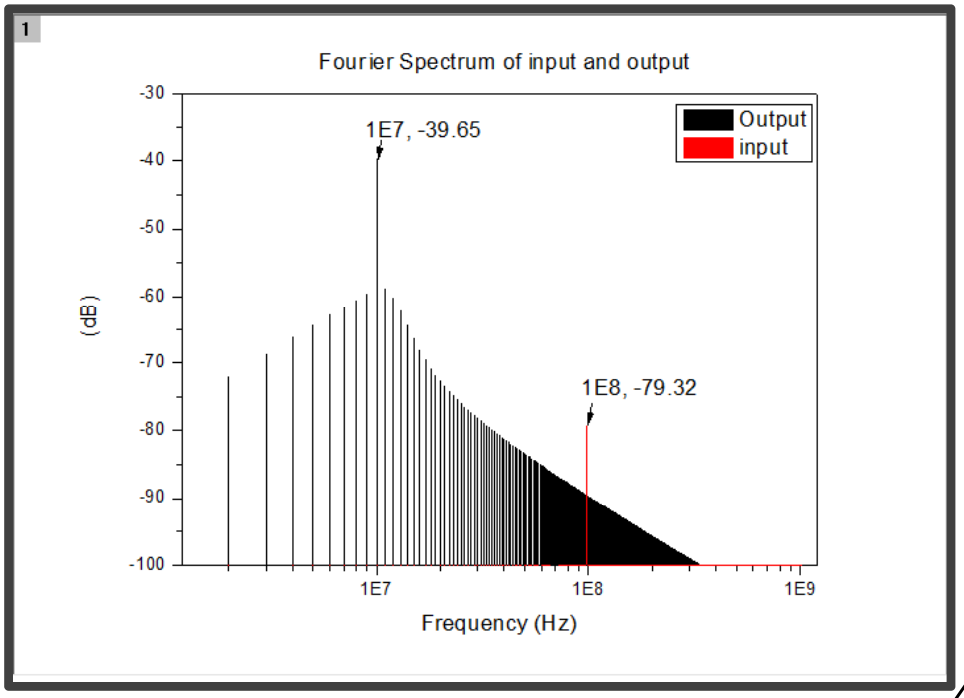
- DC bias circuit
- Current mirror
- R1 for output voltage level

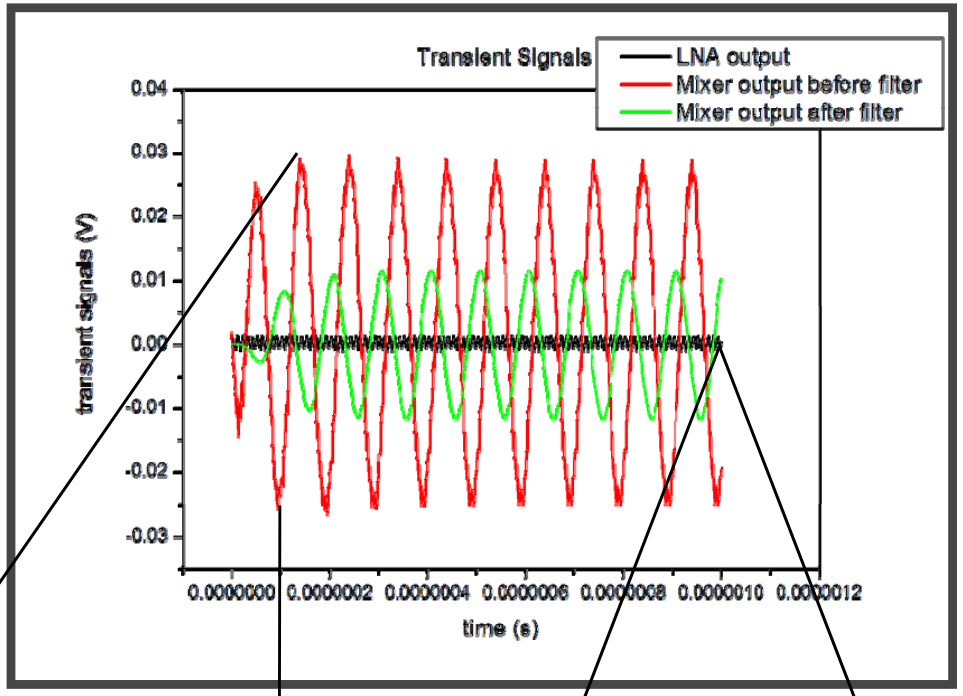
Input signal setting

- For RF input:
  V_{RF} = 1mV
- For LO input:
  V_{LO} = 0/1.0V (peak to peak)
- M1 and M2 are chosen long and wide transistors
- Switch transistors (M3~M6) are set appropriately



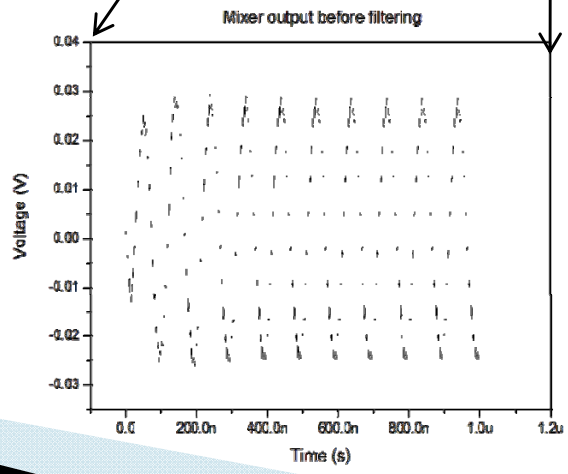
Transient simulation and Spectrum

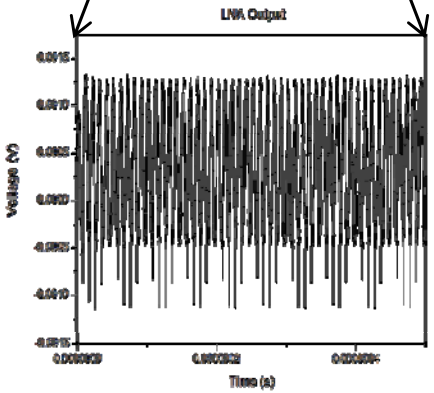




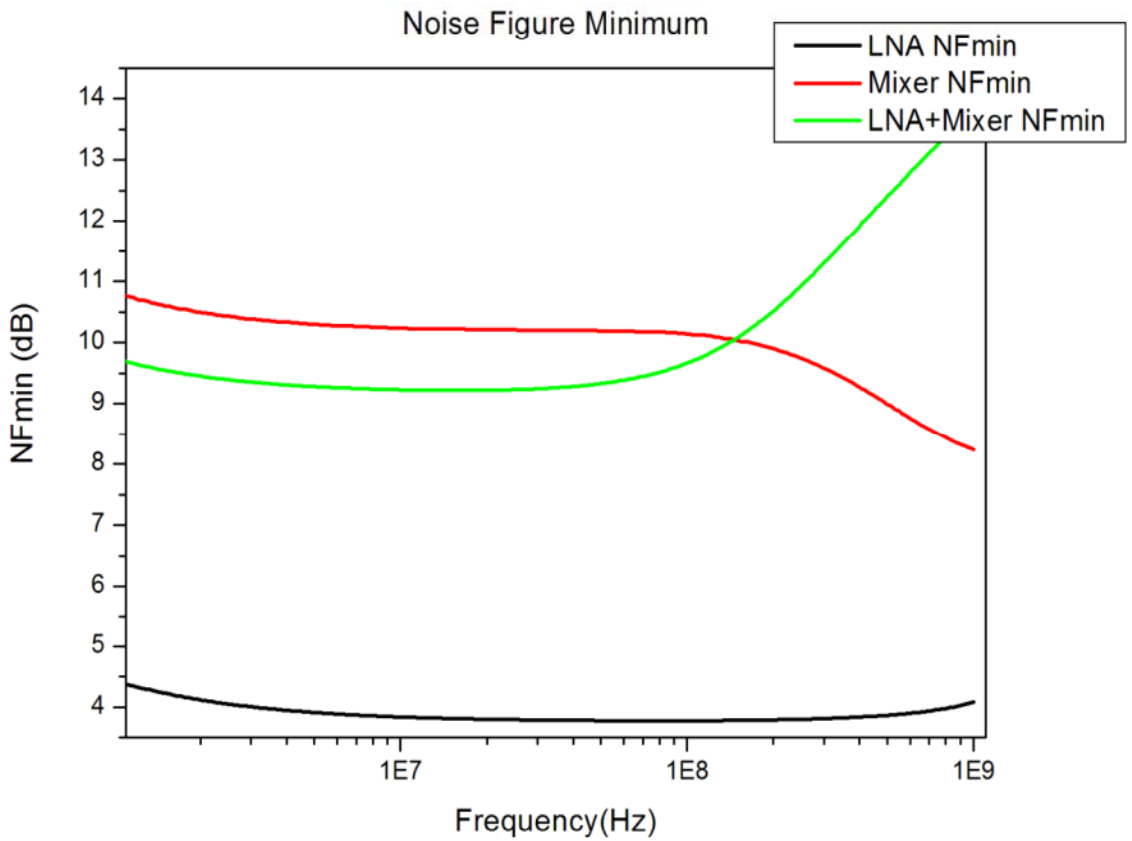
- Total Gain = -39.65-(79.32)=39.67dB

- Minus DC level





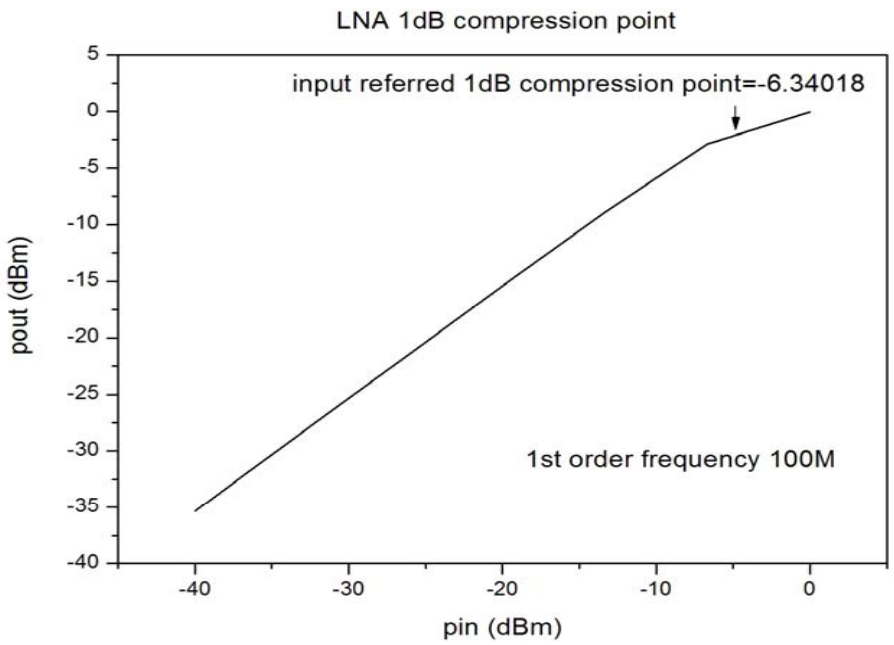
System Performance - Noise figure



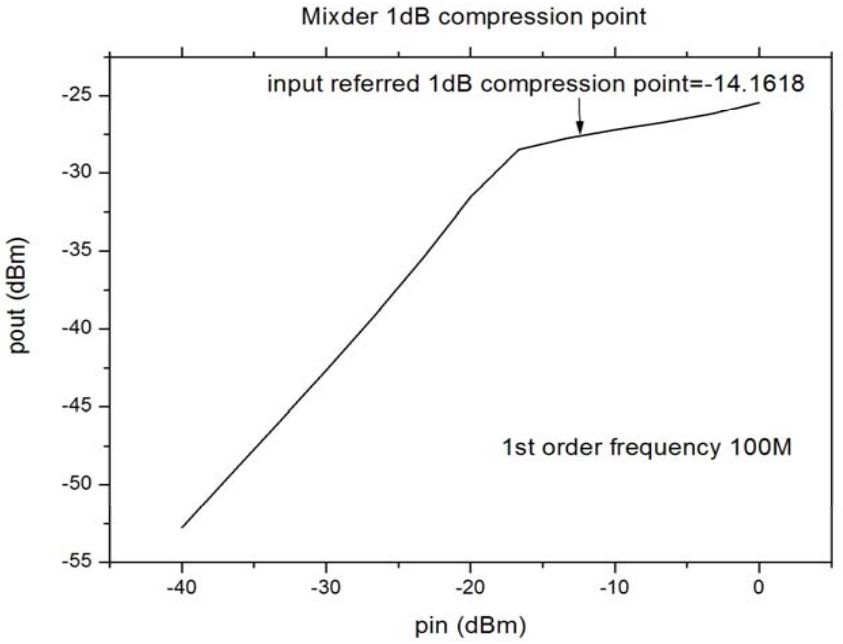
LNA: 3.77 dB
Mixer: 10.14 dB

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}}$$

System Performance - 1dB compression point



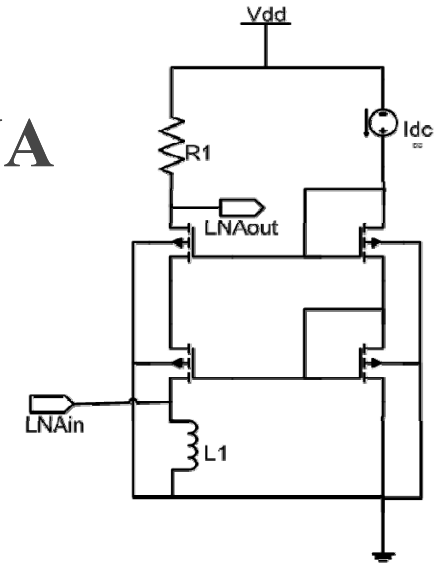
❖LNA 1dB-compression level



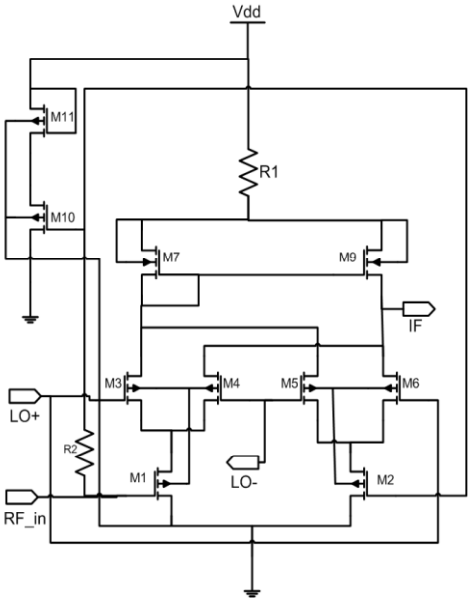
❖Mixer 1dB-compression level

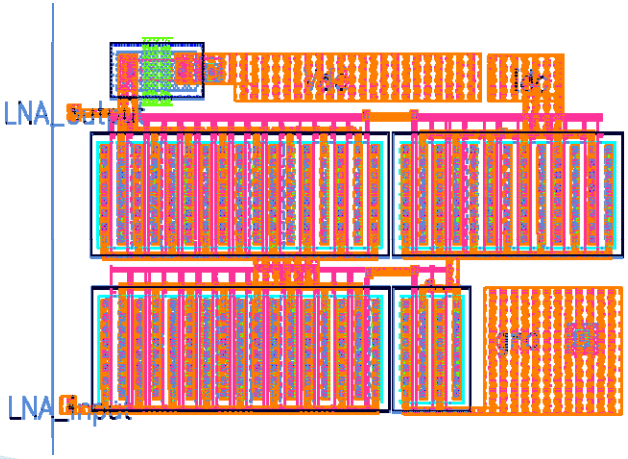
System Schematic and Layout

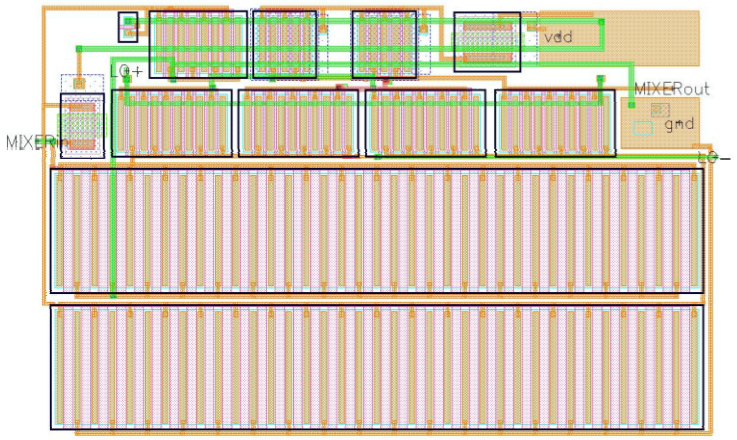
LNA



Mixer







Total specifications

LNA	This work	Karanicolas, A.N.
Power dissipation	3.9mW	20mW
Noise figure	3.77dB	1.9dB
AC Gain	22dB	15dB
Input 1dB compression level	-6.34dBm	-15.2dBm
Reflection coefficient $\lvert s_{11} \rvert$	-27.7dB	-
RF frequency	100MHz	900MHz

MIXER	This work	Zencir et al.
Power dissipation	3.105mW	5.4mW
Noise figure	10.14dB	5.8dB
Voltage gain	20.4dB	20.8dB
Input 1dB compression level	-14.16dBm	-21dBm
RF frequency	100MHz	435MHz

Conclusion

- System satisfies most of initial project specifications
  - Bandwidth, power consumption, gain…
- Possible improvements:
  - Mixer noise figure, on-chip inductor design
- Introduction to CMOS RF design

Thank You!