A CMOS LNA and Mixer for FM Receivers

Mao-Ter Chen, Wei-Ling Chiang, Yohan Kim
Introduction

- Continuous demand for high performance, low power RF circuits
- CMOS provides a favorable environment to integrate analog and digital on a single chip
- FM Band (88 – 108MHz)
Design goals

**LNA:**
- Input matching network (50Ω)
- Enough gain to overcome noise in later stages
- Low Power
- Linearity

**MIXER:**
- Translate the RF signals with minimal distortion
- High gain, low power consumption
LNA—Choosing Topology

- Why 2 stage cascode common gate?
- Isolation from output to input and better power supply noise rejection
- Increase output impedance
In RF applications, impedance is usually 50 Ω (matched to antenna)

\[ Z_{in} = \frac{sL}{sL(g_m + sC_{gs}) + 1} = 50 \]

Assume Cgs equals to 10pF,

\[ \omega_0^2 = \frac{1}{L_2C_{gs}} = \frac{1}{10^{-11} \times L_2} = (2\pi \times 100 \times 10^6)^2 \]

\[ \Rightarrow L_2 = 253.3\, nH \to off-chip \]
LNA - Gain

- Gain $A_v = \frac{g_m g_{m1} R_1}{g_{m1} + s C_{gs1}} \approx g_m R_1$

  Too high: early mixer saturation and bad linearity
  Too small: NF of whole system increases

- Ideally, $A_v = 15 \div 20\, dB$
- Our design: $A_v = g_m R_1 = 20 \log(0.022 \times 600) = 22\, dB$
S-Parameter and stability

For unconditional stability,

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\square|^2}{2|S_{12}S_{21}|} > 1 \]

\[ |\square| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \]
Mixer—down conversion

- Simple switch as a mixer
- Implementation with NMOS

\[ V_{IF}(t) = K V_{RF}(t)V_{LO}(t) = K \cos 2\pi f_{RF} t \cos 2\pi f_{LO} t \]
\[ = \frac{K}{2} [\cos 2\pi (f_{RF} - f_{LO}) t + \cos 2\pi (f_{RF} + f_{LO}) t] \]

- RF frequency = 100MHz
- LO frequency = 90MHz
- IF frequency = 10MHz
Mixer Topology

- Active double balanced mixer Gilbert Cell
- Rejection of LO coupling
- Single-ended I/O port

● DC bias circuit
● Current mirror
● R1 for output voltage level
Input signal setting

- For RF input:
  \[ V_{RF} = 1\text{mV} \]
- For LO input:
  \[ V_{LO} = 0/1.0\text{V (peak to peak)} \]
- M1 and M2 are chosen long and wide transistors
- Switch transistors (M3~M6) are set appropriately
Transient simulation and Spectrum

- Total Gain = -39.65 - (79.32) = 39.67 dB
- Minus DC level
System Performance - Noise figure

LNA: 3.77 dB
Mixer: 10.14 dB

\[ NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}} \]
System Performance - 1dB compression point

- LNA 1dB-compression level
- Mixer 1dB-compression level
System Schematic and Layout

LNA

Mixer
## Total specifications

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<th>This work</th>
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<td><strong>Power dissipation</strong></td>
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<td>3.9mW</td>
<td>20mW</td>
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<td><strong>Noise figure</strong></td>
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<td>3.77dB</td>
<td>1.9dB</td>
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<td><strong>AC Gain</strong></td>
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<td>22dB</td>
<td>15dB</td>
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<td><strong>Input 1dB compression level</strong></td>
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<td>-6.34dBm</td>
<td>-15.2dBm</td>
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<td>**Reflection coefficient</td>
<td>$</td>
<td>s_{11}</td>
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<td><strong>RF frequency</strong></td>
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<td>900MHz</td>
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<td><strong>Power dissipation</strong></td>
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<td><strong>Voltage gain</strong></td>
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<td><strong>RF frequency</strong></td>
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Conclusion

- System satisfies most of initial project specifications
  - Bandwidth, power consumption, gain…

- Possible improvements:
  - Mixer noise figure, on-chip inductor design

- Introduction to CMOS RF design
Thank You!