A High Frequency CMOS Low Noise Amplifier Design for Cellular Applications

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Motivation for LNA

- LNAs offer good compromise between noise performance and high gain amplification

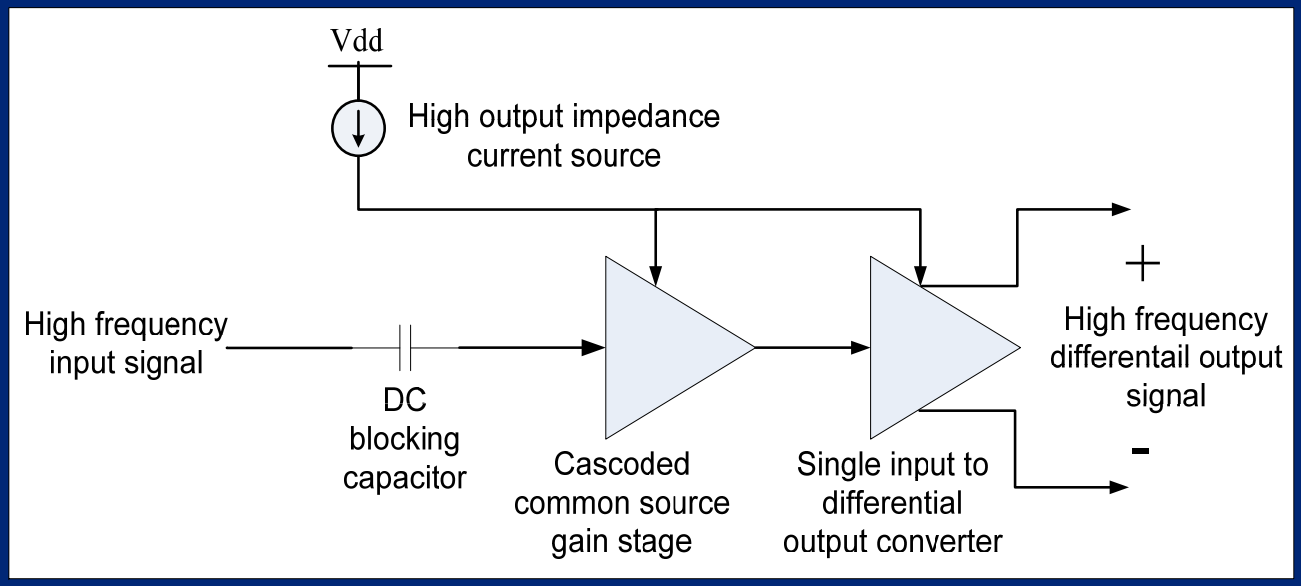
- Cellular technology (both basestation and handset) require LNAs to:
    - Increase connection range (for a given SNR)
    - Reduce dropped calls
    - Improve blocking performance
    - Improve call performance and connection quality

- Demand for size, cost, and complexity reductions motivate integration of LNA into CMOS technology

LNA System Block Diagram

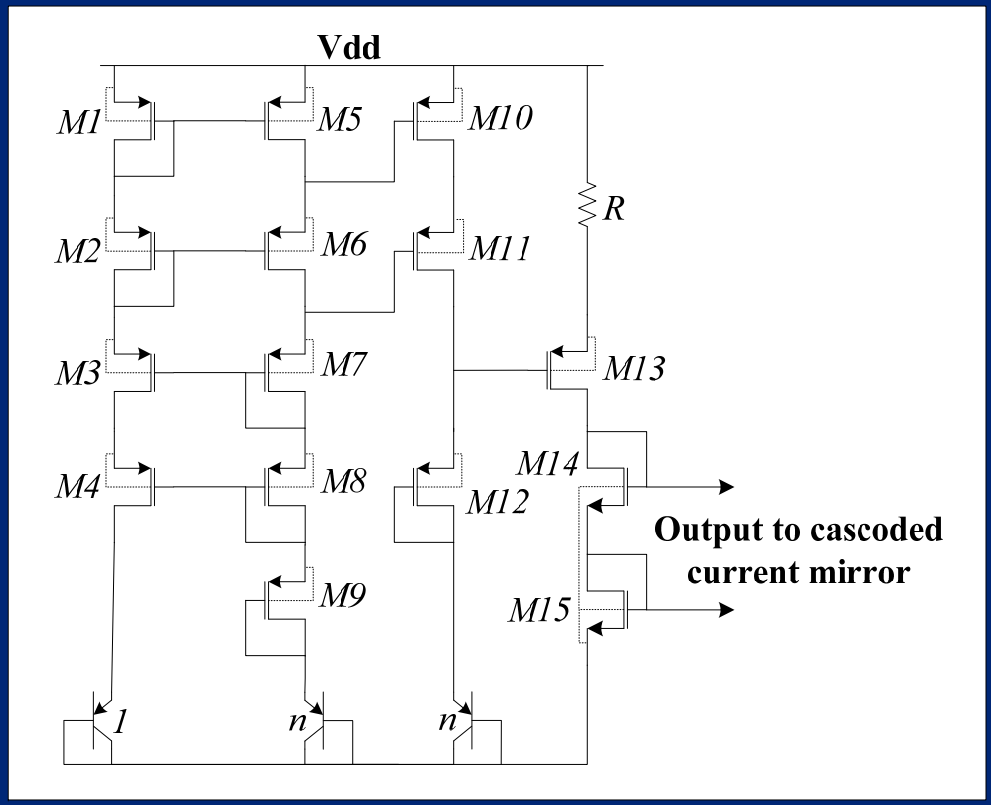
- Design consists of:
  - Band-gap reference current source
  - Cascoded common source gain stage with input matching
  - Single input to differential output converter

- Operates in EGSM cellular band for uplink from handsets to basestation (880 – 915 MHz)



Band-gap Reference Current Source Operation

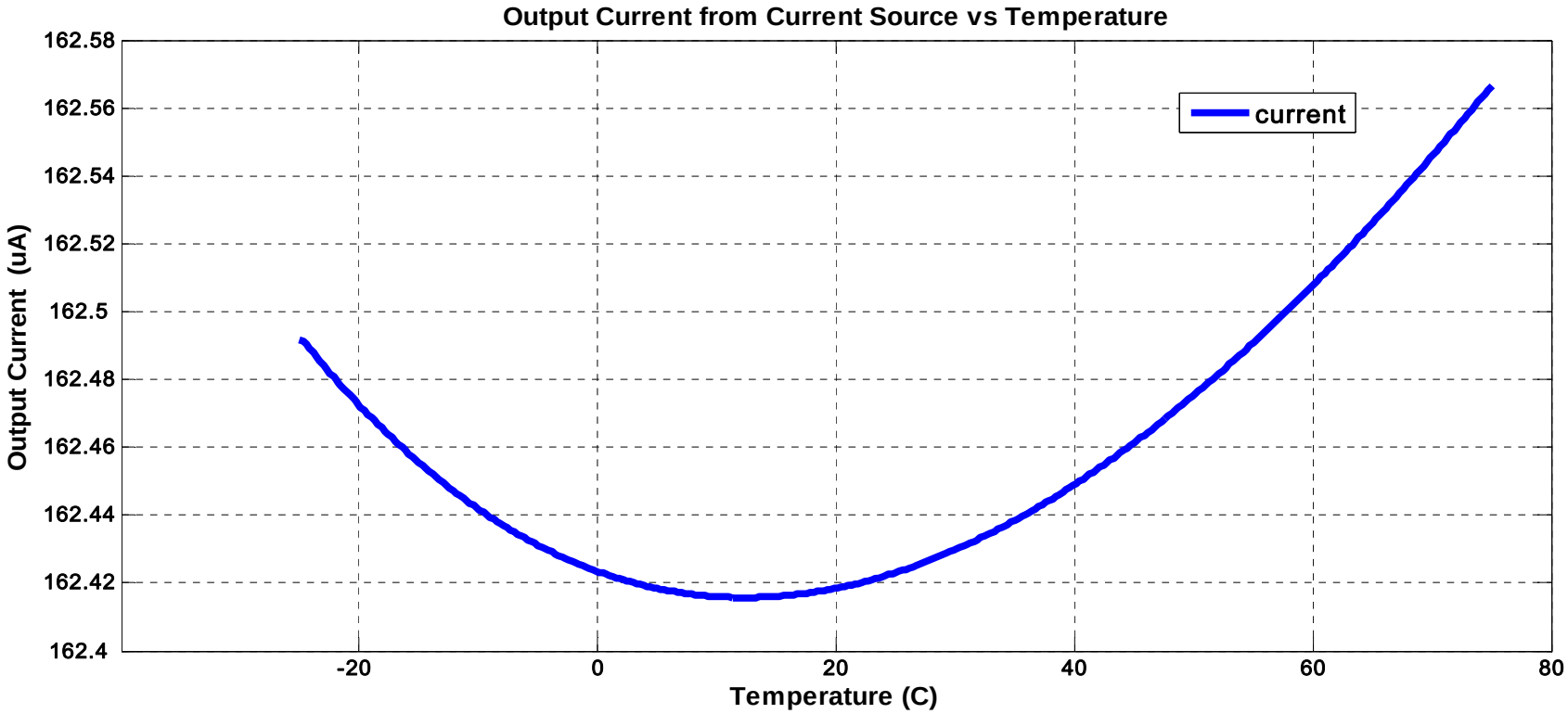
- Cascoded self-biasing network produces supply insensitive currents
- Differences in current densities across parasitic pnps produce gate bias voltage on *M13* with tunable temperature coefficient
- Ratio of resistance of *M12* and *M9* cancels temperature dependence of output current



Current Source Performance

- Current source provides near temperature independence over all realistic temperatures

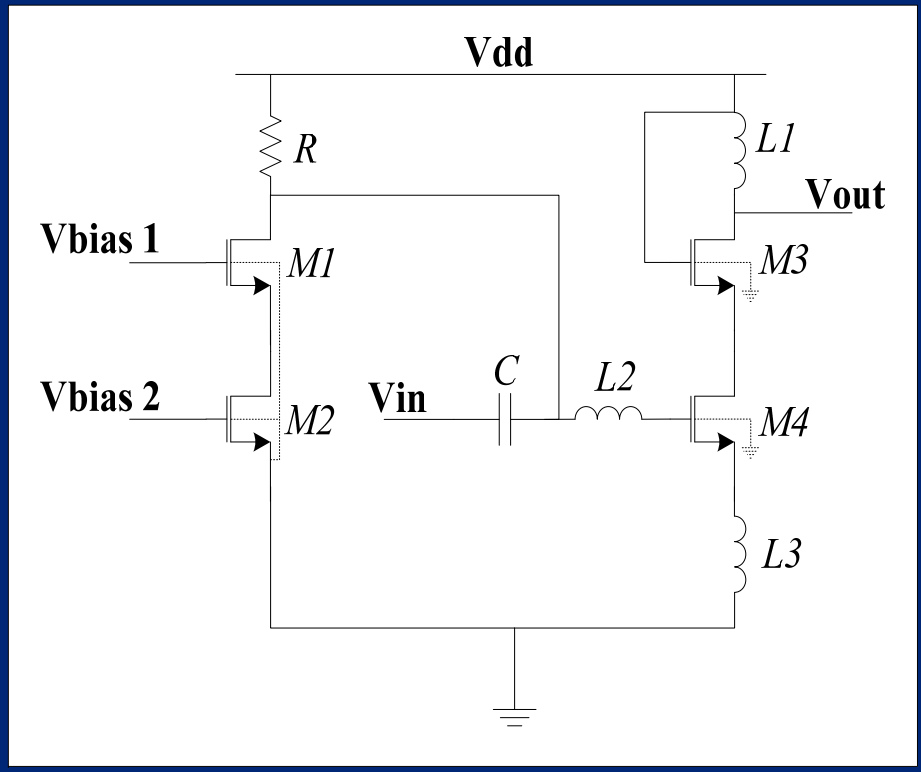
- Cascoded output mirroring provides higher output impedance for biasing networks and tail current



LNA Block Operation and Matching

- Cascoded NFETs provide:
  - Increased unilaterality for input/output isolation
  - Reduced Miller mulitplied C_{gd}, which increases unity gain frequency ω_t

$$\omega_t = g_m/(C_{gs} + C_{gd})$$

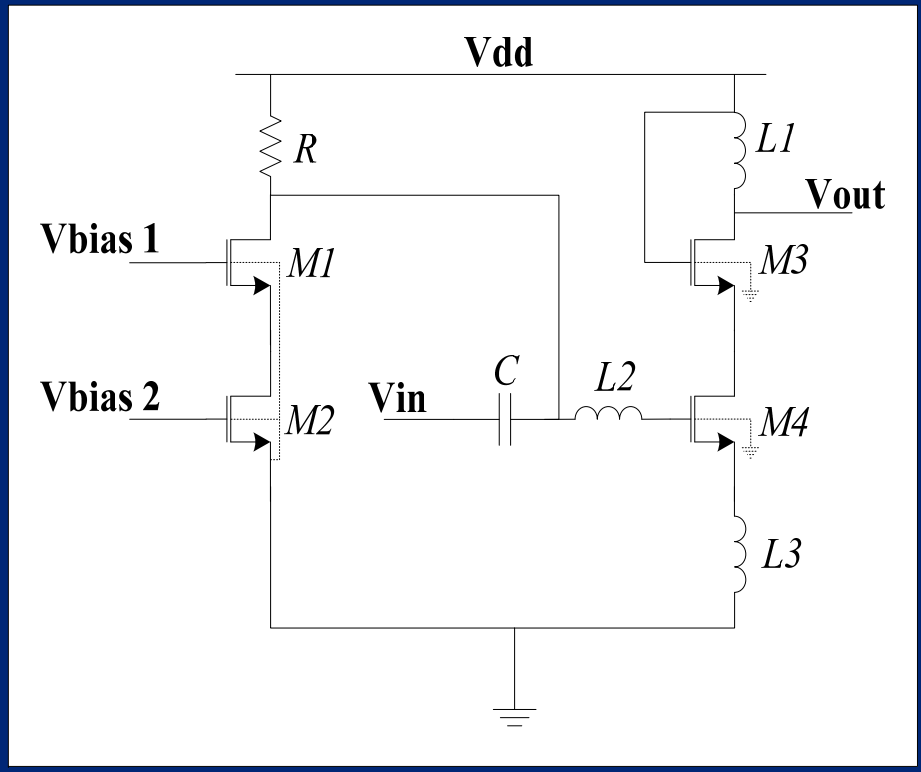


- Input capacitor acts as dc blocking capacitor and is implemented off-chip

Cascoding → decreases C_{gd} → increases ω_t → Decreases Noise Factor!

LNA Block Operation and Matching

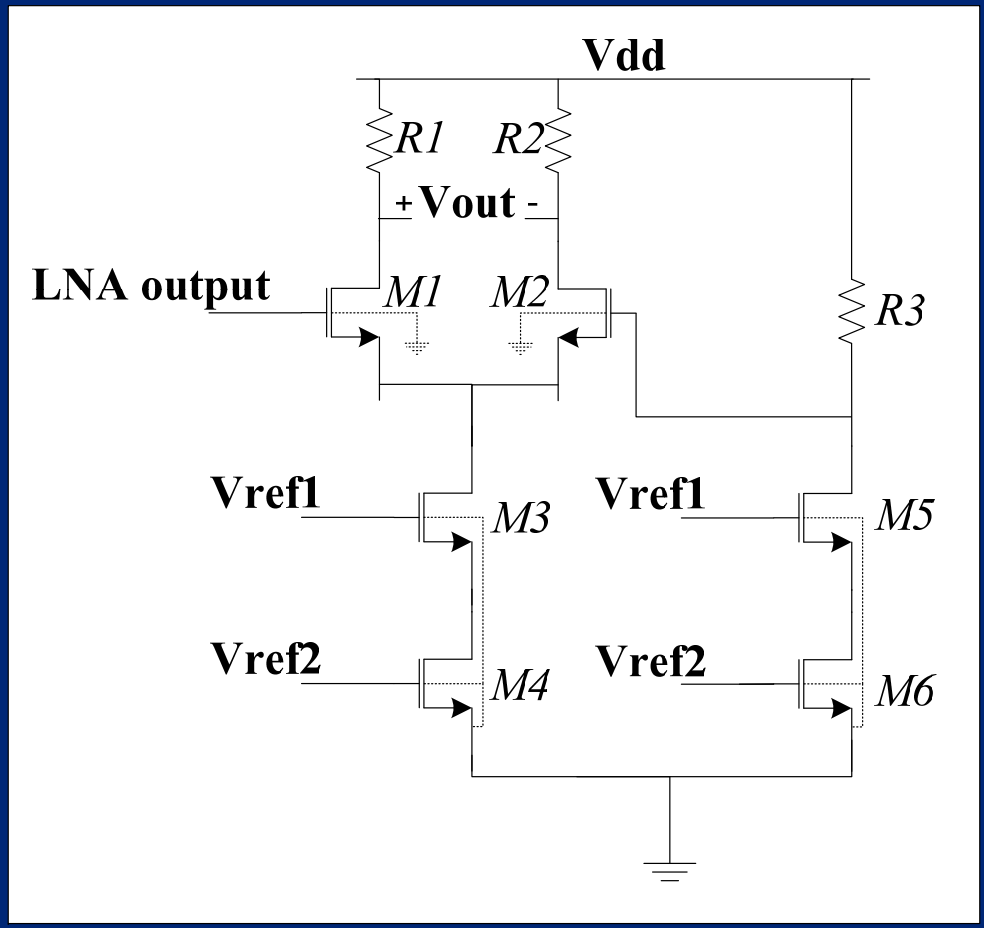
- *L2* and *L3* used to match input impedance to 50Ω with:
  - $Z_{in} = sL_s + 1/(sC_{gs}) + (g_m L_s)/C_{gs}$
- Drain inductor used to increase match bandwidth and filter output
- Width of NFETs were optimized for power constrained noise performance using:
  - $W_{opt} = 1/(3\omega L C_{ox} R_s)$



Noise Figure = 2.8dB
Gain = 18.9dB

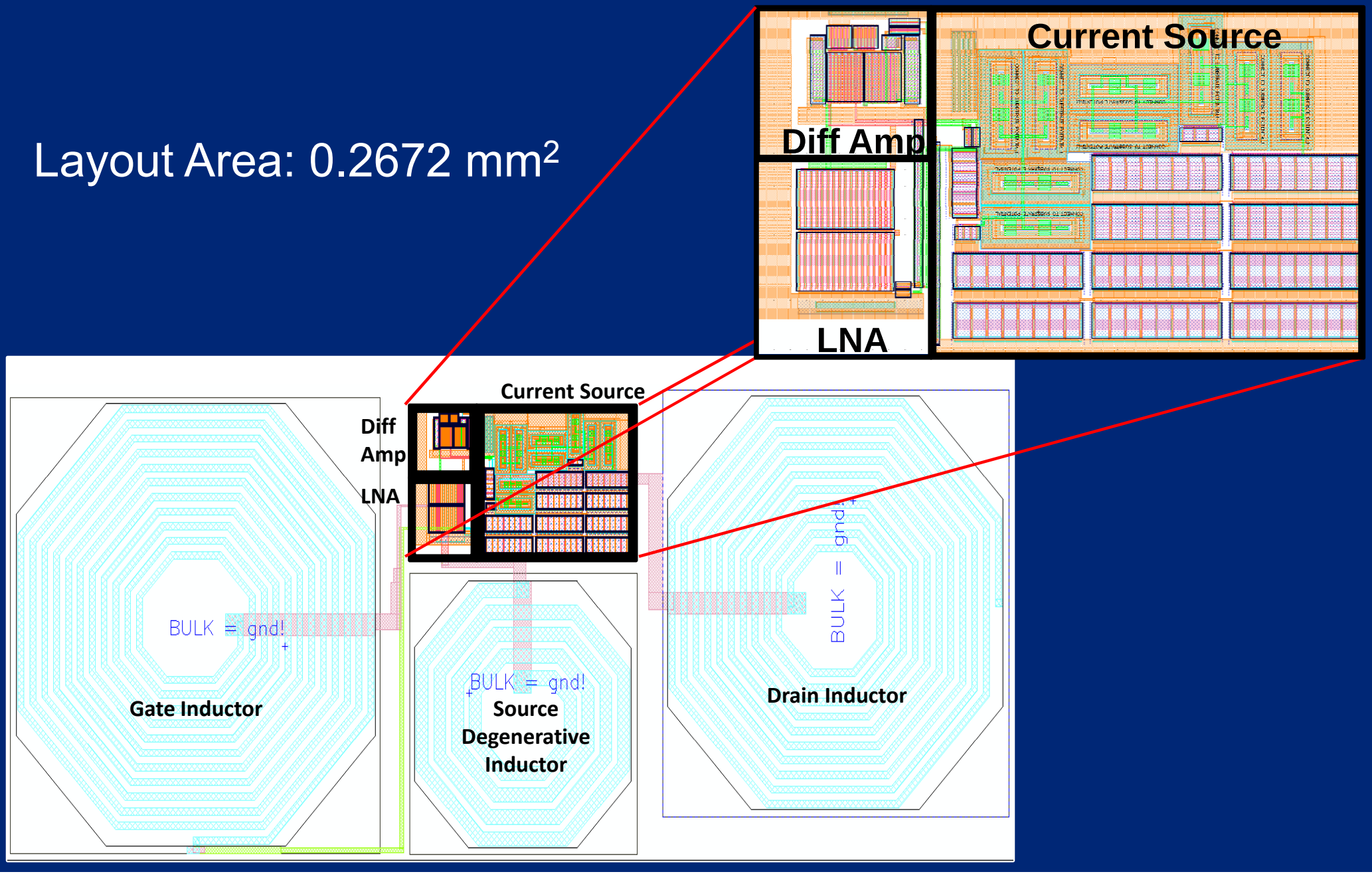
Single Input to Differential Output Converter Operation

- Composed of differential amplifier with LNA output applied to *M1* and ac ground applied to *M2*
- A dc biasing network was designed to match the dc bias points of *M1* and *M2*
- Cascoded mirror makes tail current source more ideal

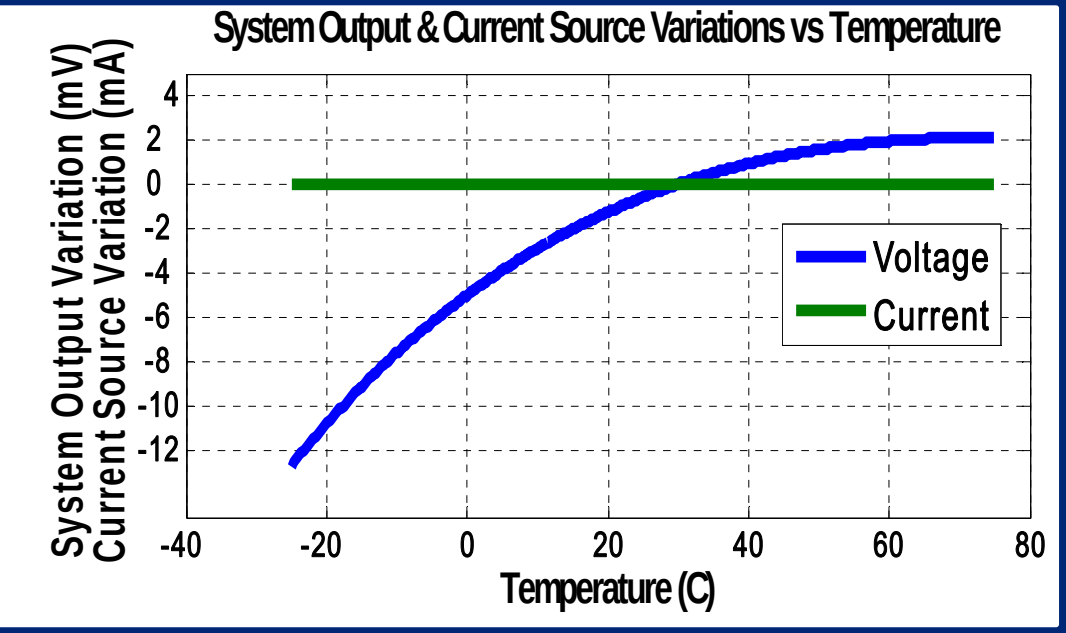


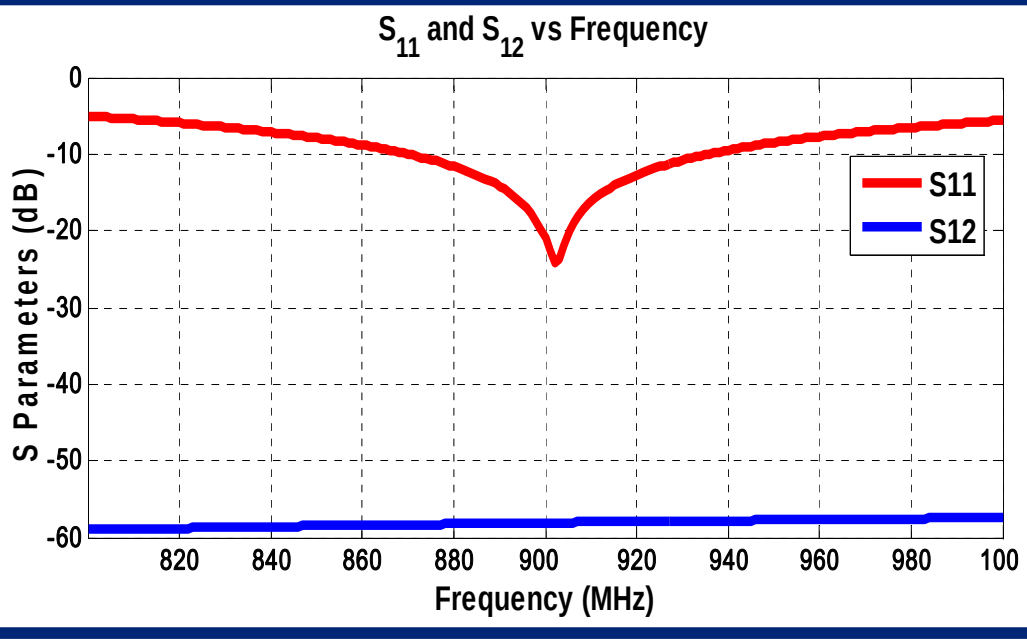
Overall LNA System Layout

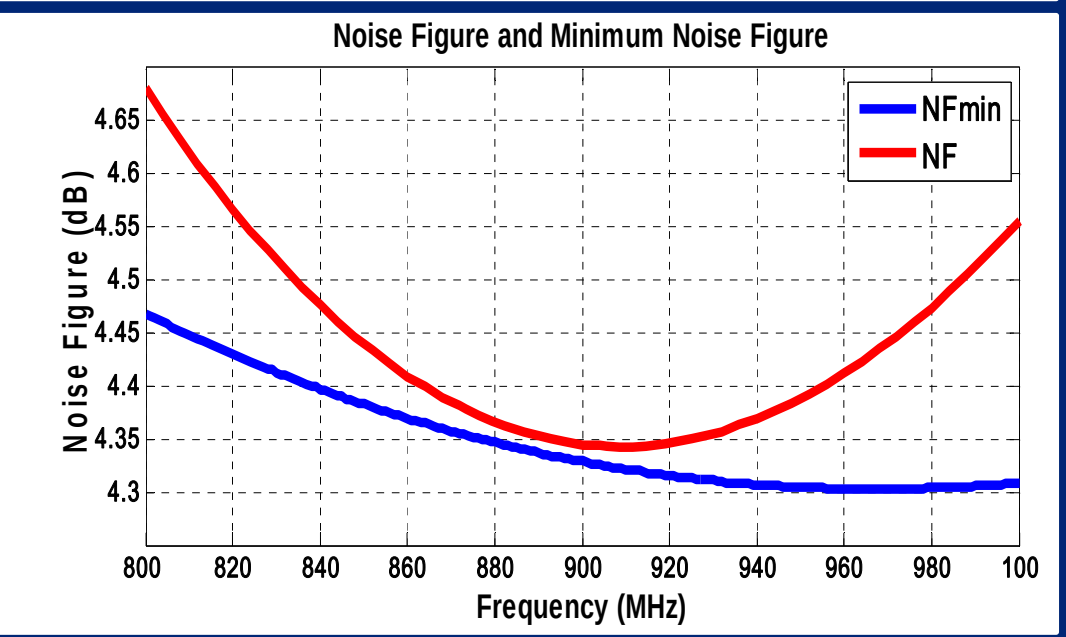
Layout Area: 0.2672 mm²

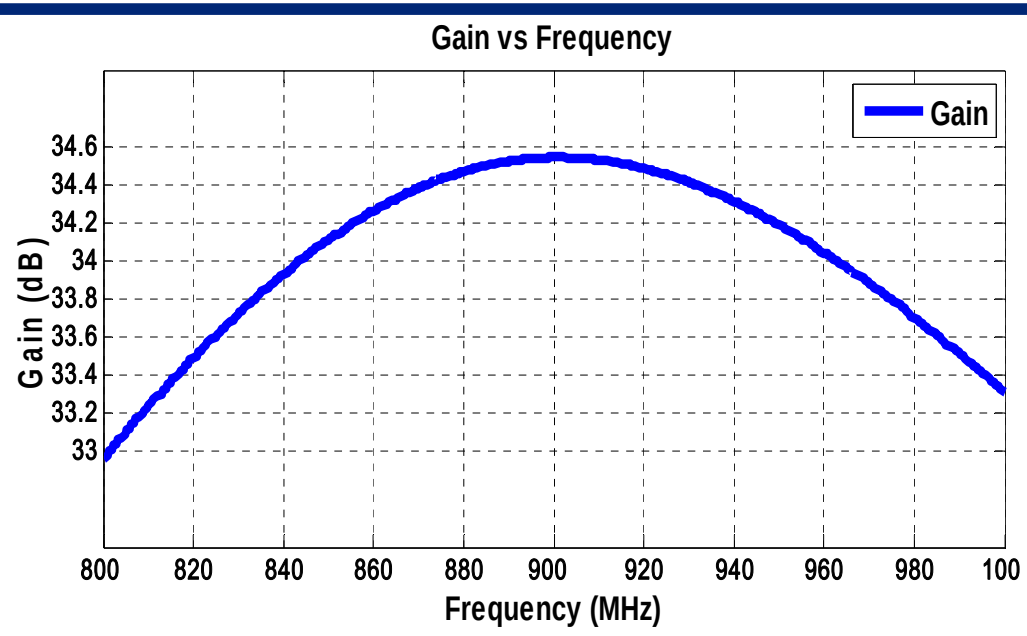


Overall LNA System Performance









LNA System Specifications

Specification	**Value**	**Units**
Power Consumption	25.74	mW
Max Gain in Passband (A_v)	34.55	dB
Gain Ripple over Passband	0.08	dB
Maximum System Noise Figure in Passband	4.366	dB
Maximum S_{11} in Passband	-11.61	dB
-10dB Bandwidth for S_{11}	65.0	MHz
Maximum S_{12} in Passband	-57.97	dB
Current Source Output Temperature Variation	150.82	nA
System Differential Output Voltage Temperature Variation	14.768	mV
Overall Layout Area	0.2672	mm^2
DRC and LVS Clean Final Design	yes	n/a

Conclusions and Further Considerations

- CMOS LNA design meets all performance specs
  - LNA could find great use in cellular applications
- LNA system meets most 2σ process corner specs, but exceeds ±0.5dB gain ripple in the passband for a few corner sims
  - Unimportant since VGAs in baseband circuitry can adjust for the small variation
- Did not consider an output match for our system
  - Acceptable since most wireless receiver LNAs drive on-chip components such as a FET gate in a mixer stage, making a 50Ω output match superfluous

Acknowledgements

We would like to sincerely thank Professor Wentzloff and Danial Ehyaie for their patience, guidance, and enthusiasm over the course of this project and this semester.