SRAM Sense Amplifier

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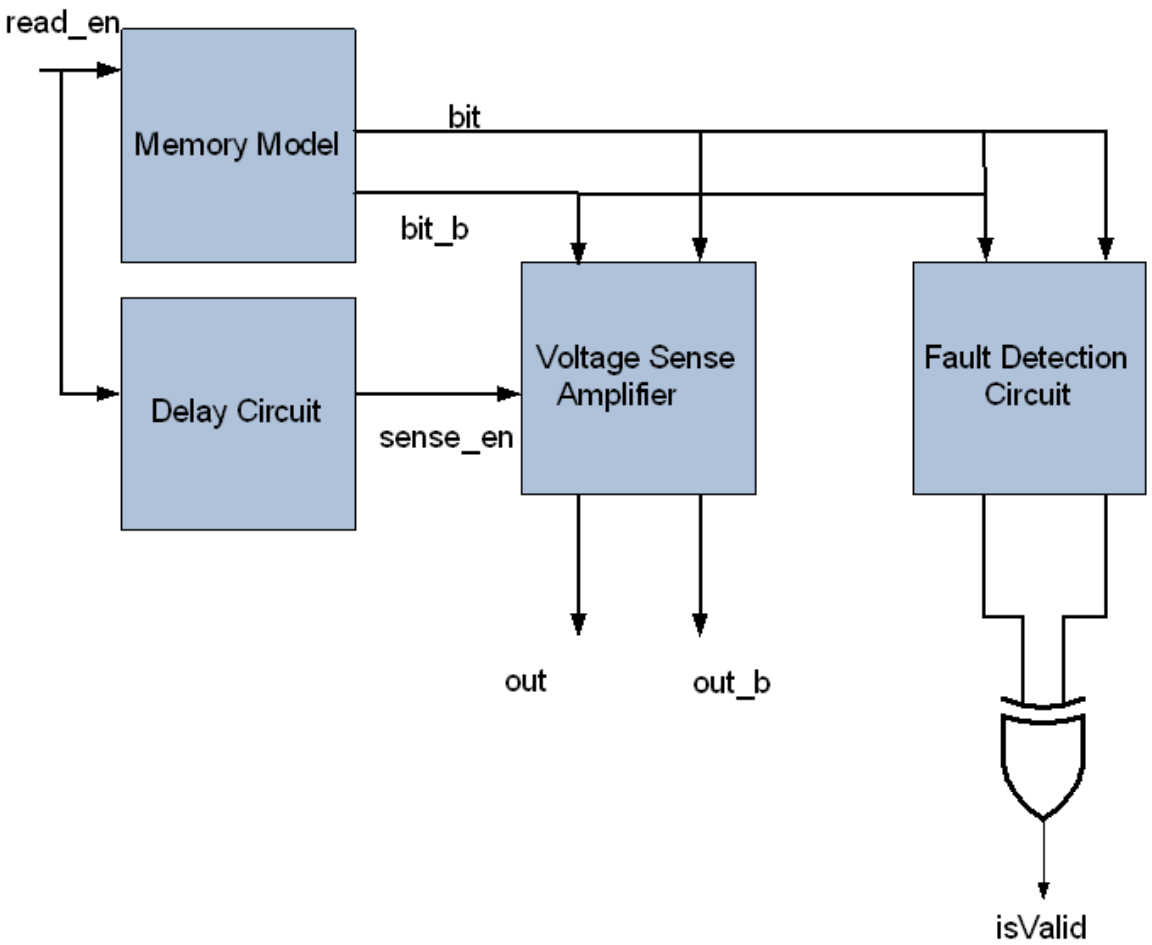
Introduction

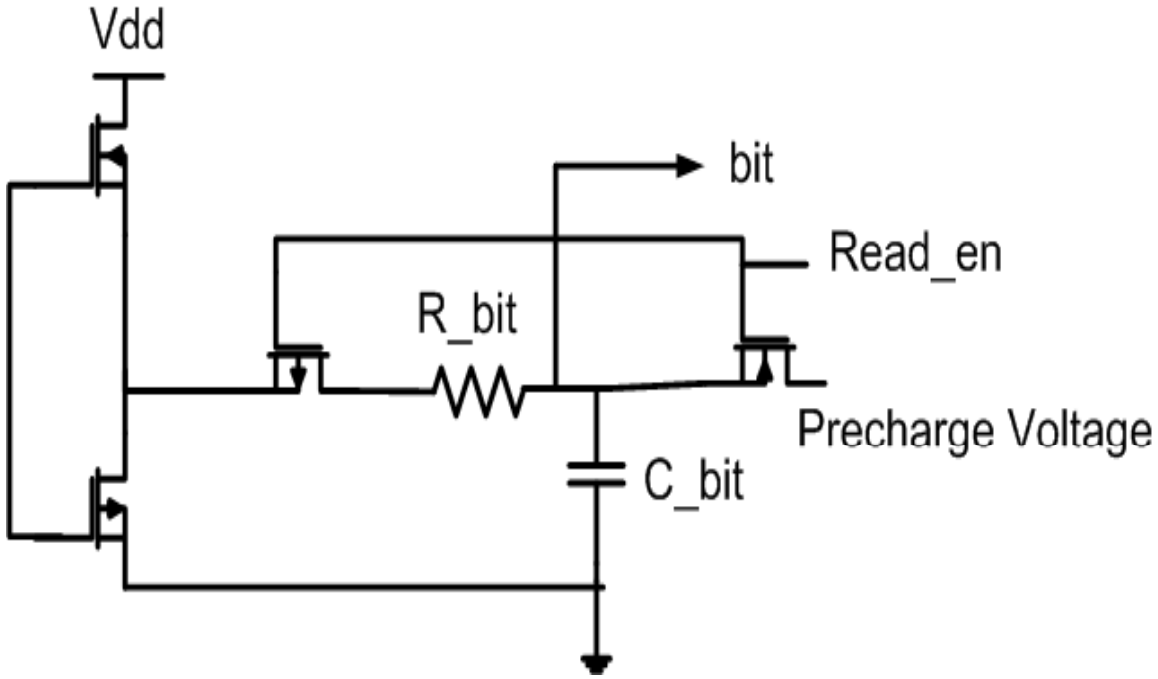
- Sense amplifiers are important circuit elements in memory design
- The aim of the project is to design a high yield and high speed voltage sense amplifier to detect change in data and the data bar lines during a read operation.
- The fault detection circuit is also designed to detect the validity of the data presented to the sense amplifier.

Block Diagram



- Memory Model simulates the input to the sense and the fault detection circuit
- Delay circuit provides the enable signal so that the input signal difference is above the noise threshold.

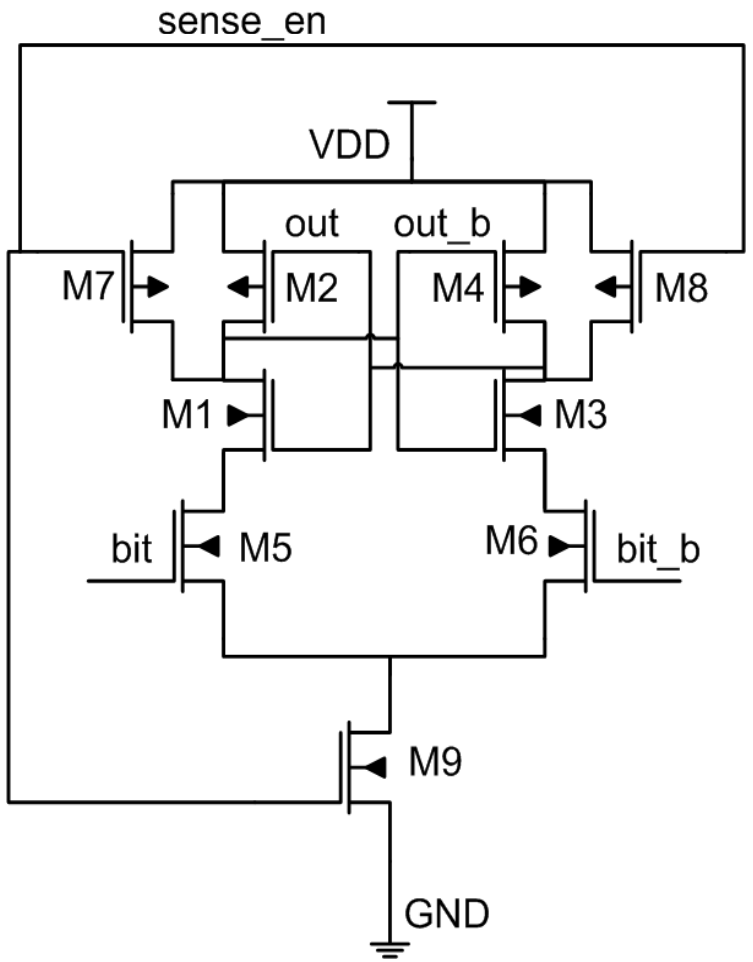
Memory Model



- Bit Line resistance and capacitance calculated for 512 word SRAM cell
- Precharge voltage was set to 1.15 V

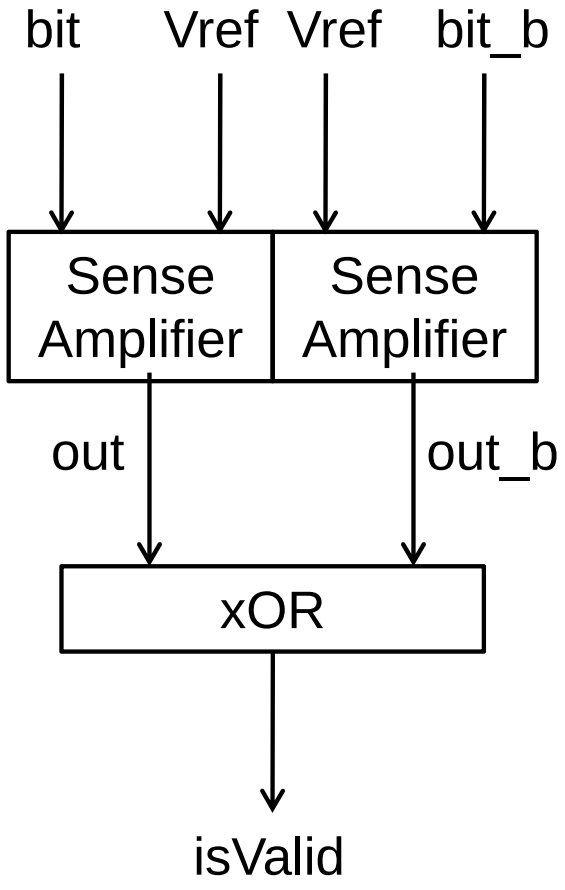
Sense Amplifier

- Outputs precharged to VDD
- M9 foot enabled, M7, M8 precharge stopped
- M5, M6 inputs control bias currents, ΔVout
- M1, M2, M3, M4 cross-coupled inverters drive full-rail swing at Vout
- Offset voltage issues/mitigation techniques



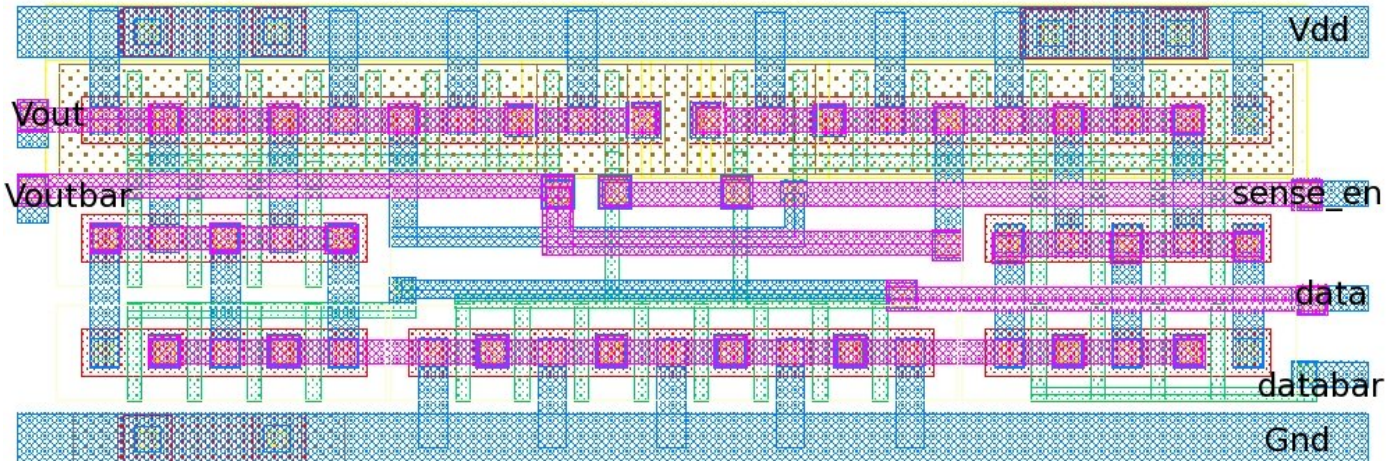
Fault Detection

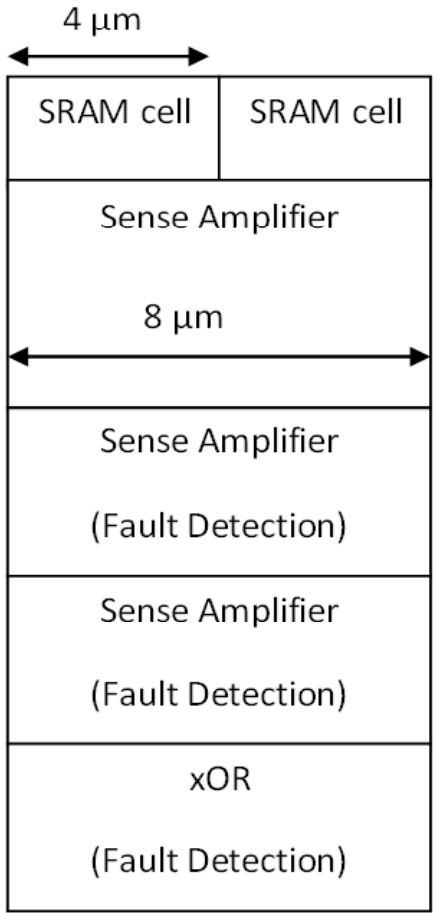
- Want to find bit errors (bit == bit_b)
- Two sense amplifiers with Vref (1.15 V) input
- Sense bit/bit_b lines independently
- Results are xORed to check if data is valid



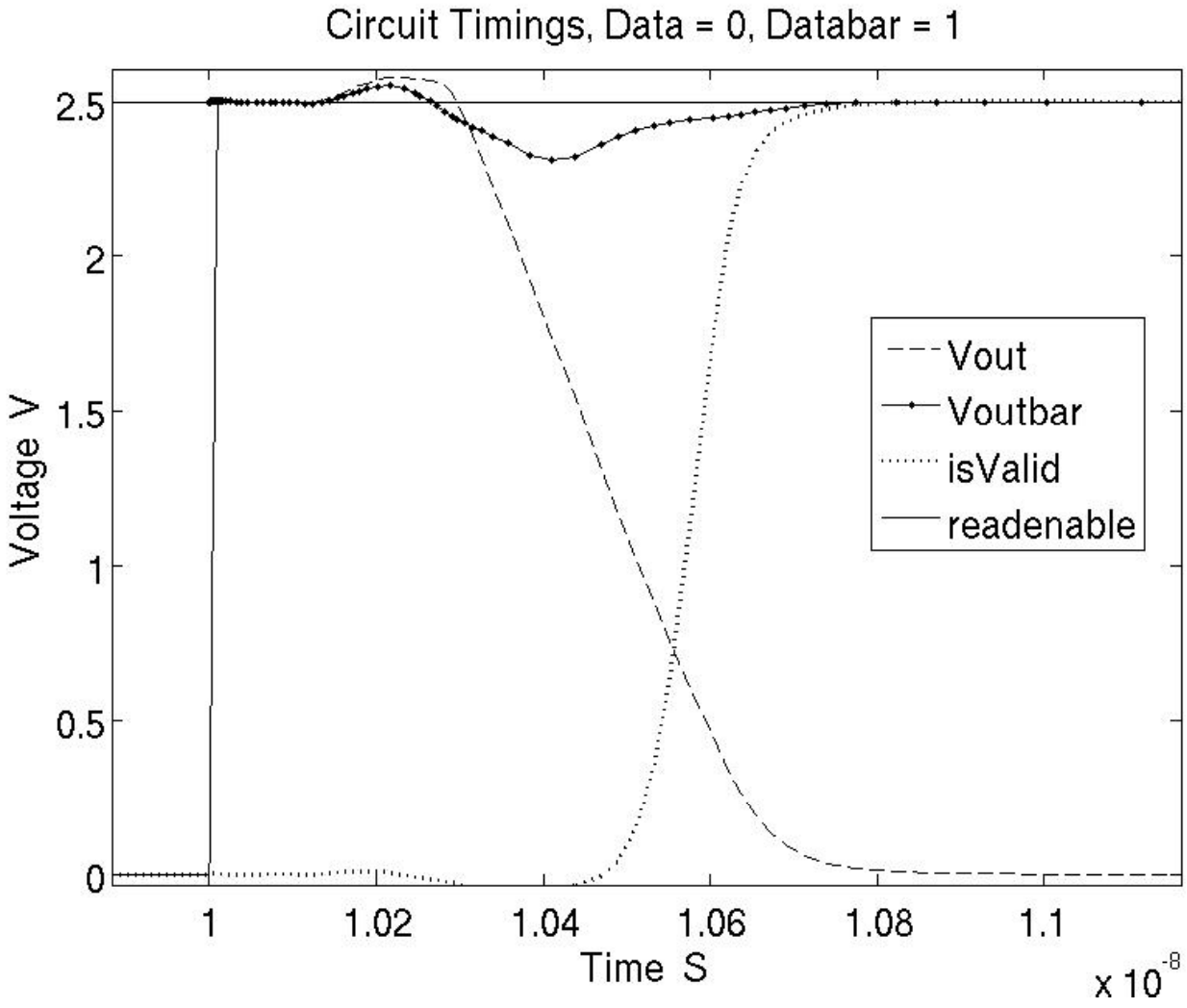
Floorplan

- 2X bit-slice, can stack 2 vertically
- Only 1 VDD, 1 GND rail
- Very regular topology
- Attaches to bottom of SRAM core

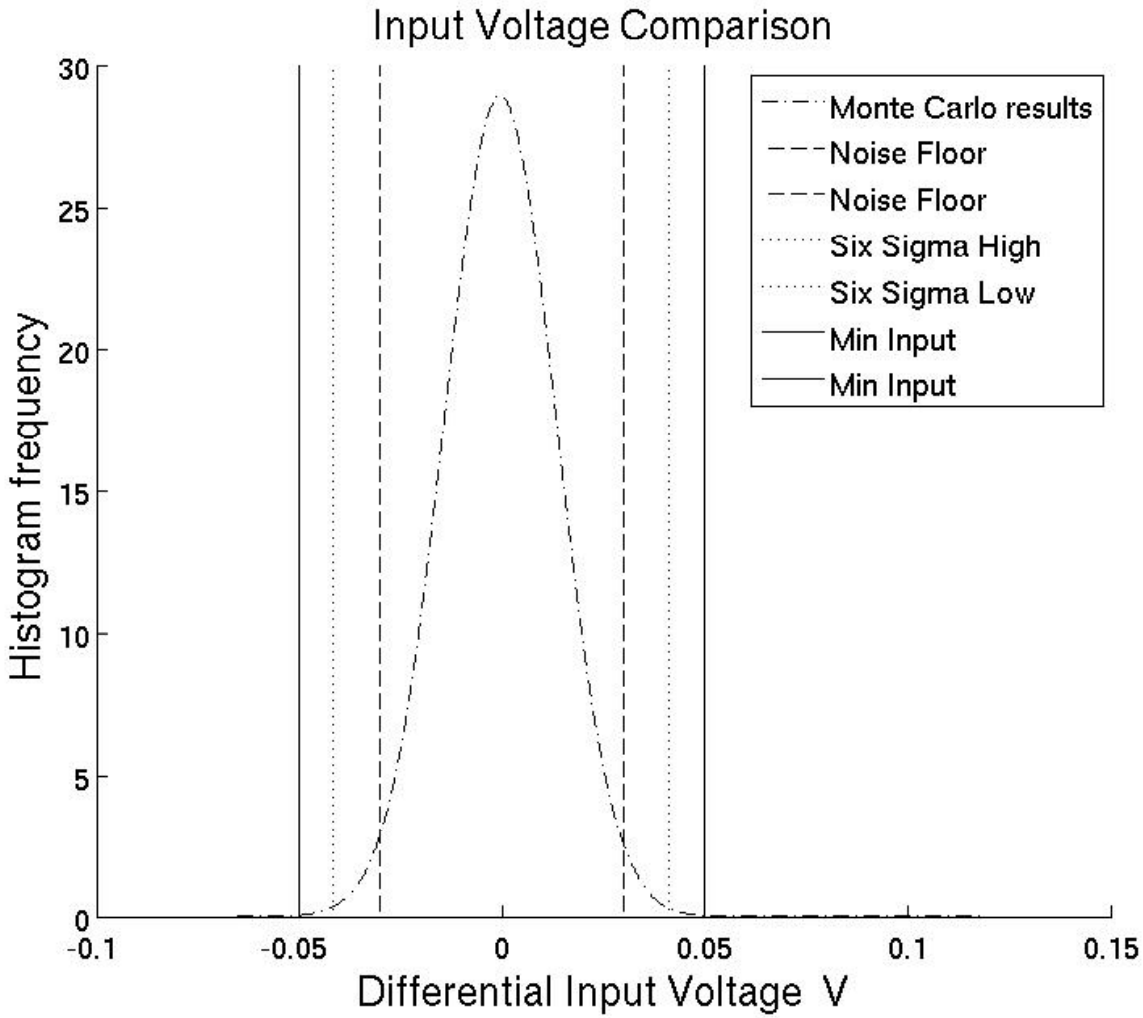




Transient Results



Critical Voltage Comparison



Important Timings / Voltages

Characteristics	Simulated Results
Read enable- sense enable delay	200 ps
Read enable- data output delay	475 ps
Read enable- fault detection delay	575 ps
XOR delay	100 ps
Sense amplifier differential Input	250 mV
Fault detection differential Input	50 mV
Noise Floor	30 mV
6σ offset voltage	±40 mV