A CMOS Digitally Controlled, Low Power, Variable Gain Headphone Amplifier

Jonathan Yamoty, David Bowlus, Lu Luo

Motivation and Scope

The device we are designing is a low power headphone amplifier with digitally adjustable volume control. This device is meant to take the output of a portable mp3 or CD player and amplify it to a pair of headphones. The design must be compact and use low power since it will be used in portable applications. It will have linear gain and low distortion in order to provide reliable volume control and good sound quality. The overall gain of this device will vary from 0dB (no amplification) to 20dB, which is typical for a headphone amplifier. We will set the input and output impedances to match typical headphone impedances (75-150 Ohms).

Circuit Topology

The schematic of our circuit is shown in Figure 1. The circuit consists of four stages. The first stage is used to mirror currents and to generate a voltage bias for other stages. The second stage is the input stage, which is used to set the input impedance and to produce gain. The third stage is the volume control stage, which is used to adjust the volume by attenuating the gain produced by the first stage. The fourth stage is the output stage, with is used as a buffer and to set the output impedance.

The Current Source/Bias Generation Stage

This stage uses current mirrors to supply currents to each of the other stages. The width and length ratios are adjusted in order to supply the desired current to each stage. This stage also supplies the input stage bias voltage and the gate voltages to each stage. These voltages were chosen in order to maximize headroom and ensure that the transistors stay saturated.

The Input Stage

The input stage is used to match the output impedance of a music device and set a high, positive gain. We designed the input impedance to be 100 Ohms, which is within the range of typical impedances for headphones. This stage uses a common gate with degeneration topology. We chose this topology for the relatively low input impedance that is determined by 1/ (gm1 + gmb1) of the common gate transistor and relatively high output impedance. This stage uses a diode-connected device for the drain resistor in order to eliminate the use of a resistor in the design. This diode connected device also allows us to set the output impedance of this stage to be approximately 1/gm2. The gain of the common gate is determined by (gm1 + gmb1)*(R_L). Since the load resistor in this case is a diode-connected transistor, the impedance is set by 1/gm2. This results in the gain being approximately (gm1 + gmb1) / gm2, with 1 being the common gate transistor and 2 being the diode-connected transistor. This configuration allowed us to set the gain of this stage to be approximately 23.0dB.

The Volume Control Stage

This stage is a common source stage with degeneration and a diode-connected load. Since the input impedance is into the gate, it is approximately infinite and does not affect the gain of stage 1. The gain of this stage is approximately –gm*Rd/(1+gm*Rs), with Rd being the 1/gm of the diode-connected transistor, and Rs being the ro of the current mirror transistor (see Figure 1). The adjustable gain is achieved digitally by switching the current mirror transistor used to supply current. The block diagram of the digital volume control is shown in Figure 2. The volume control is a digital three bit multiplexer that selects one of eight possible current mirrors, which give eight gain choices. We stacked transistors over each current mirror transistor and gave them a gate bias voltage of Vdd or 0V, such that they are either in linear mode or cutoff and basically behave as switches for each current. The digital control (or a MUX) supplies these voltages in order to select the desired gain setting. The selectable gains can be seen in Figure 4. The gain of this stage is adjustable from -0.77dB to -20.89 dB in order to achieve an overall gain of 0dB to 20dB.

The Output Stage

The output stage is a buffer used to set the desired output impedance. This stage is a source follower, which has an output impedance of approximately 1/gm of the current mirror transistor and has an infinite input impedance. This allowed us to set the output impedance to the desired value of 100 Ohms. Since the gain is determined by gm/(gm+gmb) (the gm of the SF transistor), it is not possible to attain a gain of 1. We achieved a gain of -2.441dB (a gain of approximately 0.775) for this stage, which is why the gain of the input stage had to be around 23dB to compensate for an overall gain of 20dB.

Simulation Results

The design goal was to build a headphone amplifier that meets certain specifications for power consumption, overall gain, input and output impedance, linearity, and total harmonic distortion. We wanted to attain a maximum gain of 20dB, and we achieved a maximum gain of 19.78dB. We designed the minimum gain to be 0dB and obtained a minimum gain that ranged from -0.2711dB to 0.513dB over our desired frequency range. We met our desired frequency range of 100 Hz to 23 KHz, which is the typical range for audio applications. We designed for an input impedance of 100 Ohms and obtained a value of 98.38 Ohms in our simulations. We also designed the circuit to have an output impedance of 100 Ohms and realized a value of 100.3 Ohms in our circuit testing. One of our major design goals was to minimize power consumption, since this device is meant to run on batteries in a portable application. We set the goal at using less than 6 mW for total power consumption and realized a total power consumption of 3.77 mW in our simulations at maximum gain. We planned to make the maximum input signal 50 mV, but achieved a maximum input signal of 40 mV for a linear output (see Figure 5). In addition, we wanted to achieve a circuit that would have a total harmonic distortion (THD) of less than one percent. We attained a THD of 0.7537% with an input signal of 1 mV.

Process Corners Variation

We ran our design through the process corners (FF and SS from 0-75˚C) at max gain. A summary can be found in Figure 6. We found that all parameters were within acceptable ranges except at SS_75˚C, where input impedance was high (500.1 Ohms) and gain was very low (2.568dB). However, this result is reasonable because our amplifier would not need to run at such a high temperature. Also, other variations in gain can be compensated by adjusting the volume.

Conclusion

The design circuit meets all requirements except for maximum input signal, which suffered from non-linearity. These results can be seen in Figure 7. Overall, the device can be used to one's satisfaction in amplifying a signal from a portable music device to a set of headphones.

References

[1] Razavi, Behzad. Design of Analog CMOS Integrated Circuits. Signapore: McGraw-Hill Higher Education, 2001.

[2] Jaeger, Richard. Microelectronic Circuit Design. New York: McGraw Hill, 1997.

[3] Baker, R. Jacob. CMOS: Circuit Design, Layout, and Simulation. 2005.

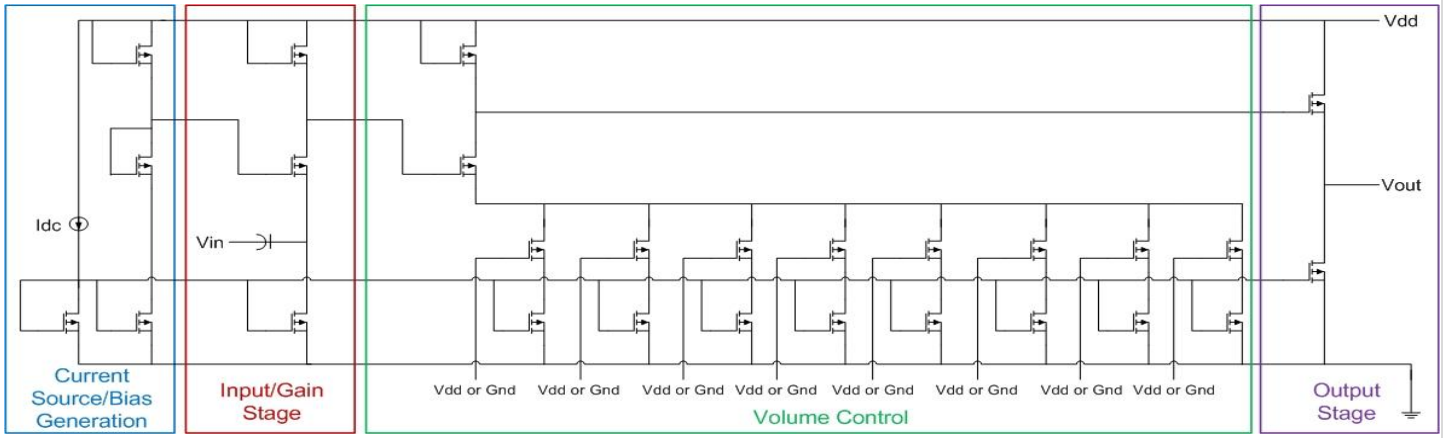

Figure 1: Schematic. A MUX chooses volume by supplying Vdd to one current mirror and 0 V to the rest in the volume control stage.

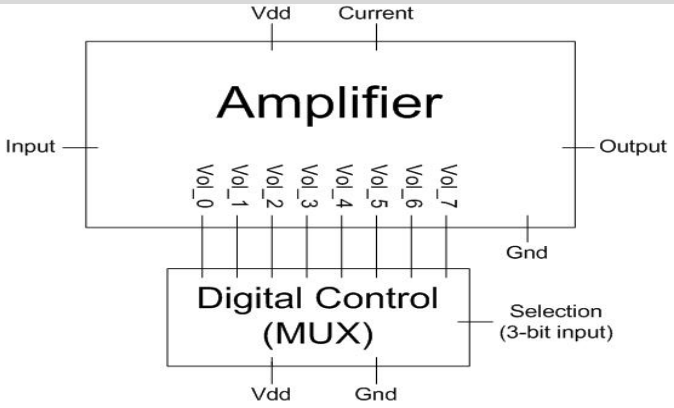

Figure 2: Digital Control. MUX (multiplexer) is used to supply either Vdd or Gnd to one input of the volume control stage of the amplifier for variable gain.

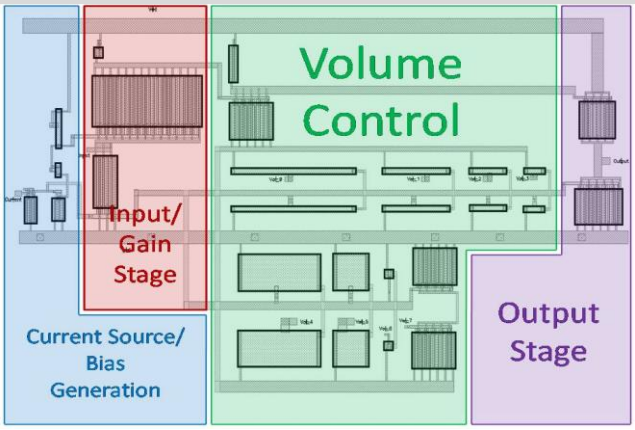

Figure 3: Layout.

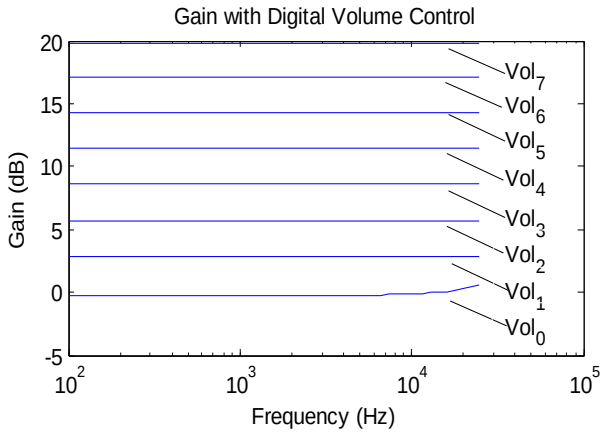

Figure 4: Gain with Digital Volume Control.

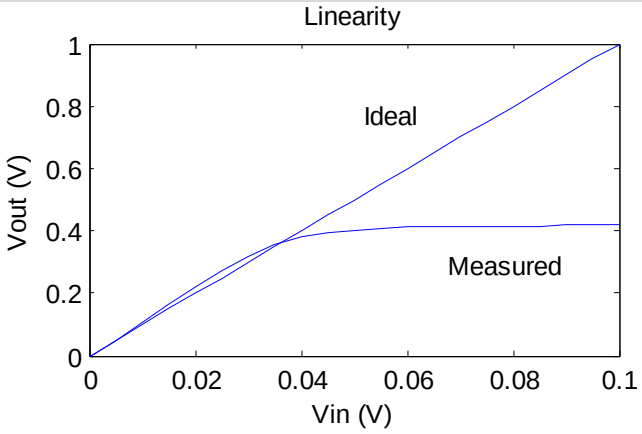

Figure 5: Linearity.

Parameter	Process Corners Variation				
	TT	FF_0°C	FF_75°C	SS_0°C	SS_75°C
Gain (at max volume)	19.78dB	21.73dB	19.02dB	19.5dB	2.568dB
Input Impedance	98.38 Ohms	80.46 Ohms	113.4 Ohms	89.85 Ohms	500.1 Ohms
Output Impedance	100.3 Ohms	86.85 Ohms	107.3 Ohms	96.69 Ohms	119.7 Ohms
Power Consumption	3.77mW	3.851mW	3.798mW	3.724mW	3.66mW

Figure 6: Process Corners Variation.

Parameter	Specification	Design
Power Supply	2.5 V	2.5 V
Current Supply	100 uA	100 uA
Max Gain	20 dB	19.78 dB
Min Gain	0 dB	-0.2711 to 0.513 dB
Input Impedance	100 Ohms	98.38 Ohms
Output Impedance	100 Ohms	100.3 Ohms
Frequency Range	100 Hz to 23 KHz	100 Hz to 23 KHz
Power Consumption	< 6 mW	3.77 mW
Max Input Signal	50 mV	40 mV (for linearity)
THD	< 1% (at max gain)	0.7537% (1mV input)

Figure 7: Summary of Results at Room Temperature.