A Digitally-Controlled Variable-Gain Amplifier for Ultra-Wideband Applications

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Introduction

Ultra-wideband (UWB) technology is a promising solution for low-complexity, low cost, low power and high-data rate wireless connectivity among devices in a personal area network. The main signal processing operations involved in a typical analog front end of a UWB receiver before demodulation are frequency translation to baseband, signal amplification and filtering to strengthen the received signal and eliminate interference. The required amplification depends on the strength of the incoming signal. This mandates a wideband variable gain amplifier (VGA) with wide controlled-gain range. The design of a VGA poses challenging constraints such as bandwidth, tuning range, dc offset, dynamic range, etc. Our design demonstrates bandwidth of approximately 900 MHz with a 31.5 dB linear-controlled gain range. Moreover our design uses a novel digital control scheme based on binary weights to control the gain of the VGA.

At the heart of the VGA is a Gilbert Cell whose gain is a function of the tail current. The tail current is controlled by the Digital Control Circuit which in turn is operated by a DSP section that is not a part of our design. The gain of the VGA is linear in magnitude controlled over a range from -6dB-25dB in 16 steps. We initially set out to achieve a 3dB bandwidth greater than 528 MHz but were able to achieve a bandwidth of approximately 528 MHz with our design. The common mode feedback circuit senses the output common voltage and compensates voltage offset from mismatches and maintains a fixed DC voltage level of output. The VGA cell implements a constant gm biasing technique since in this case the current is directly controlling the gain of the amplifier. A post Amplifier stage is designed to provide an extra 6dB gain and to extend bandwidth.

VGA

The core of our Variable Gain Amplifier (VGA) is a Gilbert cell (Figure 2A) consisting of 4 identical cross-connected NMOS's (M1-M4) as amplifying components and 2 identical diode-connected NMOS's (M5-M6) as load. Gates of M1 and M4 are inputs for V+ signal, and those of M2 and M3 are for V-. M1 and M2 are driven by the same current I1; similarly, M3 and M4 are driven by I2. The total current is then divided equally between M5 and M6. By rough calculation, the gain of this cell is

$$A_V = \sqrt{\frac{(W/L)_{1,2,3,4}}{(W/L)_{5,6}}}\sqrt{\frac{2}{I_1+I_2}}\left(\sqrt{I_1}-\sqrt{I_2}\right)$$

Thus, the maximum gain is 7.392 V/V=17.38dB, whereas the minimum gain is 0.122 V/V=-18.30 dB. In order to further increase gain, 2 constant-biased PMOS loads (M7-M8) are added to remove a large portion of currents flowing through M5 and M6. This works because the load is equal to $1/gm_{5,6}$, less current implies smaller gm, which in turn gives a larger gain. Small dimensions of M1-M6 are chosen carefully to ensure desirable bandwidth (at least 528 MHz in our case). Since tiny gains are not practical in applications, another 6-dB post-amplifier is implemented. The final gain range measured is from 0.497 V/V to 18.568 V/V (i.e. from -6.07 dB to 25.38 dB). The pole associated with PMOS loads is critical for bandwidth. By OCTC calculation,

$$\omega_P = \frac{1}{C_{gd,P}\times r_{O,P}} = \frac{\lambda I}{C_{gd,P}}$$

so the pole frequency is about 700 MHz. If one replaces M1-M4 with cascode amplifiers, headroom problem may occur; if replaced with folded cascode amplifiers, bandwidth must be sacrificed.

Common-Mode Feedback

The output DC level should be stable in order to drive the next stage properly. Therefore, CMFB is necessary. A simple averaging circuit, [4] as shown in Figure 2B, is utilized to sense the common-mode level. The PMOS's are in deep triode region functioning as large resistors averaging out ac signals; a capacitor also assists in filtering ac signals (but this capacitor is realized by an NMOSCAP in layout for reducing area). A differential amplifier compares this voltage level with Vref, a constant bias of desired level, and feeds back to every biasing circuit. The CM level is thus balanced.

Digital Control Circuit

All the VGA's in the references either assume an analog control voltage [2] or use a DAC to convert from a digital signal to an analog voltage [3]. The proposed VGA employs a novel scheme (Figure 3) for controlling its gain without converting from current to analog voltage. The input to the control circuit will be a combination of bits from the DSP stage that are set according to the required gain. A current source is generated from the biasing circuit. Since PMOS switches are used, the inputs are first inverted and then connected to the gates of M2, M4, M6 and M8. PFET's M1, M3, M5 and M7 copy current from M10 in the ratio of binary powers. PMOS's M9, M12 and M14 form a current subtraction circuit. We have used this topology to eliminate the need to have binary weighted current copies for both current paths. The base currents are constant at 5uA and 475uA and are setup in the tail of the two branches of the Gilbert cell. The step size chosen is 30uA to help us achieve a resolution of 1.2 in magnitude. The maximum gain is 25.4 dB when all bits are set to 0 while the minimum gain is -6.07 dB when all the bits are 1. Another important feature of this topology is that it has only one stack in the current path which is made possible by the introduction of M11 and then copying the required currents to the subtraction circuit and the output. For maximum gain the digital control circuit alone consumes about 0.268mW of power while for the minimum gain it consumes about 0.842 mW. Simulations have shown that the Control circuit is stable over process corners. The plot of gain vs. current Figure 6A shows a linear relation which is a desirable factor in the front end of analog receivers.

Post Amplifier

The post amplifier (Figure 4A) has input voltage with large magnitude; therefore, high linearity is important. For CS with source degeneration topology, the Gm is described as

$$Gm = \frac{g_m}{1+g_m R_s} \approx \frac{1}{R_s}$$

, which for large $g_{m*}R_S$ approaches 1/Rs, an input-independent value. However, the input DC level is limited by the previous stage; thus, I_{SS} going through R_S will consume a voltage headroom; therefore, topology with resistive degeneration between two tail current is desirable. Besides, for this topology, there is a parasitic capacitor formed by the current source, thus overall gm becomes

$$\text{Gm} = \frac{1}{1+gm\left(R_S \parallel \frac{1}{sC}\right)}$$

, forming a zero to extending bandwidth for whole system. However, it may cause a slow transient response.

Constant gm bias

Constant gm bias (Figure 4B) is designed to maintain the constant trans-conductance for whole system. To keep M3 and M4 flowing through the same current, long length transistors for current mirror are desirable. For this topology,

$$I_{out} = \frac{2}{\mu_p C_{ox}(W/L)_P}\frac{1}{\left(R_{S2}-R_{S1}\right)^2}\left(1-\frac{1}{\sqrt{K}}\right)^2$$

In addition, a start-up circuit composed of an inverter and M5 is used to prevent the zero current state.

Simulation Results

Through simulations, it is found out that the variable gain range of our VGA and Post-Amp is from 0.497 V/V to 18.568 V/V (i.e. from -6.07 dB to 25.38 dB), shown in Figure 7. The bandwidth varies accordingly to gain; the worst case occurs when largest gain is obtained, where the bandwidth is approximately 680 MHz. For smaller gains, bandwidth can be as large as 900 MHz. This result is good enough for UWB applications which require a bandwidth of 528 MHz.

Corner simulations show that the circuit is quite stable to temperature and process variation except when setting to minimum gain under FF_0C condition. We had made much effort in eliminating variation factors by choosing appropriate transistor type, device dimensions, and configurations. Common-mode feedback circuit works properly in balancing the current of the entire circuit. Power consumption of the whole circuit, including the digital control circuit, VGA cell, Post-Amp and all biasing circuits, is about 9 mW with Vdd=3.3 V. The power of the digital part ranges from 0.2 to 0.9 mW depending on the current it is supporting. This is a direct result of the scaling down of both imaging currents and device sizes. The transient response is reasonable even with the fact that nearly 60 transistors and 12 resistors are implemented. Results are summarized in Table 1.

Conclusion

A VGA cell is proposed for UWB system applications. It consists of a Gilbert Cell, digital control circuit, and a post amplifier. The gain range of the whole amplifier is -6dB~25dB. The resolution is 1.2V/V in magnitude. The bandwidth is over 600 MHz, which is sufficient for UWB application. Implemented in 0.25um CMOS technology, the chip consumes 11.36mW from a 3.3V supply.

References

[1] Chia-Hsin Wu, Chang-Shun Liu, and Shen-Iuan Liu, "A 2GHz CMOS Variable Gain Amplifier with 50 dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet", ISSCC 2004/ Session 26/Optical and Fast I/O / 26.8.

[2] Quoc-Hoang Duong, T. -J. Park, E. –J. Kim, and Sang-Gug Lee, "An All CMOS 743MHz Variable Gain Amplifier for UWB Systems", IEEE International Symposium on Circuits and Systems 2006 proceedings, pp. 678-681, May, 2006.

[3] Sivasankari Krishnanji, "Design of a Variable Gain Amplifier for an Ultra Wideband Receiver", Master's Thesis, Texas A&M University.

[4] Po-Chiun Huang, Li-Yu Chiou, Chorng-Kuang Wang, "A 3.3V CMOS Wideband Exponential Control variable-gain-amplifier", Proceedings of the IEEE International Symposium on Circuits and Systems, 1998.

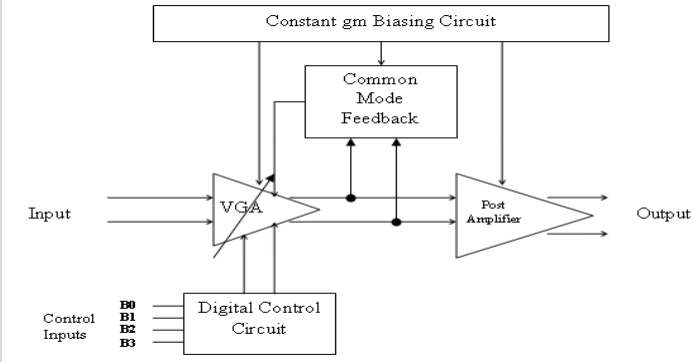

Figure 1: Block diagram of proposed VGA cell

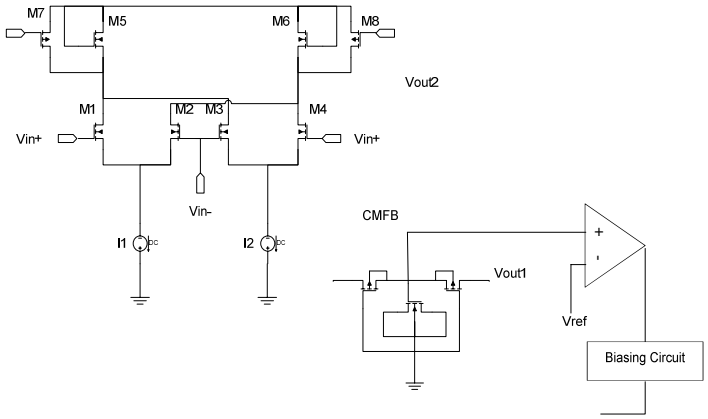

Figure 2A: Schematic of VGA

Figure 2B: Schematic of CMFB

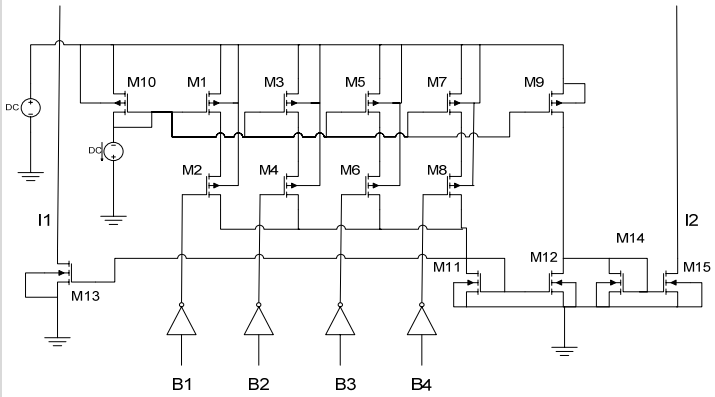

Figure 3: Schematic of Digital Control Circuit

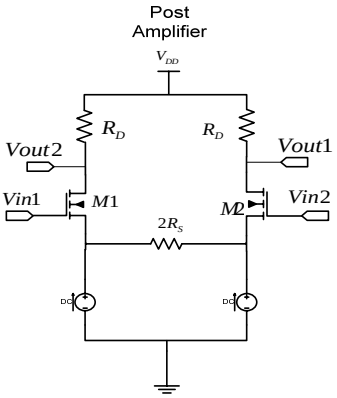

Figure 4A: Schematic of Post-Amp

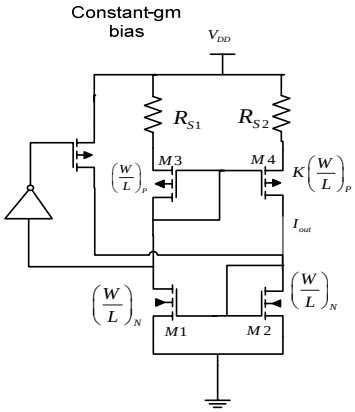

Figure 4B: Schematic of constant gm bias

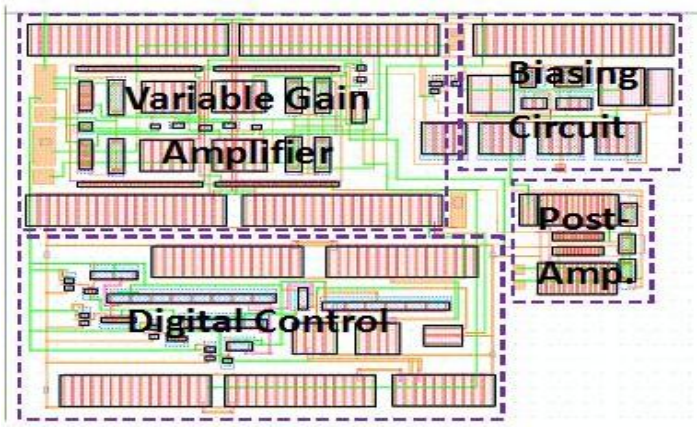

Figure 5: Layout in Cadence(DRC and LVS clean)

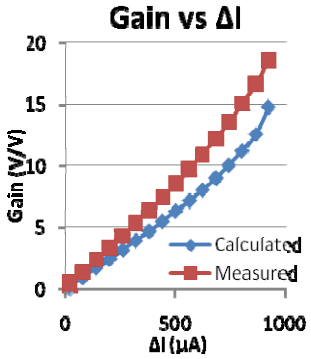

Figure 6A: Voltage gain vs. Control current

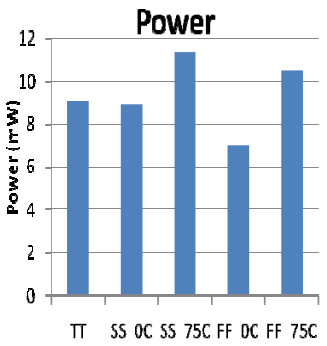

Figure 6B: Power consumption with different corners

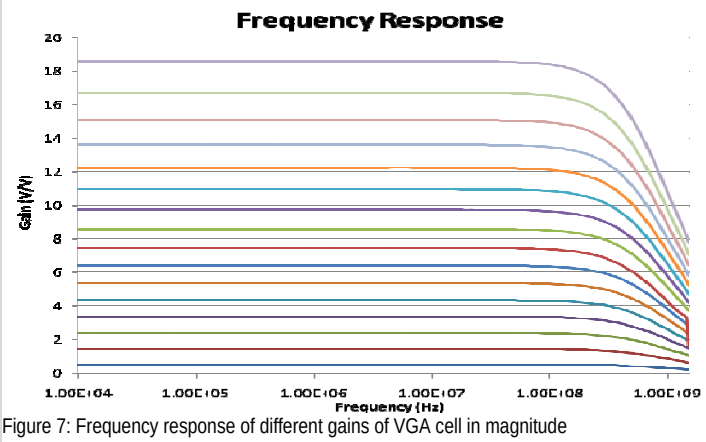

Figure 7: Frequency response of different gains of VGA cell in magnitude

		TT	SS_0C	SS_75C	FF_0C	FF_75C			TT	SS_0C	SS_75C	FF_0C	FF_75C
Extraction	Max Gain (dB)	25.38	25.76	25.42	24.49	24.97	schematic	Max Gain (dB)	25.38	25.76	25.41	25.08	24.97
	Max Gain (V/V)	18.568	19.412	18.654	16.778	17.714		Max Gain (V/V)	18.568	19.412	18.652	17.946	17.716
	Min Gain (dB)	-6.073	-4.734	-3.707	-10.92	-6.14		Min Gain (dB)	-6.069	-4.734	-3.707	-9.005	-6.136
	Min Gain (V/V)	0.497	0.5798	0.6526	0.2844	0.4932		Min Gain (V/V)	0.4972	0.5798	0.6526	0.3546	0.4934
	Bandwidth (MHz)	689	635	517	939	775		Bandwidth (MHz)	899	821	637	1333	1030
	Power (mW)	9.101	8.95	11.36	7.048	10.58		Power (mW)	9.266	9.02	11.36	8.6	10.76

Table 1: Simulation results of Extraction and Schematic Circuit