A low power and low frequency sample and hold circuit for pacemaker application

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Obtaining low power and low supply voltages are the major challenges in bio-electronics. Moreover, low frequency operation makes the design even harder, due to the large leakage current over a long period of time. This paper demonstrates the design of low power and low frequency sample and hold circuit, which consumes power of 92.9nW with a supply voltage of 0.7V and has a compensated leakage current as low as 4fA. Devices are working in weak inversion. Additional technique of leakage cancellation [1] has been employed to further improve the performance of sample and hold and to decrease the layout area of the devices by significantly reducing the size of hold capacitor.

The major blocks of the circuit are two Subthreshold Op-amps, one switching circuitry and one leakage cancellation circuitry.(Figure 2)

The two Op-amps in this design employ the same topology, a differential pair with active current mirror load cascaded with a common source amplifier. This topology is selected because (1)the cascade topology can provide a very high gain, which in this application, is crucial since it ensures that the closed loop gain of the buffer is very close to one, and the S/H accuracy will not be seriously affected; (2) this topology is easy to compensate, thus, a decent phase margin can be obtained to avoid a large overshoot at the output of the buffer, hence, reducing the settling time. As power is the major concern for an implantable device, the circuits are designed to operate in subthrshold region, and I/O transistors are used. Also, the transistors are sized with a longer length to reduce leakage current. The open loop gain of the opamp is:

$Av = g_{m1,2}(r_{o1,2} \,||\, r_{o3,4})\, g_{m6}(r_{o6} \,||\, r_{o7})$,

where $g_m = \frac{I_D}{nKT/q}$ for the Sub-Threshold operation and

$Id = (\frac{W}{L})_{eff}\mu(\frac{KT}{q})^2\sqrt{qN_{ch}\varepsilon_{si}/4\phi_F}\, e^{\frac{(V_{GS}-V_{TH}-V_{OFF})}{nKT/q}}$,

where ϕ_F is the Fermi Potential, N_{ch} is the channel doping and V_{OFF} is a constant introduced to correct for the drain current when V_{GS} = 0[2]. The equation indicates that current varies exponentially with V_{GS} and also current has quadratic dependence on temperature. Our Op-amp is robust and gives good performance over all the corners from 0^oC to 75^oC as depicted in Figure 3.

This Op-amp topology has different slew rates for rise and fall transitions, and they are limited by the bias current, which is small because of subthreshold conduction. The maximum amount of current the Op-amp can source is limited by M7, while the maximum amount of current the Op-amp can sink is much more than I_{D7} by pulling the gate of M6 high. However, slew rate is not a critical issue in this application, because the input signal does not vary very fast.

Switching network controls the charging and discharging of the hold capacitor. The switches are implemented using transmission gate, which gives lower impedance and hence a smaller time constant for charging and discharging the hold capacitor. It is desired to reduce RC in S/H circuit because it can reduce the acquisition time of signal. However, the choices of R and C are limited by the fact that the voltage on the hold capacitor will drift due to leakage current. If the sizes of transistors are increased to reduce R, they will source more leakage current, causing signal to drop more during hold mode. On the other hand, if C_{hold} is small, in the range of several pF, for the same leakage current, the droop of the signal during hold mode will also become intolerable.

Since in pacemaker application, area is also of concern, we cannot reduce the signal drift by using a large hold capacitor. To compensate the leakage current problem, a leakage current cancellation technique [3] is employed (Figure 4). Replica switch and hold capacitor C_{rep} are used to provide reference voltage for comparison. The voltage on C_{rep} and C_{hold} are fed into an opamp, which drives the leakage circuit to supply cancellation current. C_{rep} is a much smaller capacitor than C_{hold}, therefore, the voltage drift on C_{rep} is much larger than C_{hold} The opamp compares the voltage on C_{hold} and C_{rep}, if V_{rep} is lower than V_{hold} because capacitors are discharged by the same leakage current from the switches and C_{rep} is a smaller capacitor, the output of the Op-amp will drop, and make the leakage cancellation circuit source current to the capacitor. Again, since C_{rep} is smaller, V_{rep} is charged up quickly and after exceeding V_{hold}, opamp will drive the leakage circuit to sink current from the capacitors. Ideally, this continues until the cancellation current fed back is the same as the leakage current (Figure 7). The voltages on C_{rep} and C_{hold} do not become exactly the same in figure 7 because of offset voltage of opamp.

The NMOSs in the leakage cancellation circuit are sized twice as large as PMOSs such that the cancellation current varies almost linearly with the control voltage from the Op-amp (Figure 4). By using the leakage cancellation technique, we are able to significantly reduce the hold capacitor size (from nF to pF) and resultantly reduce the area of the layout.

The Op-amp draws 9nA from a current source and consumes 41nW. The open loop gain is 68.9dB and the phase margin for the unity gain buffer is 45 degrees. Corner simulation results are shown in figure 3, which indicates slight variation of performance.

The S/H circuit is simulated with a 1Hz 20mV PPK input signal at a sampling frequency of 10Hz at 37°C. Figure 5 shows the TT simulation over one cycle of the input signal. The zoom-in plot of the hold period shows the output has a settling time of approximately 4ms, and the error is around 10uV. After using the leakage cancellation technique, the leakage current is reduced to 4fA in our circuit, comparing to 10fA in the previous work[1]. Figure 6 shows the simulation of S/H circuit over SS, FF corners with temperature of 32^oC and 42^oC . The accuracy of the signal during the hold mode deteriorates significantly under corners, up to ~150uV. This is likely due to the quadratic temperature dependence of the current of the subthreshold devices in the leakage cancellation circuit.

In summary, the S/H circuit discussed in this paper makes an improvement over the key performance parameters like power consumption and the accuracy over the hold period. Figure 8 shows the performance of the SH circuit compared to the previous work designed in [1]. The layout is showed in Figure 1, it uses 4 metal layers and occupies 300umX100um area.

References:

1. Louis Wong, S. Hossain, " A very Low power CMOS Mixed-Signal IC for implantable pacemaker Applications" ISSCC 2004 / SESSION 17 / MEMS AND SENSORS / 17.5
2. G. Guistolisi et. al.," A Low voltage low power voltage reference based on Subthreshold MOSFETs" IEEE Journal of Solid State Circuits Vol 38 No.1, January 2003
3. Louis Wong, S. Hossain, "Leakage Current Cancellation Technique for Low Power Switched- Capacitors Circuits" patent pending

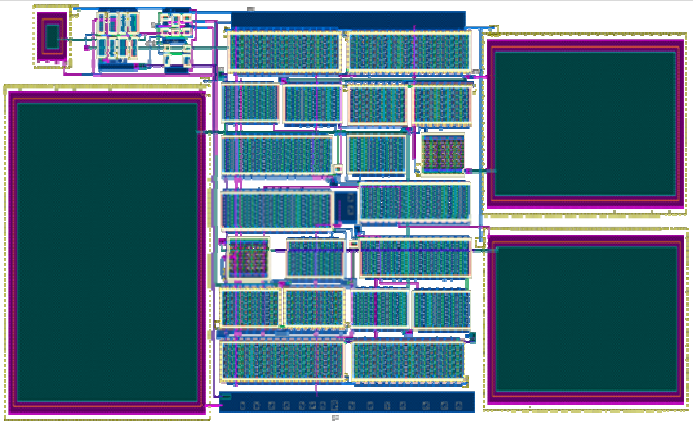

Figure 1:Layout (LVS and DRC clean)

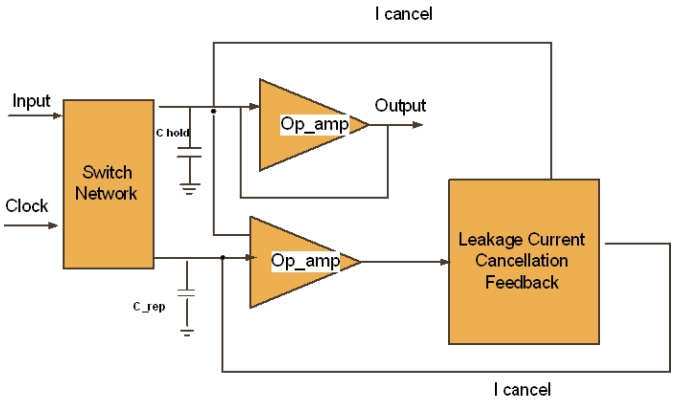

Figure 2. Block diagram of the S/H circuit

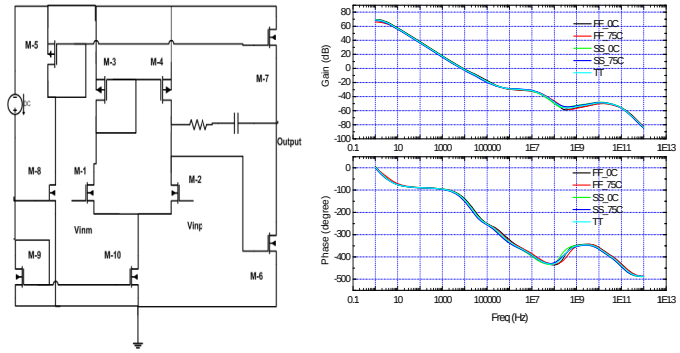

Figure3. Op-amp topology (left) and gain and phase of the open loop response(right)

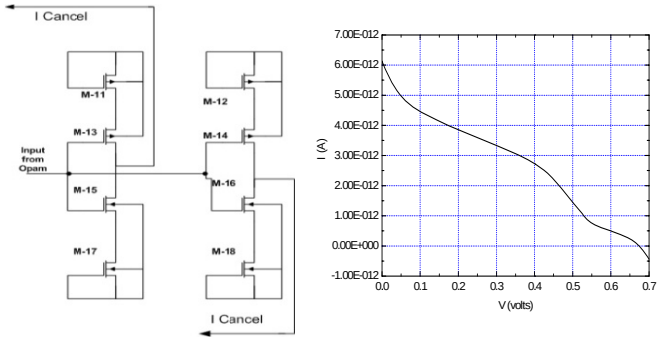

Figure 4. Leakage Current Cancellation Circuit (left) and its I-V characteristic (right)

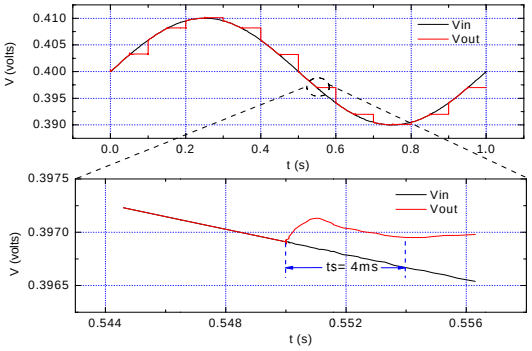

Figure 5. Output of S/H circuit at 37C (upper) and zoom-in plot of hold period showing the settling time (bottom)

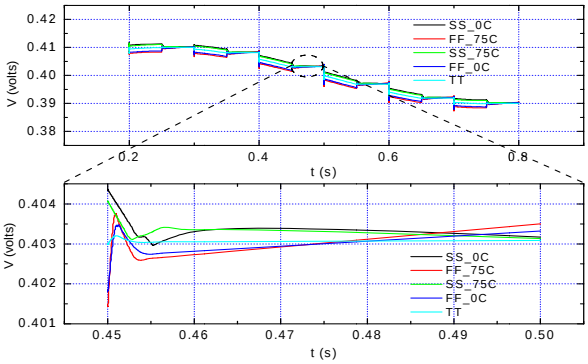

Figure 6. Corner simulation of the S/H circuit over 32^oC to 42^oC

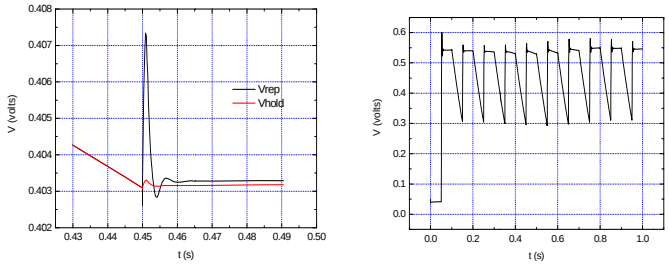

Figure 7. The variation of voltages on Crep and Chold during hold mode (left) and the drive signal of the leakage cancellation circuit (right)

Specification	Our work	Other work[1]
Process	0.25um	0.5um
Power	92.9nW	~150nW
leakge current after cancellation	4 fA	10 fA
Settling time	4ms	??
Hold capacitor	10pF	1pF

Figure 8: Table summarizing the performance