Low Noise CMOS Simulation of Outer Hair Cell Activity in the Mammalian Cochlea

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Introduction

The mammalian cochlea is an impressive transducer. The cochlea has inspired the construction of many devices [1,2] that both mimic the performance of the cochlea and shed light on the functionality and complexity of the organ. This work describes CMOS circuitry capable of mimicking outer hair cell (OHC) activity in the cochlea. This circuitry is designed to be flip-chip bonded to a MEMS device under development at the University of Michigan [1] to create the first physical model of the cochlea incorporating multiple channels of active feedback.

A block diagram of the circuit can be seen in Figure 1. The input stage of the circuit amplifies the voltage developed across the electrodes of a piezoelectric beam. To avoid adding noise to the signal, the input stage of the device has been designed to have noise below the self noise of a piezoelectric beam. This piezoelectric noise is inversely proportional to the square root of frequency and, for these particular beams, has a mean voltage spectral density of less than 38nV/√Hz at 1kHz. The gain of this first stage must be great enough to keep this noise level below that of all following stages. A complete description of stage specifications can be seen in Table 1. The second stage of the circuit simulates OHC activity and must be externally adjustable to allow for the testing of various theories of OHC operation. The third stage of the circuit outputs the filtered signal to a piezoelectric beam which imparts a force on the vibrating membrane of the device. This stage must be capable of attenuating the signal to simulate various levels of OHC activity.

First Stage

The first stage must have a large gain with low equivalent input noise from 20Hz to 20kHz. The topology of this circuit is composed of a PMOS differential input stage with active current mirrors as shown in Figure 2. This equivalent input noise (E_{eq}^2) is composed of white noise (E_{white}) and 1/f ($E_{1/f}$) noise components and is expressed as:

$$E_{eq}^{\ 2} = \left(E_{white}^{\ 2} + E_{1/f}^{\ 2}\right)\Delta f = \left(\frac{8kT(1+g_{mbs}/g_m)}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right)\Delta f \quad (1)$$

where, k is the Boltzmann's constant, T is temperature, KF is the flicker coefficient of the 1/f noise component, K' is the transconductance parameter, WL are the width and length of the transistor, and g_m is the transconductance. White noise is inversely proportional to transconductance (if g_{mbs}/g_m is << 1) and 1/f noise is inversely proportional to the gate area (WL). The white noise can be set by achieving the desired transconductance level, while the 1/f noise can be reduced by increasing the gate size. Since the noise of the entire circuit is mostly influenced by the noise of the input stage, the transistors used in the input were scaled by the largest amount. This stage was designed to meet the low noise and high gain requirements.

Second Stage

The second stage of the circuit is designed to have the transfer function shown in Figure3 with time constant, τ, and quality factor, Q. This circuit is based on one presented by Lyon and Mead [1]. The basic building block of this circuit is a differential input, single ended output, transconductance amplifier with a voltage controlled bias current, as shown in Figure 4. The second stage was added to increase the minimum common mode input voltage in order to make this stage more compatible with the bias voltage of the output of stage 1. A block diagram of the complete second stage is depicted in the upper right corner of Figure 4. This block diagram consists of two follower integrators with an additional amplifier in feedback to add current onto the first follower integrator capacitor. The transfer function matches that shown in Figure 3 with $\tau=C/G$, and $Q=0.5(G_1+G_2)/(G_1+G_2-G_3)$.

The bias voltages have not been incorporated into this design because they are applied externally as indicated in Figure 1. Bias voltages ranging from 200mV to 500mV give time constants that encompass the bandwidth of interest and keep all devices operating in subthreshold. Subthreshold operation reduces the transconductance of the amplifiers, and provides an exponential relationship between transconductance and bias voltage. Lower transconductance allows the use of smaller capacitors and an exponential relationship between transconductance and bias voltage means that linearly spaced taps to a resistive line give exponentially varying time constants, matching the exponential taper of the MEMS device.

Third Stage

The third stage is used as a buffer between the second order system and the high impedance of the transducer. Since there is enough gain from the first stage, no gain is necessary in the final stage and a source follower circuit topology was used. Since the drive has high impedance, the gain will be set by the impedance and transconductance of the PMOS. The gate of the source follower was AC coupled and then biased with two diode connected NFETs. The coupling capacitor was chosen small enough to give a zero frequency less than 10Hz.

Layout and Simulation

The circuit was laid out and simulated in cadence using a 0.24μm CMOS process. The layout can be seen in Figure 5. This layout is arranged in a long, slender shape to allow several of these devices to be stacked for the complete chip design. The layout is dominated by the large transistors of the first stage.

The circuit performance can be seen in Table 1. The input referred noise of the circuit is 37.5nV/√Hz, slightly below the specified noise input. All other specifications are exceeded and are summarized in Table 1. The gain of the circuit is dominated by that of the first stage, amplifying the piezoelectric self noise above 10μV/√Hz in all subsequent stages. Operating the second stage in subthreshold allows the transconductance to be calculated as G=1.056e-10*exp(25.9V_b). This transconductance in combination with 2.5 pf capacitors gives circuit characteristics shown in Figure 6. At the corners, the transconductance of the circuit varies substantially as noted by Lyon and Mead [1]. The work of Watts et al [3] was intended to reduce this variation but did not provide significant improvement. All other variation at corners is within an acceptable range. Figure 8 compares the influence of this circuit with experimental results measured in a cochlea for qualitative comparison.

Conclusions

The circuit nominally meets all requirements but varies significantly with process. Significant work is required to reduce sensitivity to process variation appreciably as indicated by Watts et al. [3]. Nominally, the circuit behaves predictably and can be used to simulate OHC feedback characteristics.

References

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[3] L. Watts, D. A. Kerns, R. F. Lyon, C. Mead, "Improved Implementation of the Silicon Cochlea," IEEE J. Solid State Circuits, vol. 27, pp. 692–700, 1992.
[4] N. C. Cooper, "Harmonic distortion on the basilar membrane in the basal turn of the guinea-pig cochlea," J. Physiol. (London) **509**, 277-288, 1998.
[5] W.T. Holman, "A Low Noise CMOS Opamp in a 1.2uM Digital Technology," Georgia Institute of Technology

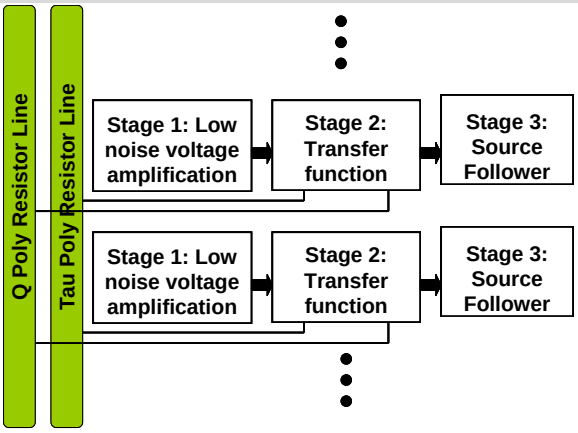

Figure 1: Circuit Block Diagram

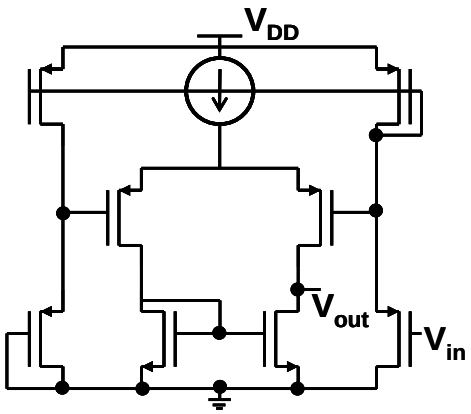

Figure 2: Schematic of stage 1.

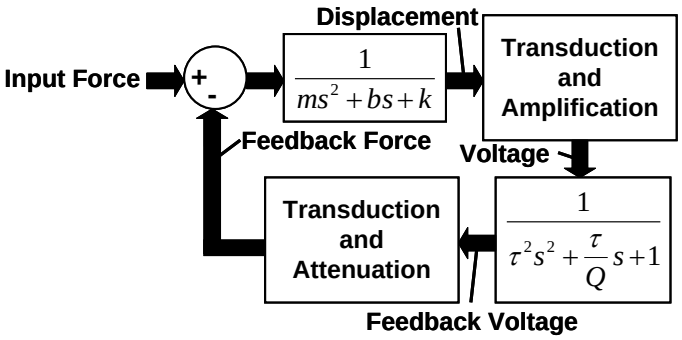

Figure 3: Block diagram of the circuit acting on a mechanical system.

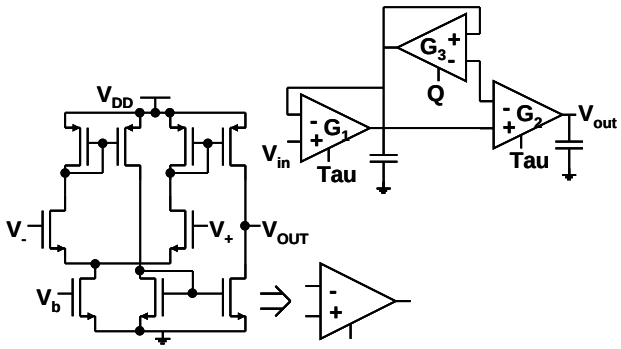

Figure 4: Schematic of transconductance amp and diagram of stage 2.

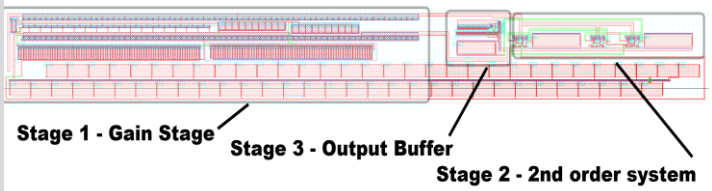

Figure 5: Layout

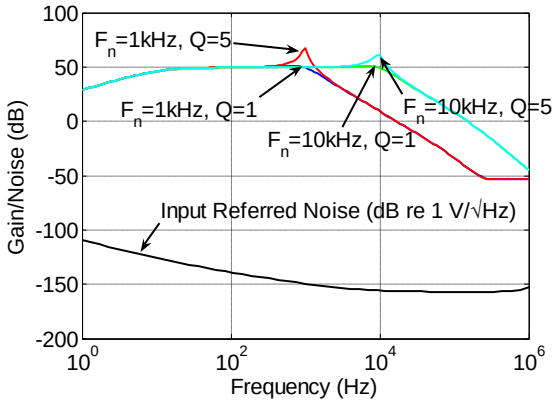

Figure 6: Modeled gain and noise of circuit

	Specification	Modeled
Bandwidth	20 Hz – 20 kHz	11 Hz – 185 kHz
Max Adjustable Gain	40 dB	49.5 dB
Input Referred Noise (1kHz)	38 nV/√Hz	37.5 nV//√Hz
Max Input Signal	276 µV	> 1 mV
Power	N/A	2.1 mW

Table 1: Table summarizing specifications and results.

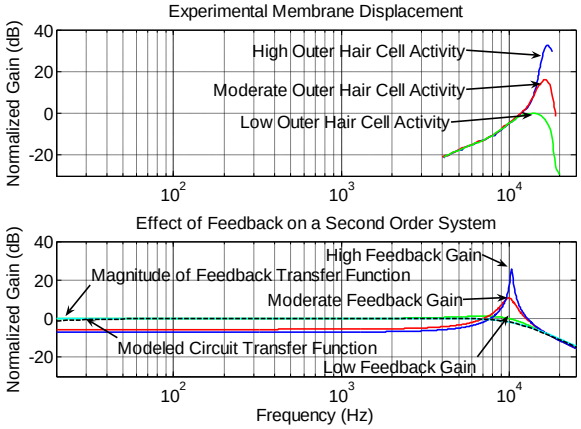

Figure 8: Comparison of feedback with experimental results of Cooper [4].