A Digitally Controlled CMOS Variable Gain Amplifier for Ultrasound Imaging

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Motivation and Scope

The dynamic range of the input signal for ultrasound receivers over the full receive interval is approximately 110 dB and is well beyond the range of analog to digital converters (ADC) used in the receivers. Variable Gain Amplifiers (VGAs) are used extensively in phased-array ultrasound receivers to bring the received signal within the dynamic range of the ADC. VGAs for standard 2D gray-scale imaging require a dynamic range of 40 dB to map a signal into a 12 bit ADC with a 70 dB dynamic range [1]. Standard imaging frequencies ranges from 2 MHz to a maximum of 15 MHz [1]. Power consumption for typical VGAs is about 150 mW. In this paper we describe the design of a low power (< 150 mW) CMOS VGA with a dynamic range greater than 40 dB (-13 to 40 dB) over the frequency range from 2 to 15 MHz.

Circuit Topology

The block diagram for our VGA is shown in Fig 1. The circuit consists of three main blocks. The input stage converts a differential voltage to a differential current. Each branch of the differential current is amplified (coarse control) by the gain control stage which is digitally controlled. Finally, the output stage converts the differential current back to a differential voltage output. The output stage is also designed to have fine control (1 dB) of gain up to 5 dB that is digitally switched. The schematic of the entire circuit is shown in Fig 1.

The Input Stage

The input stage converts a differential voltage input to a differential current output. The feedback amplifier A1 ensures that $V_+ = V_A$ and $V_- = V_B$. This is done by making sure that the gain (A(s)) of the feedback amplifier is sufficiently high. The feedback amplifier is designed as a simple differential amplifier with an active load [2]. A(s) was calculated to be approximately $g_m ro/2$ and β is 1. The expressions for the output currents from the input stage are:

$$I^+ = I_{M1} - I_{M5} = I_{M2} - I_{M6} = I_R$$
$$I^- = I_{M4} - I_{M8} = I_{M3} - I_{M7} = -I_R.$$

The differential current is then given by

$$I_{Id} = I^+ - I^- = 2I_R = (V_A - V_B)/R = V_{Id}/R$$

where $R = R_1 + M_9$. Adding M9 and M10 helps to keep the gain independent of process and temperature variations [2].

The Variable Gain stage

The variable gain stage consists of *n* gain cells, each with *m+1* gain stages. The differential current is amplified using current mirrors and the stages are controlled by digital inputs. Due to their high input resistance, cascoded transistors are used as they help reduce the error in gain [2]. When $d_m=1$, the voltage at the gate of the NMOS (PMOS) cascode transistor is V_{BN} (V_{BP}) the stage is turned on and the current adds to the output current. When $d_m=0$, this voltage is 0 (V_{dd}) and the stage is turned off. The gain stage was designed to give the following current output

$$I_{out} = I_{In}(1 + d_0 + 2d_1 + 4d_2 + ... + 2^m d_m) = 2^{(m+1)} = 6(m+1)\text{dB}$$

current gain [2]. The transistors were sized appropriately to give the required factor of 2. In theory this could extend to as many stages as needed for the required gain - but this would mean larger transistors, a higher capacitance, and a lower bandwidth. The power consumption would also be higher in this case. Therefore, instead of adding more stages to one gain cell, we added more gain cells each with just 2 stages, i.e. m=1. The gain stage is inverting or noninverting depending on whether *n* is odd or even. In this case the differential current gain is given by

$$I_{OD} = I_2^+ - I_2^- = (-1)^n A_1 A_2 \ldots A_n I_{ID} = (-1)^n A_1 A_2 \ldots A_n V_{ID}/R$$

where $A_i = (1 + d_{i0} + 2d_{i1} + 4d_{i2} + ... + 2^m d_{im})$; i=1…n; m=1. The maximum gain is now given by $2^{n(m+1)} = 6n(m+1)$ dB. In our design we have chosen values of *n* and *m* as 4 and 1 respectively giving a gain of 48 dB (6dB/gain cell).

The Output Stage

The output stage converts a differential current input to a differential voltage output and provides finer control of gain (0-5 dB in 1 dB steps). The differential output is given by

$$V_{OD} = V_o^+ - V_o^- = (I_2^+ - I_2^-)R_2 = (-1)^n A_1 A_2 \ldots A_n V_{ID} R_2/R.$$

The overall gain is given by $(-1)^n A_1 A_2 \ldots A_n R_2/R$. Implementing R2 as a digitally controlled variable resistor provides a finer control of gain. The values of R2 were chosen to achieve a gain range of 0-5dB in steps of 1 dB [2].

The Current Source

The accuracy of the DC current source determines the accuracy of the bias points throughout the VGA. Therefore, the current source should be both temperature and process independent. A bandgap reference voltage source generates a constant bias voltage over temperature. This voltage biases the gate of transistor M13, which then provides a constant current over resistor R_I. This current is scaled to the specified value (50µA) using a current mirror. The temperature variation of R_I is compensated by adjusting the size of M12 relative to M11, producing a temperature coefficient of 0 for the output current. By choosing M13 to be a PFET rather than an NFET, the effects of process variations on the bandgap reference voltage are compensated upon the conversion to a reference current.

Simulation results

The circuit was designed and simulated in Cadence. The layout for our circuit is shown in Fig 3. The layout was DRC and LVS clean. The gain is accurate to 0.26 dB across the entire dynamic range (1.2 dB with including process variations). Figures 5 and 6 show the gain variation over process corners at the maximum (40 dB) and minimum gain values (-13 dB) over the frequency range of interest from 2 to 15 MHz. The slight increase in gain (over our spec of ±0.5dB) with frequency is due to extracted parasitic capacitances from the circuit layout. These capacitances added a pole to our system – resulting in a multiple order pole just beyond our operating frequency range. This pole caused a small peaking, especially for the SS 75 process corner.

Figure 4 shows the gain error between the target gain and simulated gain for -13 – 40 dB at 10 MHz. The systematic variation in the gain error is due to the fine gain control at the output stage. Each 1 dB gain point was set by a specifically sized resistor. Sizing limitations and the resulting resistive inaccuracies caused the fine-gain variations. Each peak corresponds to the maximum error due to the 0 dB gain setting, and each low point corresponds to the 5 dB setting.

Comparison

We compared the results of our simulations to the Maxim MAX2037 – another ultrasound targeted VGA. This chip features a 42 dB dynamic gain range with 0.25dB of absolute error, 125 mW power consumption per channel and a full-differential output. Our chip has a superior dynamic range, but a worse gain error when taking process variations into account. While our power consumption was much lower, this parameter cannot be accurately compared as the Maxim chip features a LNA as well as a VGA.

References

[1] "Optimizing Ultrasound-Receiver VGA Output-Referred Noise and Gain: Improves Doppler Dynamic Range and Sensitivity." Maxim Application Note 4038, [Online] at http://www.maxim-ic.com/appnotes.cfm/an_pk/4038. 13 November 2007.

[2] A.A. El-Adawy, A.M. Soliman and H.O. Elwan, "Low voltage fully differential CMOS voltage mode digitally controlled variable gain amplifer," Microelectronics Journal 31, pp. 139-146, 2000.

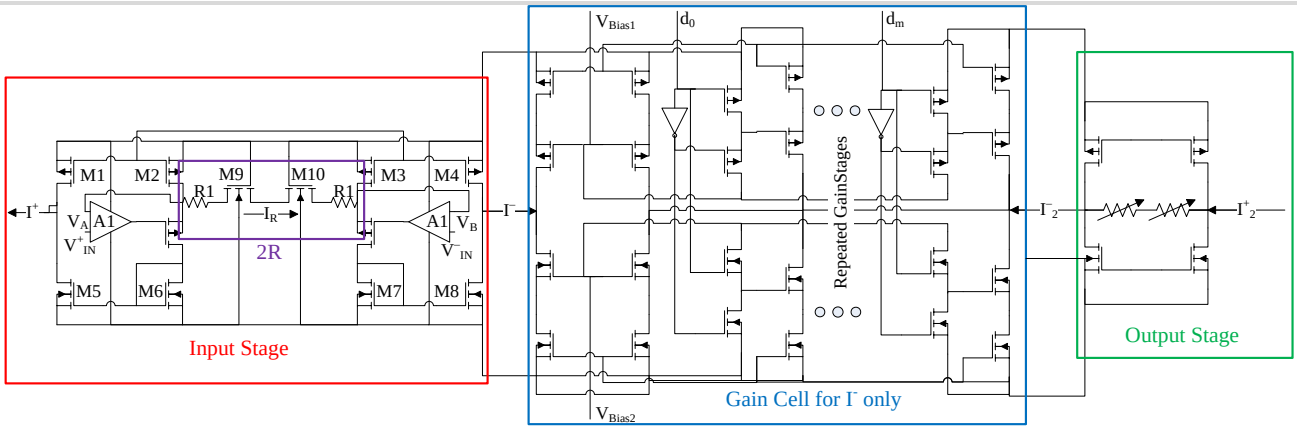

Figure 1: Schematic of the variable gain amplifier

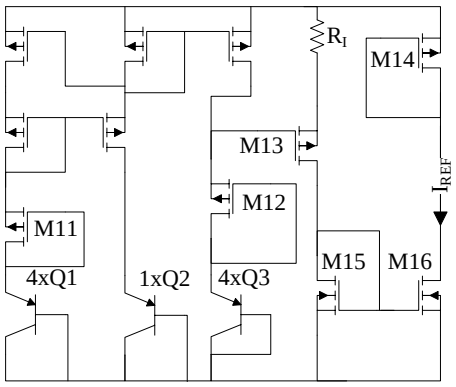

Figure 2: Schematic of the band gap reference current source

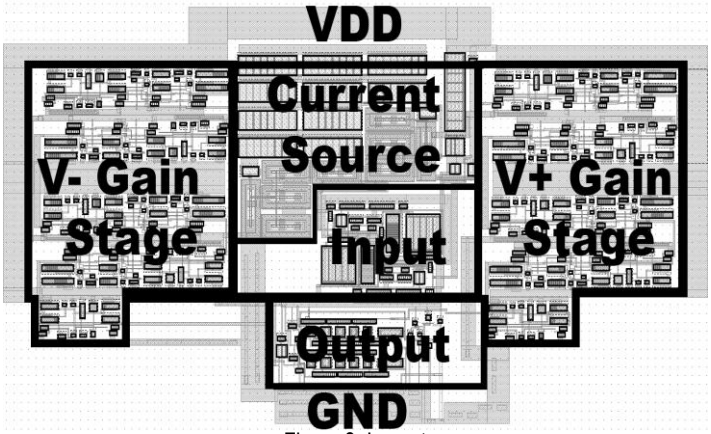

Figure 3: Layout

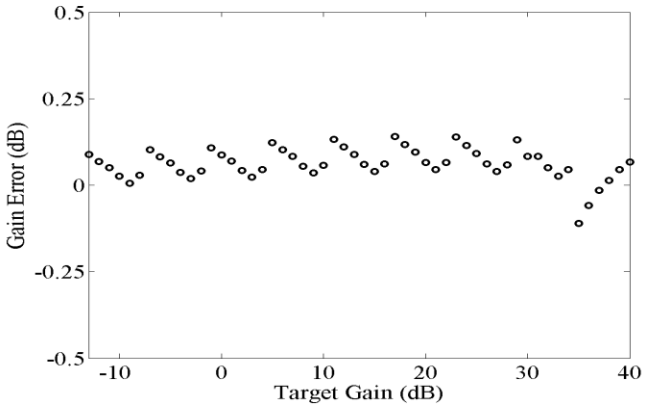

Figure 4: Gain variation Vs target gain at 10 MHz

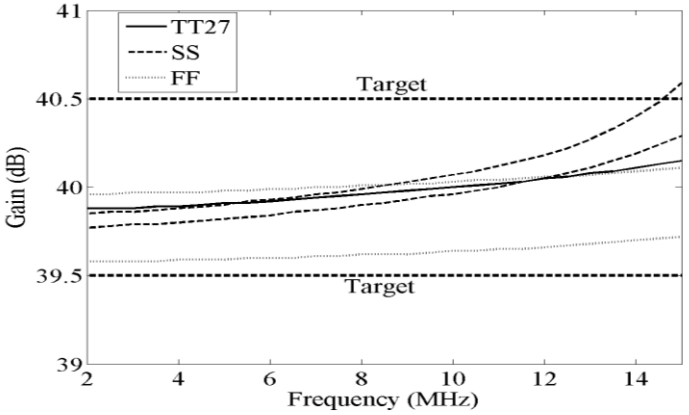

Figure 5: Variation of maximum gain (40 dB) over process corners

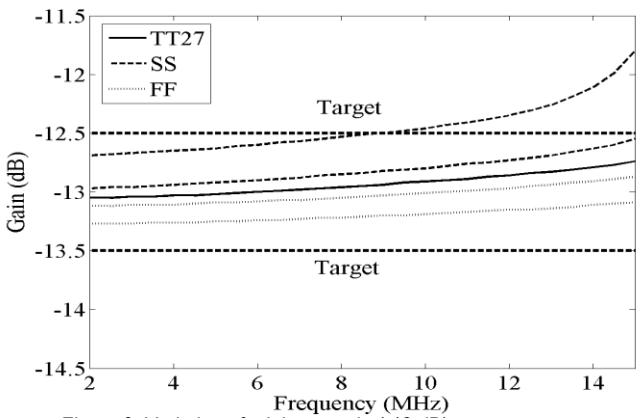

Figure 6: Variation of minimum gain (-13 dB) over process corners

Parameter	Specification	Design	Units
Power	<150	47.53	mW
Operating Range	2-15	2-15	MHz
Dynamic Range	40	53 (-13 to 40)	dB
Gain Accuracy (over process corners)	±0.5(±0.5)	±0.26 (±1.2)	dB
Reference Current	50±3%	50±2.386%	µA