Low Power Interchip Wireless Communication Using Inductive Coupling and Monocycle Signaling

Sang Wook Han, Geonwook Yoo, Dae Young Lee

Introduction

With the continuous downscaling of CMOS technology, various components are integrated in a single chip. However, it takes considerable time to develop such system (e.g. system LSI or system-on-a chip) with low yield. As an alternative, attention has been drawn to the System-in-Package. Even though several wired 3D interfaces, such as a micro bumping and a 3D via have been investigated, wireless interconnection among chips has been introduced newly for low cost and high speed [1][2]. In this work, inductive coupling transceiver with smaller area and higher power efficiency is presented.

Circuit Components and Simulations

The purpose of wireless communication is to minimize the power consumption on transmitting signal with minimized the area of each channel. Especially, for low power implementation, the ratio of transmitted to received power should be maximized. As shown in Figure 3, transfer function of coupled inductor shows that the efficiency in low frequency range is very low. To maximize transmission efficiency, following efforts are required: i) shift the signal to high frequency range, ii) place the peak value of transfer function in low frequency range. To achieve i) we present monocycle signaling instead of monopulse signaling and ii) is reached by optimizing coupled inductor parameters.

The inductive coupling is designed for data communication in 0.25μm six-metal CMOS. Square spiral shape inductor is implemented with metal 3, 4 and 5, and the inductor is placed over transceiver circuit as shown in Figure 1. Inductance is proportional to the number of turns and inductor size but the limited area of channel places an upper bound on it. Likewise, increasing the number of turns with reducing wire width makes the parasitic resistance larger. Hence the transmitted current level is lowered. Taken into account of this trade-off, the inductor was designed. Figure 2 shows the layout and equivalent circuit elements of inductive coupling, and figure 3 shows the S-parameter from HFSS and frequency response of the equivalent circuit. Limited number of metal layers restricts the inductance and as a sequence, the peak of transfer function is formed around 20GHz. This issue can be resolved by using the recent process, which provides more metal layers and enables inductor to be increased.

There is a large gap between the frequency of our generated monocycle signal, 3GHz and the peak of transfer function, 20GHz. However, it is impossible to increase the signal frequency with given 0.25μm CMOS process. We can increase the transmitting efficiency with a lager inductor, but within 20μm x 20μm area of the TX and RX circuits the size of inductor is the limiting factor of channel size. Finally we determined the inductor specifications through the trade-off between transmitting power and channel size. As shown in Figure 3, monocycle signal we designed creates 50% larger current than monopulse signal, and if we can use more scaled technology, signal frequency can be increased to the peak of transfer function. Consequently performance of the transceiver circuit is expected to increase further

Figure 5 shows transmitter circuit which consists of pulse generator, pulse delay & MUX, and H-bridge with inverters. The input of pulse generator is 1GHz CLK signal and a short pulse of 300ps duration is created at every rising edge [3]. Pulse delay element makes the generated pulse to be delayed or advanced by the amount of the pulse width, and then depending on the DATA_IN signal, sequence of pulses to the inverters in H-bridge circuit is determined. Finally a monocylcle current will be generated through a coupled inductor. Since the induced current depends on pulse width and overlap between delayed and advanced pulse, strict control of pulse delay and MUX composed of switches is required. The size of drivers in H-bridge which controls I_TX level was determined as twice minimum size through trade-off.

Figure 6 shows receiver circuit using a current-mode sense amplifier. It senses changes of the induced current, I_RX in coupled inductors. Due to low level of I_RX (~9μA) a current-mode sense amplifier is used, which is more sensitive and less area-consuming compared to a voltage-mode sense amplifier [4]. For pre-charge stage, a top pMOS is turned on during low CLK_RX signal, which makes both output nodes metastable. At the sensing stage, high CLK_RX signal enables the current paths between current back-to-back inverters and a current source transistor on the bottom by turning on the isolation nMOS. Once current paths have been enabled, even very small current differences on the current paths can be sensed and set 1 or 0 on both output nodes and is latched by a RS latch that keep the output for one CLK_RX cycle. Therefore the rising edge of CLK_RX should be synchronized to induced current peak in order to maximize the sensitivity of the receiver.

The size of back-to-back inverters and current source transistors determines the sensitivity of a sense amplifier; large sizes lead to high gain and small delay in sensing. Also, input impedance, Rin seen from the inductor should be minimized because large Rin reduces the peak value of I_RX. Rin is calculated by current source transistors and isolation transistors. It is approximately 600Ω by equation (1). Large isolation transistors are preferred to reduce Rin. To fit receiver circuits into the 20μm x 20μm inductor, however, Rin is about 600Ω that does not lower the sensitivity. The current source transistors are biased by DC voltage around 1.8 V with ideal 150um current source after considering low-power dissipation.

$$R_{in} = 0.5 \times \left(\left(g_{m\_isolation} + g_{mb\_isolation} \right)^{-1} \| \, r_{o\_current\_source} \right) \simeq 600\Omega \quad (1)$$

Simulations over corners in Figure 7 show that the phase and amplitude of I_RX varies corresponding to process variation and temperature. Main reason of this variation is inverter chains in TX; since variation tolerance is not considered when designing it, the pulse duration and magnitude is vulnerable to process variation. Since we use BPSK as modulation method and assume AWGN, calculated bit error rate (BER) is about 10^{-5} with 0.79 pJ/b signal energy and 0.1 pJ noise energy at 1Gb/s.

Conclusion

A 2.18mW 1Gb/s inductive coupling transceiver has been implemented. Monocycle signaling and delay-and-mux scheme in the TX improves power transfer efficiency, and the current-mode sense amplifier in the RX reduces required power consumption in a transmitter. As a result, this works achieved one of the best power efficiency and layout area compared to transceivers reported at ISSCC shown in Figure 8.

References

[1] M. Sasaki and A. Iwata, "A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication scheme," *Symposium on VLSI Circuit Digest of Technical Papers*, pp. 348-351, 2005.

[2] N.Miura et al., "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link", *IEEE J.Solid-State Circuit*, Jan 2007.

[3] X.Zhang et al., "A low power CMOS UWB pulse generator," *Circuit and Systems,* 48th Midwest Symposium on, Vol. 2, pp. 1410-1413, 2005.

[4] T. N. Blalock et al., "A High-Speed Clamped Bit-Line current-Mode Sense Amplifier," *IEEE J.Solid-State Circuit*, Apr. 1991.

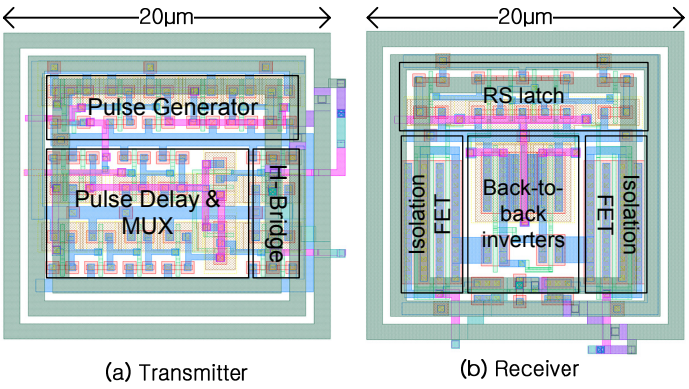
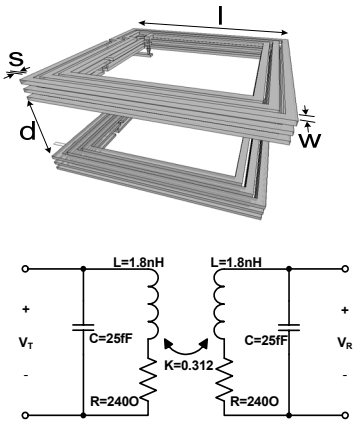


Figure 1: Layouts of transmitter and receiver



Parameter	Value
Distance (d)	15μm
Wire Width (w)	1μm
Wire Space (s)	0.5μm
Diameter (l)	20μm
Turn (n)	3
Layer (m)	3

L	1.8nH
R	240Ω
C	25fF
k	0.312
M	0.542nH

Figure 2: Inductor design and equivalent circuit

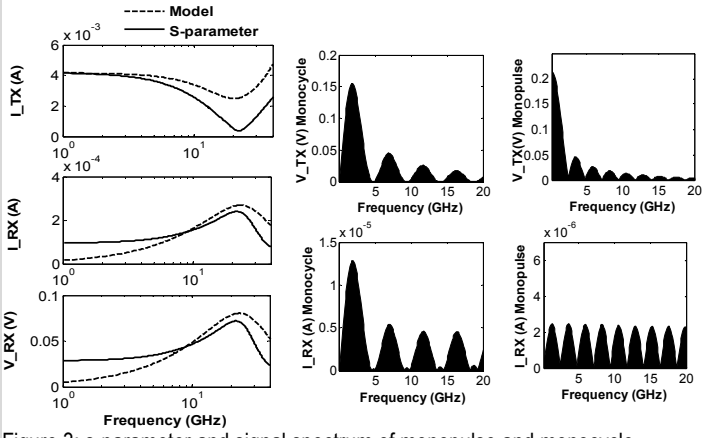


Figure 3: s-parameter and signal spectrum of monopulse and monocycle

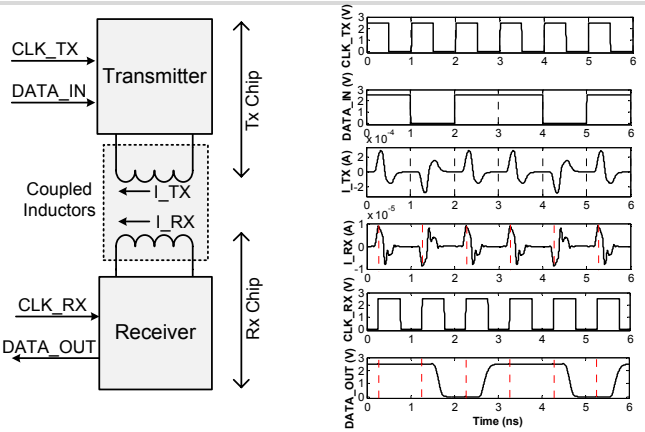


Figure 4: Top level diagram and waveform

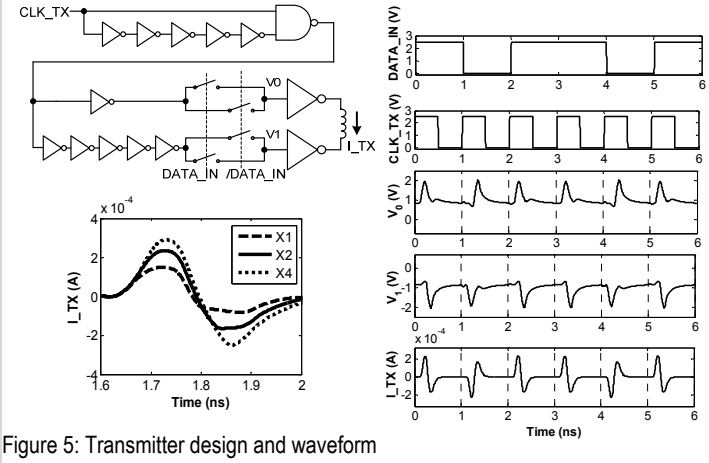


Figure 5: Transmitter design and waveform

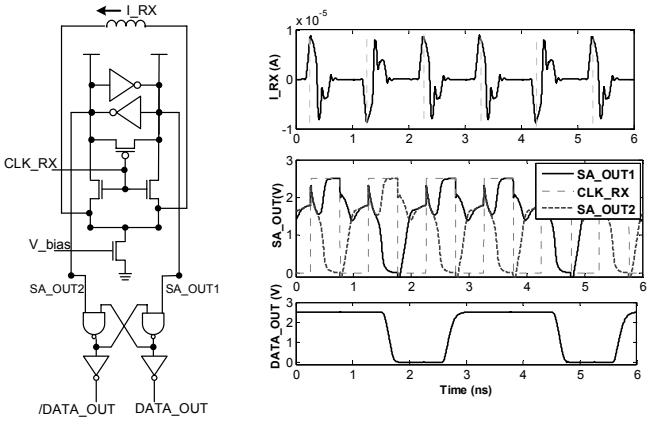


Figure 6: Receiver design and waveform

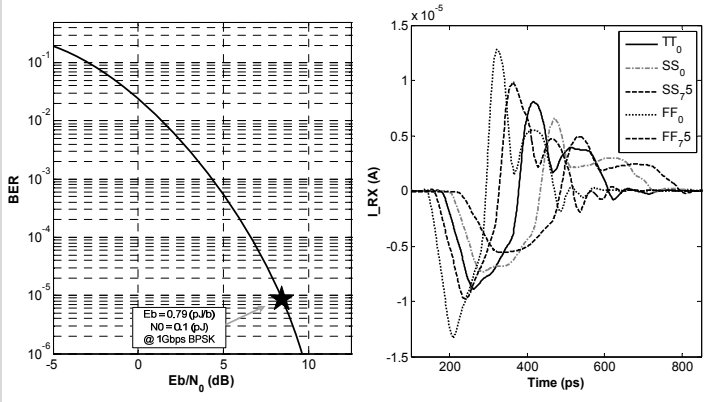
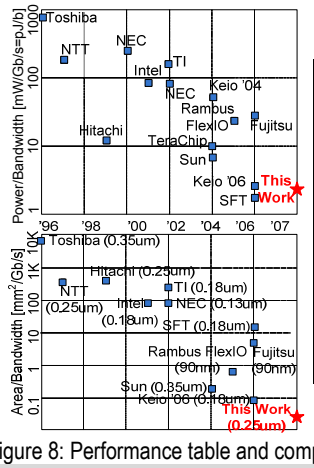


Figure 7: BER graph and corner simulation results



Parameter	Value
Channel Bandwidth	1Gb/s
Channel Pitch	20μm
Power Dissipation	2.18mW
-Transmitter	0.87mW
-Receiver	1.31mW
Total Area	400μm^2
Power/Bandwidth	2.18mW/Gb/s
Area/Bandwidth	400μm^2/Gb/s
Process	0.25μm

Figure 8: Performance table and comparison