A High Power Class D Audio Amplifier

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Class D high power audio amplifiers are high efficiency amplifiers for products where battery life is critical. The high power efficiency and low power consumption for a given output power reduce the heat sink requirements drastically. This allows for compact design and a low-weight-small-size reducing the overall cost of the chip. Conventional class AB audio amplifiers are around 60-70% efficient, where as class D architectures are up to 90% efficient due to the switching feature of the amplifier. This feature stems from the fact that the output stages of the amplifier are never operated in the active region but are either on or off, which ideally results in a 0W power dissipation[1].

In order to achieve the maximum output power, we are using a bridge-tied-load (BTL) output which is differential and allows for twice the voltage swing of a single-ended (SE) design. External LC filters are placed at the outputs to reconstruct the audio signal back from the PWM encoding. This report presents a Class D design which can output over 1W into conventional 8Ω speakers. We also analyze THD to ensure that the audio outputs are not highly distorted. Design schematics for individual stages are shown in Figures 3 and 4.

Triangle Wave Generator

A 250kHz square wave clock signal generates a reference triangle wave needed to sample the audio signal. A push-pull architecture was designed to slew the square wave clock into a triangle wave. PMOS and NMOS current mirrors set DC current biasing through the pull-up and pull-down networks. Transmission gates are used in each network as switches with opposite timing to control the charge/discharge of an output capacitor. The sizing and current biasing was determined by:

$$I_{SS} = I_C = C\ dv/dt$$

The challenge in this design was to optimize the transistor sizing to achieve equal and well timed slew rate on both the high and low transitions of the clock. These switches are fed by the clock input and are sized large in order to minimize impedance effects on the output charge/discharge and reduce the nonlinearity of the output voltage transitions. Finally, the current mirrors are sized to achieve the slew rate needed for the 250kHz clock and minimize the output capacitance needed for adequate slewing. This capacitance of roughly 3pF is large enough to compensate for the gate capacitance variation at the comparator input.

Comparator

A comparator is essentially a high gain open loop op amp, railing the output to gnd or Vdd based on the input voltages. The architecture for this block was based on the tradeoff for gain, bandwidth, output swing, and power consumption. The available options included one/two stages, cascoding (un)folded, and gain boosting. However, based on what we needed, the two stage non-cascoded design worked best[2]. It has higher gain and moderate bandwidth. Our first stage is a differential input, SE output active load amplifier with another common source amplifier as the second stage. The second stage serves as the high output swing stage needed to create the rail-to-rail PWM signal for driving the output buffers. Because this is a two stage design, it was more challenging to achieve proper DC biasing to ensure all FETs are in saturation. Also, we used low bias currents to both minimize power and maximize gain. This is because for both stages:

$$A_v = -g_m(r_{01}//r_{02}) \propto I_D^{-\frac{1}{2}}$$

To further increase the gain for higher comparator resolution, we increased the length of the r_0 FETs while maintaining constant W/L ratio since $r0 \propto 1/\lambda \propto L$. This tweaking limited the bandwidth too much, so we reduced the widths of the 2nd stage to compensate for bandwidth, accepting a slightly lower gain. We achieved a gain of around 500 V/V with a ~30MHz bandwidth.

Level Shifters

2.5V to 5V level shifters were designed to ramp up the PWM output of the comparator to 5V for the output buffers. We selected our design based on a differential amplifier input with cross-coupled PMOS loads for fast acting response. The cross-coupled reinforcement allows for the greater voltage shift of 2.5V to 5V. An advantage of this architecture is that it provides both the level shifted output and its inverse, negating the need for another level shifter for the second buffer chain.

Output Stages

In order to drive 1W of power to the load, R_{DSON} FETs in the output H-bridge had to be reduced. This is achieved by large FETs on the order of mm widths. This meant that a tapered chain of inverters was needed to drive the large gate capacitances of the output bridge to avoid distortion caused by unequal rise and fall times. Following equations were used to determine the optimum number of stages (N), and sizing for each stage:

$$F = {C_{out}}/{C_{in}}$$

$$N = \frac{\log(F)}{\log(f_{opt})} \quad with\ f_{opt} = 3.6$$

And $C_{i+1} = f_{opt}\, C_i$ for the i_{th} inverter in the chain. Because of the large sizing of the final inverters, we had to use large amounts of fingering to achieve proportional aspect ratios.

Results

The design goal of a peak output power of 1.1W using this 5V BTL architecture was achieved. However, not every specification of the chip performed greatly. As shown in Figure 7, there was a slight DC offset between at the output terminals, which was caused by the inability of the comparator to continue capturing the PWM waves at the peak and trough of a high amplitude input. This was due to the speed limitations of the comparator. This caused higher THD values than desirable. THD values obtained can be seen in Figures 5 and 6 which were obtained by the DFT of the output signal (Figure 2). Also, as can be seen in Figure 8, the efficiency of the amplifier is not very high, and this was caused entirely by the large output buffer stages and their high dynamic power dissipation. Typical class D efficiencies are greater than 90%. Due to time constraints other output stage architectures to achieve our goal could not be analyzed. Specification measurements were calculated as follows:

$$THD\ (\%) = \frac{P_2 + P_3 + P_4 + \ldots P_N}{P_1}$$

$$Eff.(\%) = \frac{P_{LOAD}}{V_{dd2.5} * I_{dd2.5} + V_{dd5} * I_{dd5}}$$

Where $P_1$is at the audio frequency. Layout is given in Figure 1. DRC and extraction came out clean. However, LVS registered terminal errors and some net errors on output stages which could not be fixed due to limited time and experience.

References

[1] H. C. Foong, M. T. Tan, "An Analysis of THD in Class D Amplifiers," IEEE APCCAS, pp. 724-727, 2006.
[2] B. Razavi, "Design of Analog CMOS Integrated Circuits," Ch. 9.
[3]"B. Zhang, L. Liang, X. Wang, "A New Level Shifter with Low Power in Multi-Voltage System", IEEE, pg. 1, 2006.
[4] Texas Instruments, TPA2012D2 datasheet, www.ti.com

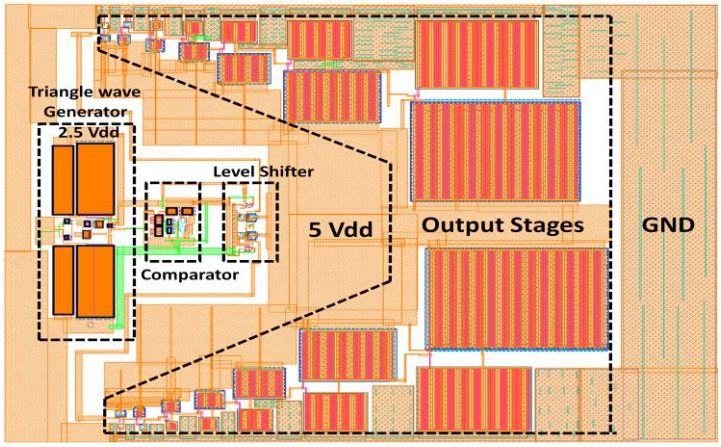

Figure 1: Layout

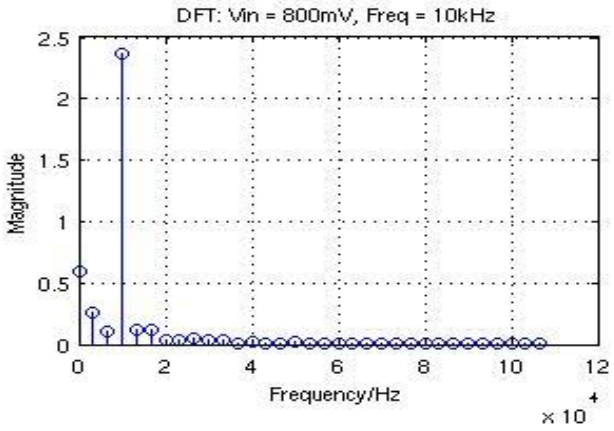

Figure 2: DFT of Output Signal

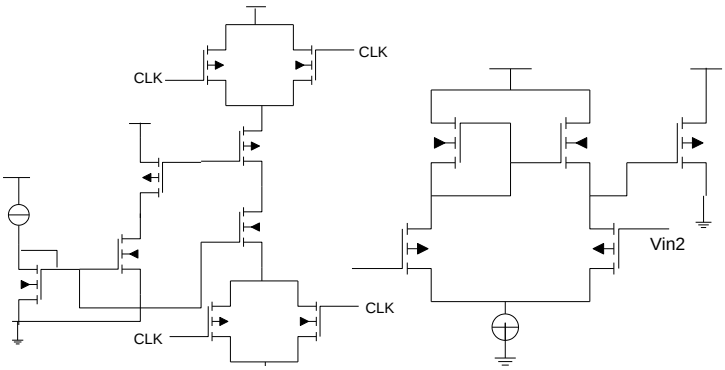

Figure 3: Triangle Wave Generator (Left), Comparator (Right)

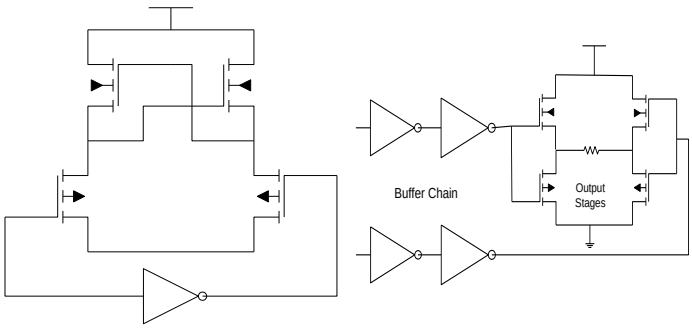

Figure 4: Level Shifter (Left), Output Stages (Right)

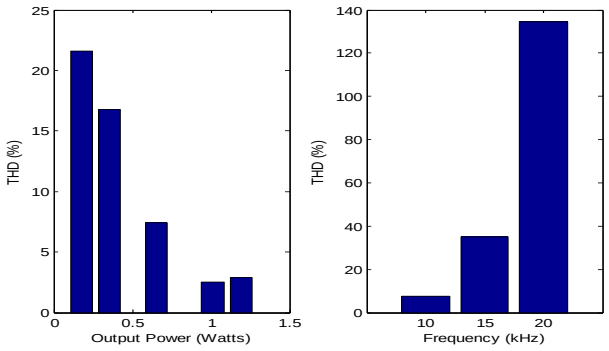

Figure 5: THD vs. Output Power and Frequency with DC Offset

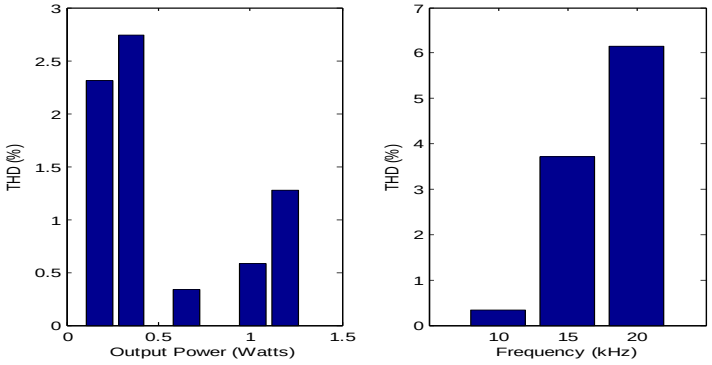

Figure 6: THD vs. Output Power and Frequency without DC Offset

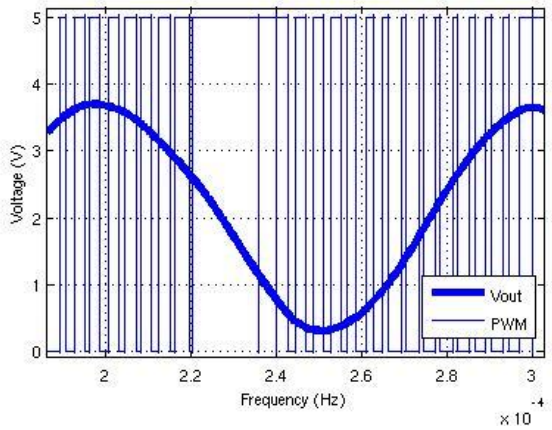

Figure 7: Reconstructed and PWM Signal

System Specification		
PARAMETER	**VALUE**	**UNITS**
Maximum P_{out}	1.192	W
Nominal Efficiency	47.33	%
Max Input Swing	2.4	V_{ppk}
Max Output Swing	8.471	V_{ppk}
Reference Gen. P_{DISS}	377.1	µW
Comparator P_{DISS}	510.1	µW
Level Shifter P_{DISS}	118.575	nW
Output Stages P_{DISS}	404.093	mW
Peak Total P_{DISS}	404.98	mW
Bandwidth	20-20k	Hz

Figure 8: Results

T (°C)	THD % w/ DC offset	THD % w/o DC offset
-20	4.3	8.6
0	2.3	1.3
27	7.4	3.4
40	8.6	7.5
60	8.9	9.6