Temperature Compensated Logarithmic Amplifier for CMOS Image Sensor

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Introduction & Motivation

For sensing lights by human eyes, it is more suitable to use logarithm instead of linearity. Human can recognize in detail for weak signal and roughly for large signal. Therefore logarithmic amplifier deserves to be used in image sensor. The most challenging part for CMOS logarithmic amplifier is temperate compensation [1]. In addition, dark current is major noise generation for CMOS image sensor. In this project, we provide novel method to compensate temperature and dark current.

Circuit Topology & Methodology

The architecture of the proposed Logarithmic Amplifier is shown in Fig. 3. Photodiode is represented as the equivalent model where photo current, $I_{ph} = q\lambda\eta P_o A/hc$ [2]. However, dark current still flows even if there is no incident light in the photodiode. This is due to the reverse bias in PN junction resistor of photodiode, R_{sh} in the equivalent model. Even though dark current is highly dependent on temperature, the effect is not critical if the reverse bias in photodiode is close to zero. We can keep this reverse bias close to zero using a zero bias feedback buffer [3]. This dark current compensated I_{ph} is now logarithmically converted to V_{gs} of M_1 which operates in the subthreshold region like below:

$$V_{gs} = \zeta V_T \ln\left[(I_{ph} + \Delta I_{ph})/I_o\right] \qquad (1)$$

where ΔI_{ph} is dark current from R_{sh}, $I_0 \propto T^3$ and $\mathrm{V_T} \propto T$. To maintain this logarithmic relation, V_{gs} of M_1 should be less than threshold voltage. This means higher ratio of $(W/L)_{M_1}$ is required to increase dynamic range, but it also increases the size of M_1. To minimize pixel size and related circuits, zero bias feedback buffer and logarithmic amplifier can be shared by adjunct 6 pixels such as Fig. 2.b.

V_{gs} of subthreshold transistor is then transferred to the temperature compensation circuit through source follower and column select switches. In equation (1), I_0 term can be eliminated if V_{gs} is subtracted from V_{ref}, which can be obtained from I_{ref}, the temperature invariant current. As $V_{ref} = \zeta V_T ln\,(I_{ref}/I_0)$, $V_{in} - V_{ref} = \zeta \mathrm{V_T} \ln(I_{in}/I_{ref})$ is proportional to temperature [4]. In Fig. 3, we devise $V_{in} - V_{ref}$ using differential amplifier with active current mirror. If $I_{ss} \gg \frac{1}{4}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$, we can approximate I_{diff} as below:

$$I_{diff} \approx \sqrt{\mu_n C_{ox}\frac{W}{L}I_{ss}}\,(V_{in1} - V_{in2}) \qquad (2)$$

If we make $I_{ss} \propto \mu_n T$, then $I_{diff} \propto \mu_n \sqrt{T} V_{id} = T^{-1.5+1.5} = T^0$, which means I_{diff} is independent of temperature. This I_{ss} can be implemented using differential amplifier again. In this case, we set $I_{ss2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \propto \mu_n$ and $V_{id2} = V_{ref1} - V_{ref2} \propto T$. In practice, μ_n is not exactly proportional to $T^{-1.5}$. We can adjust the bias point of I_{ss2} to control the temperature dependence of μ_n so that we can make I_{diff} temperature independent.

The temperature independent current source I_{ref} is also required for temperature compensation. Since the drain current of PMOS exhibit the negative TC, we can compensate the temperature dependence of PMOS by the bandgap voltage which has a maximum reference voltage at zero TC and minimum reference voltage at high temperature. The temperature derivative of saturation drain current of PMOS is given by

$$\frac{\partial I}{\partial T} = \frac{\partial \mu_n}{\partial T} C_{OX} \left(\frac{W}{L}\right)_P {V_{od}}^2 + \mu_n C_{OX} \left(\frac{W}{L}\right)_P 2V_{od} \frac{\partial V_{od}}{\partial T} \qquad (3)$$

To set this zero, we use the reference voltage which is represented by $V_{REF} = V_{BE} + V_T \ln n$ [5]. In the bandgap generation block of Fig. 5, M_{P1} and M_{P2} are designed with long channel devices to reduce the channel length modulation. In the error amplifier block, the temperature dependent offset voltage of the error amplifier is given by [6]:

$$V_{OS} = \Delta V_{THN} + \frac{g_{mP}}{g_{mN}} \cdot |\Delta V_{THP}| + \frac{1}{2}\sqrt{\frac{2I_{DN}}{\mu_n C_{OX}(W/L)_N}}\left[\frac{\Delta (W/L)_P}{(W/L)_P} - \frac{\Delta (W/L)_N}{(W/L)_N}\right] \qquad (4)$$

To reduce the temperature dependence of the offset voltage, the (W/L) of M_{P3} and M_{P4} should be small and the (W/L) of M_{N1} and M_{N2} should be large.

Simulation result

The right graph in Fig.4 shows the change of I_{ref} according to temperature variation. The drain current of PMOS exhibits a finite curvature. This temperature invariant current shows the 1% deviation from our specification. The left graph in Fig.5 shows the relation between voltage and current of M_1 comparing the case when there is no compensation of dark current. The dark current compensation is especially important when photocurrent is below 1 nA as the reverse bias becomes higher in the lower current. The zero bias feedback buffer guarantees less than 5 % of dark current when photo current is 100 pA. However, the right graph in Fig.5 shows that there is severe temperature dependency of subthreshold region as most parameters such as V_T and I_o are functions of temperature. Fig.6 exhibits the logarithmic relation between photo current and output current where temperature compensation is completed. Within specified temperature range, it only shows 1.6 % of maximum variation from the operation at room temperature. Compared to ideal logarithmic response, this log amplifier shows 1.35 % of logarithmic mismatch.

Conclusion

Fig.8. summarizes the overall result and comparison with other published works. Comparing to merit of each work, we can achieve relatively large dynamic range, less logarithmic mismatch, and less temperature dependence. However, the size of each pixel is not exactly matched to our previous specification as dark current compensation circuit is added. This amplifier can be utilized in the severe environment where temperature and light intensity vary dramatically.

References

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[6] Chi Yat Leung; Ka Nang Leung, "Design of a 1.5-V high-order curvature-compensated CMOS bandgap reference," *Circuits and Systems, ISCAS. Proceedings of the International Symposium on*, May 2004.

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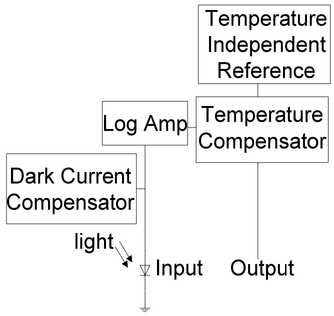

Figure 1: Block Diagram

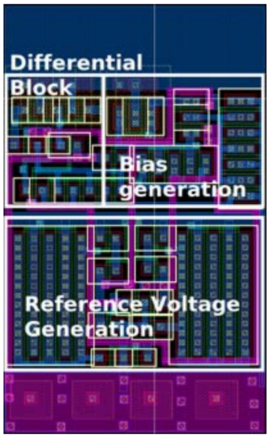

Figure 2.a: Layout of Temperature Compensation.

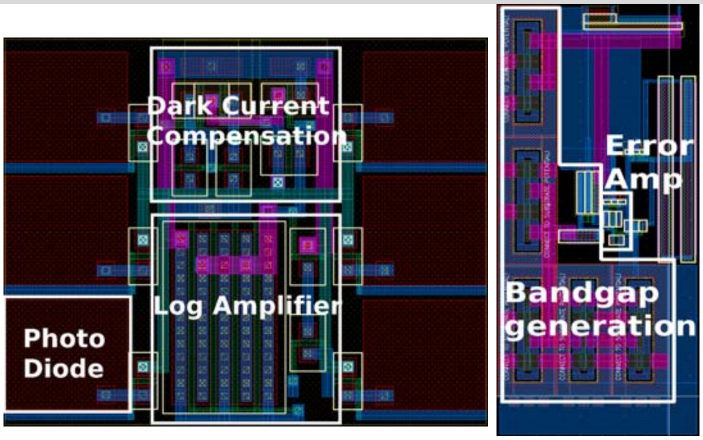

Figure 2.b: Layout of Pixel and Bandgap reference.

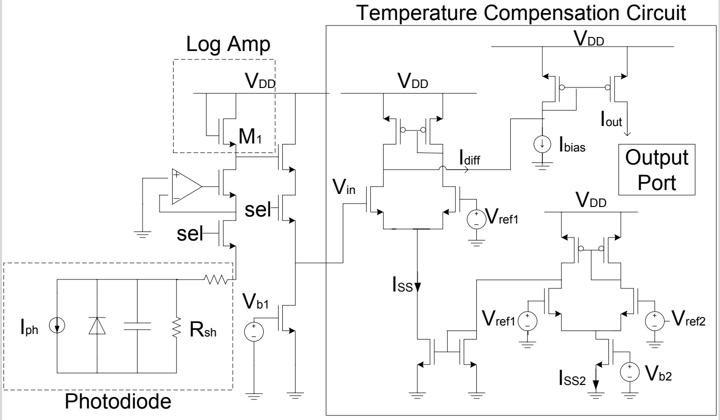

Figure 3: Schematics of Loa Amp. and Temperature Compensation Circuit.

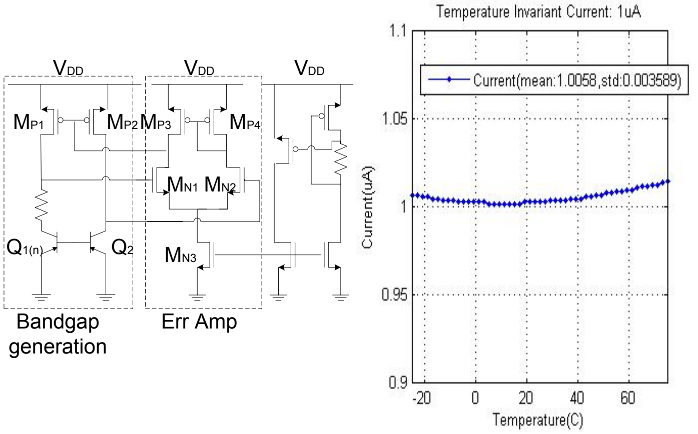

Figure 4: Schematic and Result of Bandgap reference.

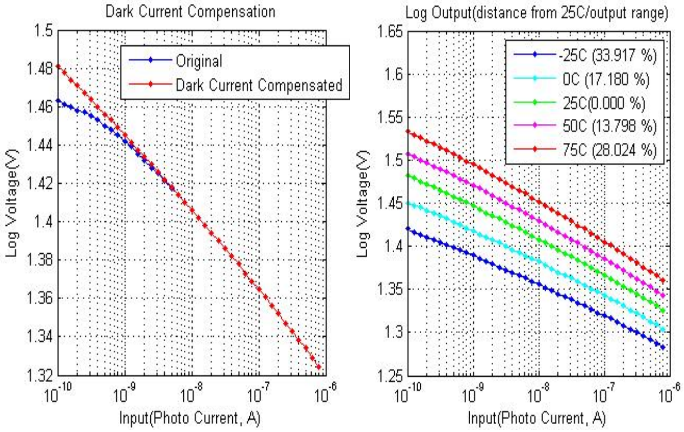

Figure 5: Result of Dark current compensation and Log Amp. output.

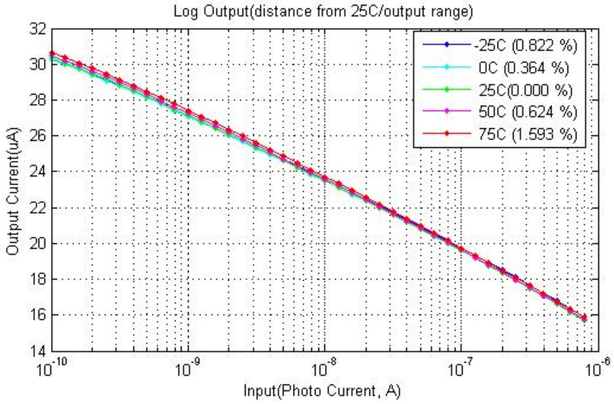

Figure 6: Result of the temperature compensated output.

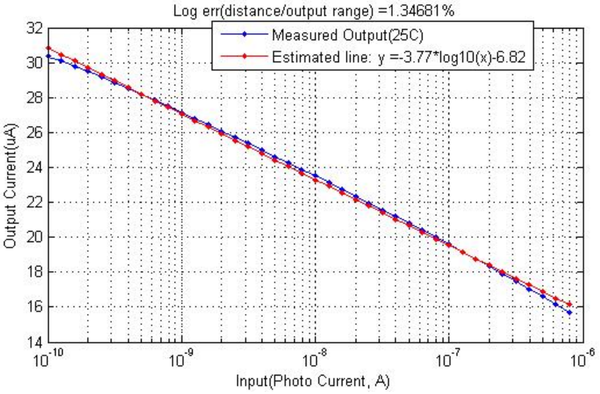

Figure 7: Comparison to ideal logarithmic response

Specification	**This work**	**Infinion Tec. [7]**	**Koli *et al.***
Dynamic Range	80dB	68dB	60dB
Log Error	1.35%	3%	±3dB
Temperature Error	1.59%	1.2%	±1dB
Settling Time	35us		
Power Supply	2.5V, 3.3V	2.5V	2.5V
Power Consumption	906uW	1.675mW	3mW
Log Slope	-3.76uA/dB		
Output Range	15uA ~ 31uA	0uA ~ 400uA	12mV ~ 29mV
Size (pixel / chip)	8.5um×6um	1.46 mm^2	3.2mm^2

Figure 8: Table of Summarizing the results.