EECS 413 Final Report – Group 7
A CMOS LNA and Mixer for FM Receivers
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Introduction
Due to the unabated growth of wireless technologies, the demand for high-performance, small, low-power RF devices has soared in recent years. In this report, our team presents the design and simulation of an LNA and Mixer, which are key front-end components of any radio receiver. In our project the targeted frequency was the FM radio band (88MHz – 108MHz), which has an IF frequency of 10.7MHz. We attempted to address classical design tradeoffs: gain, bandwidth and power consumption. The challenge was to deliver as much amplification as possible with minimal signal distortion and power consumption over our 20MHz spectrum.

LNA Design
In RF design, high gain is often desired at the initial stages of a receiver. One of the reasons is that high initial gain attenuates the effects of noise in later stages in the overall noise figure (NF) of the system, which is calculated using the expression: [1]

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}}$$

Where G corresponds to the gain of each stage. In our design, therefore, the LNA parameters dictate, in large part, the overall NF of the system. Another task in our LNA design was to match the input impedance to 50Ω. To achieve matching input impedance, we used the inductive degeneration method on a CG LNA. Figure 5 shows the input reflection coefficient (-31dB at 100 MHz), which shows a good match. Due to size limitations, however, the inductor had to be placed off chip. The input impedance equation is given below (ignoring body effect and channel length modulation):

$$Zin = \frac{sL}{sL_1(g_m + sC_{gs12}) + 1}$$

The CG LNA topology has the advantage of offering a wideband input match with low susceptibility to input parasitics such as those introduced by bond pads [2]. The small signal voltage gain of the CG LNA can be given by the expression:

$$Av = \frac{g_{m12} g_{m14} R_1}{g_{m14} + sC_{gs14}} \sim g_{m12} R_1 \qquad (lowfrequency)$$

Typical gains for a single stage LNA topology are around 15 to 20 dB [2]. We took 20dB as reference value for our initial calculations. Figure 6 shows the finalized LNA schematic and its LVS-clean layout are shown in figure 1.

Mixer Design
A double balanced mixer was used to both translate the signal from the LNA to a low IF frequency and to maximize the overall gain. The mixer was implemented using a double-balanced Gilbert cell. This topology offers advantages such as minimal LO feed and generates less distortion since its inputs are differential. Because our LNA design was single-ended, the input signal at the mixer (LNA output) was referenced to a DC voltage through a resistor to emulate a differential signal from a single input port. The bias voltage was supplied by a bias generator on chip. Figure 2 shows the schematic and corresponding layout of the mixer. The conversion gain of this type of topology is given by the formula [1]:

$$A_{conv} = \frac{2}{\pi}\sqrt{\mu C_{ox1}(W_1/L_1)(I_{M1} + I_{M2})} * R_l$$

Where Rl is the output impedance looking upwards from the IF output. The PMOS mirrors force the current flow to be evenly divided in the mixer.

Simulation results
Simulations were executed in two different ways. The LNA and Mixer were tested individually, as well as in conjunction. Typically in RF design, S parameter (SP) analyses would be emphasized, but we chose to focus on transient and AC analysis results, which the group felt more appropriate to show in this report. The LNA simulations generally involved AC analysis, while the mixer simulations were carried out through transient signal inputs. Figure 3 shows the transient signals of different stages in our system. For testing purposes, we connected the LNA to a 5th order Butterworth filter to obtain the final sinusoidal signal. Figure 4 shows the signal magnitudes in frequency domain. Our input RF signal was at 100 MHz and our output IF signal at 10MHz. From the plot, the total gain can be seen to be close to 40dB. Measured individually, the gains add up to be slightly higher, which indicates that there is loss in the coupling capacitor between the two components.

Conclusion
Our design meets most of the specifications that we had aimed for at the beginning of the project. The gain of the LNA was less than what we had initially set (>30dB) but this was compensated by the high gain provided by the mixer in the overall system. Higher gains for the LNA were achieved (up to 35dB) with a multiple stage topology, but this initial circuit had high NF (close to 11dB) so our group opted for the single-stage CG LNA, which satisfied our goal for NF (< 5dB). Table 1 puts our results in perspective with previous works. Overall, our group considers that the performance of the system satisfactorily met most of what we had initially set at the beginning of project. Quite a few of the techniques and simulations used for performance optimization and measurement were borrowed from books and papers beyond the scope of basic analog design, but we unanimously recognize that such a foundation was essential to the execution of this project, as it allowed us to build upon and learn a great amount.

Design link:
/afs/umich.edu/class/eecs413/f07/groups/group7/final_project

References
[1] Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd Edition
[2] Allstot, D.J.; Xiaoyong Li; Shekhar, S. "Design considerations for CMOS low-noise amplifiers", RFIC Symp., 2004. Digest of Papers.2004 IEEE 6-8 June 2004 Page(s):97 – 100
[3] Karanicolas, A.N. "A 2.7-V 900-MHz CMOS LNA and Mixer" IEEE JSSC Volume 31, Issue 12, Dec. 1996 Page(s):1939 - 1944
[4] E. Zencir, N.S. Dogan and E. Arvas, "A low-power CMOS mixer for low-IF receivers, "IEEE RAW-CON pp. 157-160, Aug. 2003

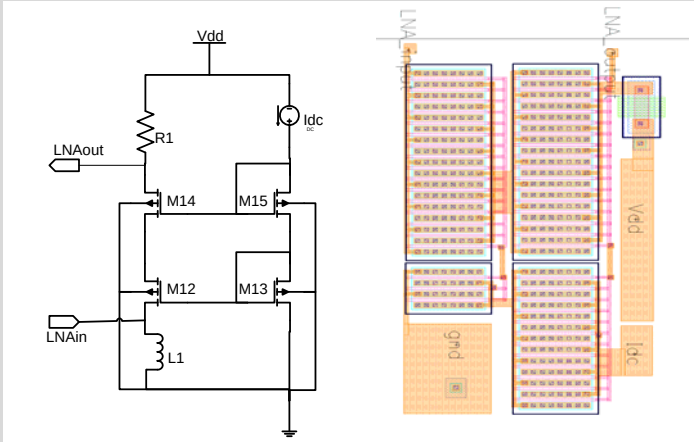

Figure 1: LNA schematic and layout

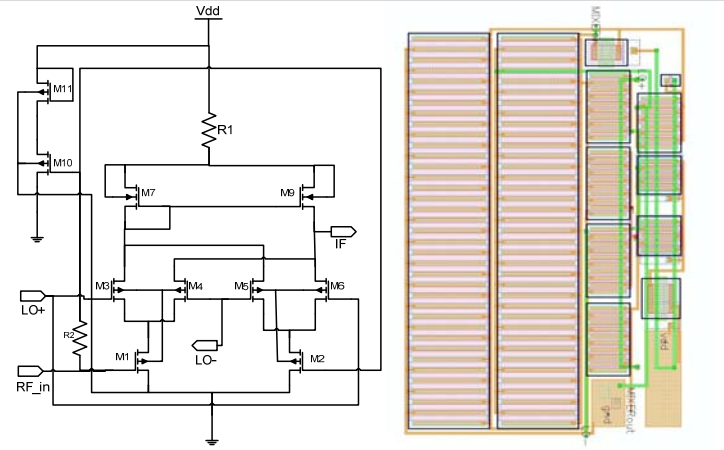

Figure 2: Mixer schematic and layout

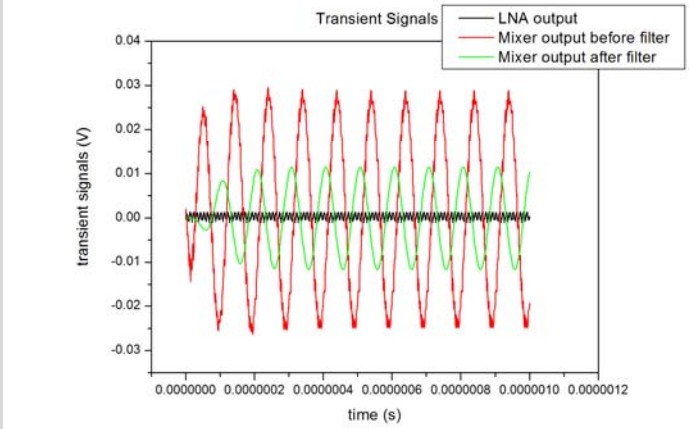

Figure 3: Measured input and output signals of different stages in the system

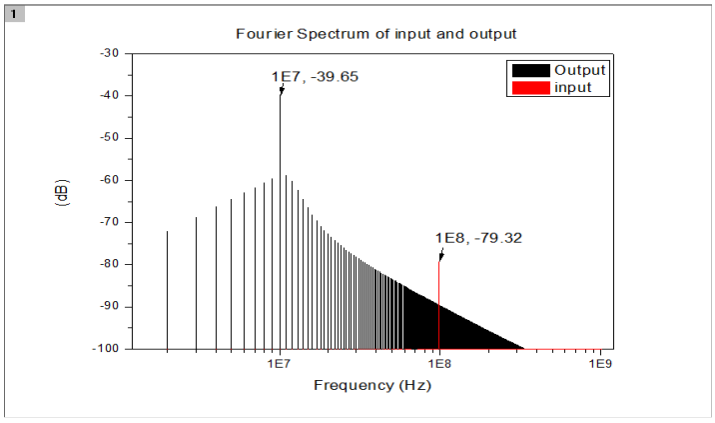

Figure 4: LNA input (100MHz) and Mixer output (10MHz) signals

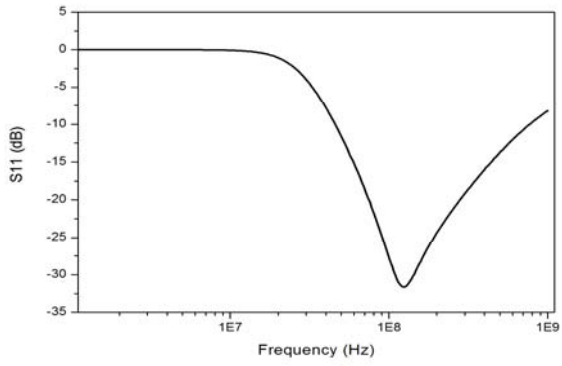

Figure 5: System input reflection coefficient (50Ω reference)

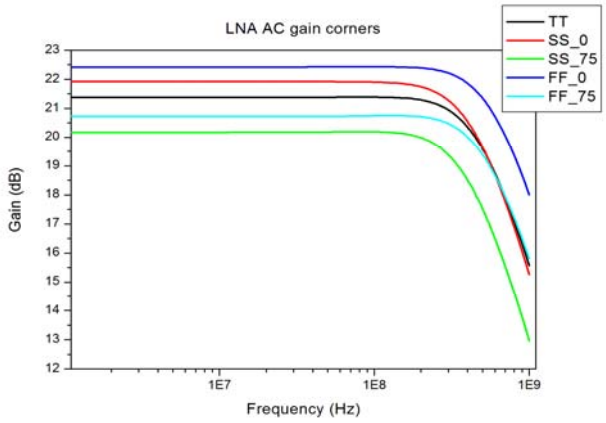

Figure 6: LNA Gain over corners simulation

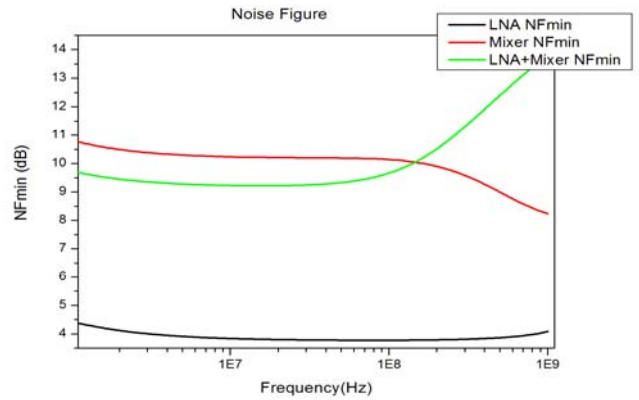

Figure 7: System noise figure

Specification	LNA	Mixer	LNA[3]	Mixer[4]	Units
RF Frequency	100	100	900	435	MHz
Power	3.9	3.105	20	5.4	mW
BW	>530	NA	<200	NA	MHz
Gain (AC-LNA or Transient-Mixer)	22.29	20.4	15	20.8	dB (V/V)
NF	3.77	10.14	1.9	5.8	dB (W/W)
1dB Compression point	-6.34	-14.16	-15.2	-21	dBm
Voltage Source	2.5	2.5	2.7	2.5	V

Table 1: Performance Summary and Comparison.