A High Frequency CMOS Low Noise Amplifier Design for Cellular Applications

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Introduction and Motivation

Low noise amplifiers (LNAs) present a solution to the high gain low noise tradeoff by offering high gain while minimizing noise corruption. This results in increased sensitivity or increased range for a given SNR. The cellular industry relies on LNAs in receiver systems to boost low amplitude signals in both basestations and mobile handsets. EGSM band is a widely used frequency band for cellular technology and handset uplink to cellular basestations operates from 880-915MHz. LNA integration into a receiver for an EGSM basestation provides larger range connections, reduction of dropped calls, greater resistance to out-of-band interferers, and improved overall call performance. Furthermore, demand for reductions in size, cost, and complexity of single-chip transceivers clearly motivate integration of LNA components into CMOS technology.

Circuit Topology and Components

Our LNA system consists of three components: a high output impedance temperature independent band-gap referenced current source, a cascoded common source gain stage with input matching network, and a single input to differential output converter. A block diagram of our system can be seen in Fig. 1.

The current source begins with a cascoded self-biasing circuit, which essentially operates as two current mirrors attached in series that take their references from opposite branches, creating a cyclic self-biasing circuit (a schematic of the current source can be seen in Fig. 2). The self-biasing allows the current source to be less sensitive to the supply voltage, and the cascoding is implemented to further improve supply rejection. In order to uniquely define the currents in the two branches of the self-biasing circuit, a diode connected load (*M9*) functioning as a resistor is added in series with the right branch. The right branch is used to mirror a supply insensitive current to an additional branch used to bias the gate of *M13* through a resistive divider.

At this point, we have a temperature dependent current source that is insensitive to supply variation. To achieve temperature independence, we can turn our current source into a band-gap reference by placing a single parasitic pnp bipolar junction transistor below M4 and *n* identical pnp devices below *M9* and *M12*. It has been shown that if two BJTs operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature; we have now setup this exact situation. Now, by making the resistance of *M12* a multiple of *M9*, we can tune this ratio to change the proportionality constant of V_{BE} with temperature. The source follower stage will have a positive temperature coefficient, so we tune the ratio of resistance of *M12* and *M9* to have a negative temperature coefficient in order to cancel the temperature dependence of the output current. A plot of the current variation with temperature can be seen in Fig. 3.

The most important component to our design is the cascoded common source (CS) gain stage of the LNA. The CS NFET was cascoded in order to increase the gain, increase unilaterality, and increase isolation of the input and output tuned elements. Also, cascoding reduces the effects of C_{gd} at the input; this pushes our pole frequency higher as can be seen with open circuit time constants. This makes our unity gain frequency $\omega_t = \frac{g_m}{C_{gs}+C_{gd}}$ larger, and since noise factor is inversely proportional to ω_t, our noise performance also improves. The gate of the CS NFET is biased using a cascoded current mirror, and an off-chip dc blocking capacitor isolates the transistor biasing from the input RF signal and blocks any dc offset of the input signal.

Furthermore, on-chip spiral inductors are connected between the blocking capacitor and gate of the CS NFET and between the source of the CS NFET and ground as well as between V_{dd} and the drain of the cascoded NFET for matching, filtering, and pole-zero cancelation. The inductors connected to the CS NFET are used to tune the input impedance to 50Ω (the assumed source resistance R_s) using $Z_{in} = sL_s + \frac{1}{SC_{gs}} + \frac{g_m}{C_{gs}}L_s$, which was derived from the small signal model and where the gate inductor is used as an extra degree of freedom; this will present the best noise response and an acceptable power gain. The inductor connected to the drain of the cascode NFET is used for shunt peaking in order to increase the bandwidth around our center frequency; it also forms a LC tank circuit with the total capacitance of the output node to provide bandpass filtering of our output signal. Moreover, since we would like to avoid small channel effects such as channel length modulation, we decided to make the length of our LNA transistors 1μm. We also found the optimum width for power constrained noise figure of our LNA transistors by using the equation $W_{opt} = \frac{1}{3\omega L C_{ox} R_s}$ to be 276μm.

Our final component in our LNA design was a single input to differential output converter. This is composed of a differential amplifier with one input gate connected to the output from the LNA and the other input gate connected to ac ground. A biasing network was designed to match the dc bias on both gates of the differential pair. We can tolerate a larger noise figure in our differential amplifier since it will be divided by the gain of the LNA stage when determining the cascaded noise figure.

System Performance

We passed DRC and LVS tests and resimulated the performance of our design including extracted parasitic capacitances from layout. Plots of temperature performance, overall gain, S_{11} and S_{12}, and minimum noise figure and actual noise figure appear in Fig. 3, 4, 5, and 6 respectively. Also an image of our final layout appears in Fig. 8. Our system managed to meet all of the specifications required of it, achieving a high gain, low noise figure, and temperature independence with relatively low power consumption. Also, we achieved very good return loss (S_{11}) and unilaterality (S_{12}) over our band, proving our input match to 50Ω and the added benefits of the cascode. Our system met performance specs over most process corners but not all corners, yielding more than ±0.5dB gain ripple in the passband for two corners. Still, this is not of great concern since variable gain amplifiers in the baseband circuitry could easily adjust for this. Also, we did not consider output matching (S_{22}) because in most cellular applications, our LNA system would be feeding a mixer with high input impedance; thus, output matching cannot be currently performed and will most likely not be necessary.

LNAs are ubiquitous in wireless technology, and they provide much needed gain to low amplitude signals as well as a valuable reduction in the significance of added noise from receiver components. The cellular technology industry relies heavily on LNAs for both basestation and mobile handset performance. Our CMOS LNA exhibits performance that would make it well suited for many of the needs of the cellular industry.

References

[1] P. R. Gray and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits.* 3rd ed. John Wiley & Sons Inc., New York, 1993, Chapter 4.

[2] T. H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge University Press, New York, 1998, Chapters 8, 10, and 11.

[3] B. Razavi. *Design of Analog CMOS Integrated Circuits.* McGraw-Hill, New York, 2001, Chapters 5 and 11.

[4] D. K. Scaeffer and T. H. Lee, "A 1.5V, 1.5GHz CMOS Low Noise Amplifier," IEEE J. Solid State Circuits, vol. 32, pp. 745-759, May, 1997.

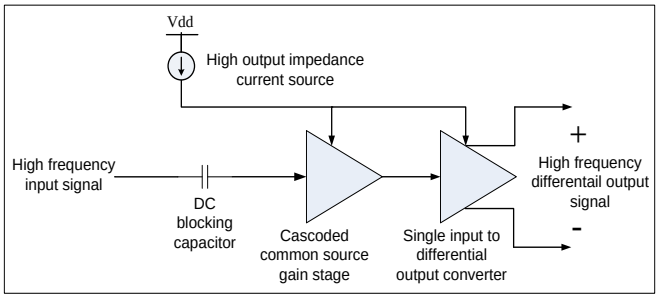

Figure 1: Block diagram of the complete LNA system (all components on-chip except the dc blocking capacitor).

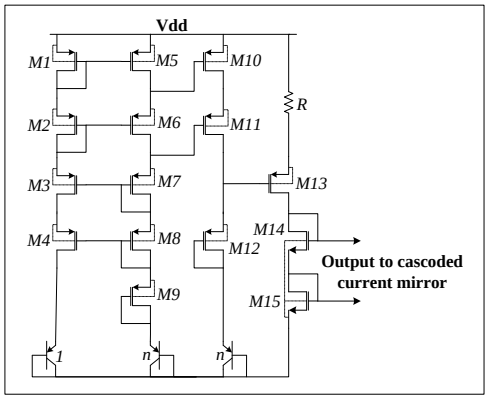

Figure 2: Band-gap referenced temperature independent current source schematic.

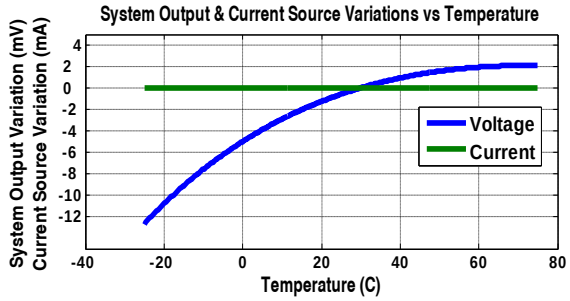

Figure 3: Current source output variation with temperature and entire system differential voltage variation with temperature.

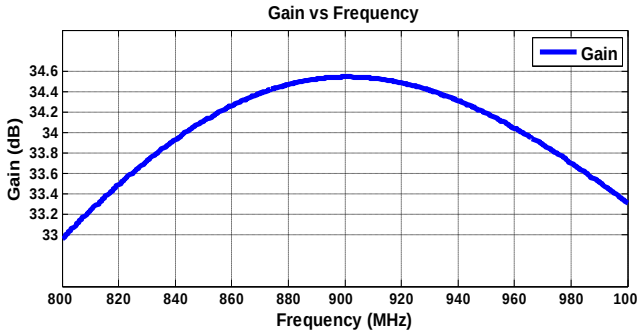

Figure 4: Gain of the overall LNA system over frequency showing the gain ripple and achieved gain

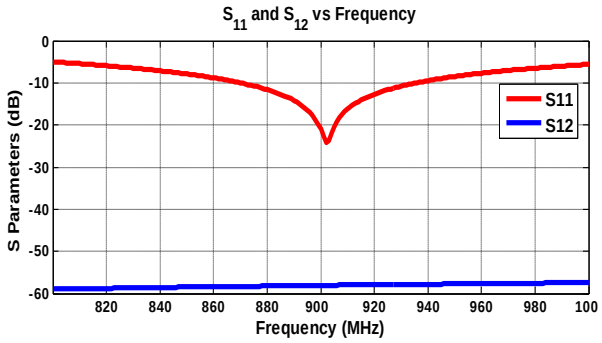

Figure 5: Input return loss (S_{11}) and a measure of unilaterality (S_{12}) for our LNA.

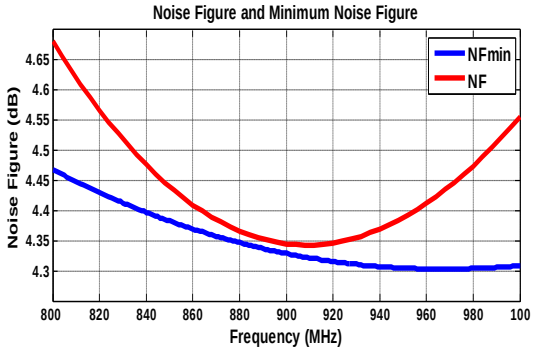

Figure 6: Achieved noise figure and minimum possible noise figure for our LNA.

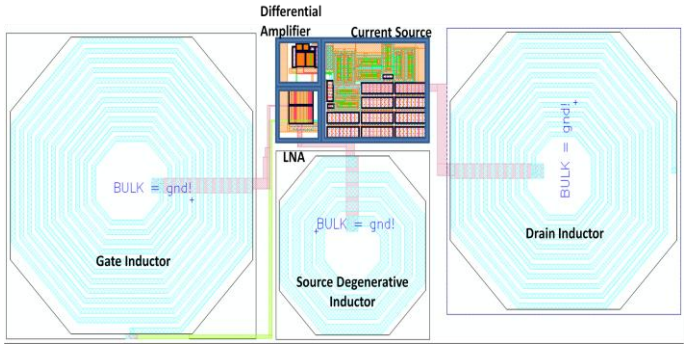

Figure 7: Overall layout of our LNA system.

Specification	Value	Units
Power Consumption	25.74	mW
Max Gain in Passband (A_v)	34.55	dB
Gain Ripple over Passband	0.08	dB
Maximum Noise Figure in Passband	4.366	dB
Maximum S_{11} in Passband	-11.61	dB
-10dB Bandwidth for S_{11}	65.0	MHz
Maximum S_{12} in Passband	-57.97	dB
Current Source Output Temperature Variation	0.15082	µA
System Differential Output Voltage Temperature Variation	14.768	mV
Overall Layout Area	0.2672	mm^2
DRC and LVS Clean Final Design	yes	n/a

Figure 6: Summary of complete LNA performance.