SRAM Sense Amplifier

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Background

Sense amplifiers are one of the most critical circuits in memory design. A sense amplifier speeds memory operation by sensing small initial changes in the data line and driving the stored value to the output quickly. This project addresses voltage sense amplifier design, with the focus on high yield and low delay. Yield is important because each sense amp is responsible for a large segment of the memory array. Sense amp power consumption is relatively insignificant due to this ratio of sense amps to memory cells. Also, a fault detection circuit has been designed to detect the validity of the data that is being input to the sense amp, which could be extremely useful to system designers and in the production test environment. Fig. 2 shows the block diagram of the design.

Design

The voltage sense amplifier designed in this project is a positive feedback differential sense amplifier with high impedance input. This circuit in Fig. 4 has been selected over other topologies to increase the yield and speed of the system. This topology takes advantage of the available complementary outputs from the SRAM cell, while presenting minimal additional load to the SRAM cell. The output terminals are pulled to Vdd when the sense amplifiers are idle. The sense enable signal turns M9 on, which turns the transistors M5 and M6 on. The charging speed at the output will be different due to the difference in the input voltages which causes both the outputs to differ. Now the strong positive feedback enhances the voltage difference and the latching is complete when either M1 or M3 is cut off. Fig. 5 shows the transient behavior of the circuit explained above.

The offset voltage of a sense amplifier is defined as the minimum differential input voltage required in order for the sense amplifier to be activated in the right direction. Hence, it is important that the sense enable signal is given to the circuit only after the offset voltage has been exceeded at the inputs.

An important aspect of this design is the ability to control when the sense amplifiers fire. If they fire too early, the memory cells do not have enough time to charge the bit lines to levels that can be confidently detected. At the same time, waiting too long degrades the overall performance of the circuit. A delay of 200 ps was chosen because it was the smallest physically achievable delay that allowed for sufficient bit line charge.

This design provides the user with a signal indicating the validity of the data inputs to the sense amplifier. More specifically, if both inputs transition high or low in the same read operation the data is considered invalid. The main sense amp design was leveraged to achieve this fault detection due to its high performance. Each bit-line is compared with its precharge voltage, and the output of these comparisons is XOR'ed to provide the data valid signal.

The classic 6T SRAM cell model, presented in Fig. 3, has been used to analyze this sense amplifier design. A lumped RC element was connected to represent the bit line load, which consists of the wire and the drain impedances of other cells (a 512 word cell was modeled). Values for these impedances are based on the memory model presented in [3]. The SRAM cell has been broken into two mirror circuits to exercise the fault detection features of this project. Finally, bit lines are precharged to 1.15 V, which is a compromise between differential voltage swing and process sensitivity. Higher precharge voltage improves differential voltage swing but degrades process sensitivity. An ideal voltage source with a PMOS pass-transistor is used to model the precharge circuitry.

A typical bit width is 4um which allows for a maximum sense amp width of 8um. This allows two parallel or offset rows of sense amps to fit well into the overall floorplan. Fig. 7 is an example floorplan using parallel sense amps. This design will be used in a digital application, hence overall area and regularity of the layout is a concern. The layout of the sense amplifier shown in the Fig. 1 successfully addresses these issues.

Challenges

One of the main challenges in designing the sense amplifier was the required noise immunity. Noise comes primarily from capacitive coupling and the intrinsic offset voltage of the sense amplifier, and can trigger false results at the sense amplifier outputs. This was addressed by delaying the *sense_en* (enable) signal with respect to the *read_en* (enable) signal until the voltage across the differential bit lines becomes larger than the capacitive cross-talk noise on the sense amplifier inputs. [2] indicates that 30 mV is a standard noise level.

Device mismatch was another major challenge. Monte Carlo analysis allowed for analysis of process variation on the sense amplifier circuit. Since the circuit topology is based on a differential pair, it becomes all the more important to have good device matching across the symmetric plane of the circuit in order to have predictable performance (e.g: noise immunity, sensing delay). Two key strategies which we used to minimize process sensitivity (i.e: offset voltage) of our circuit were transistor upsizing and lowering the input DC level, thereby lowering the bias currents. This strategy is discussed further in [1].

Speed of operation was also an important performance metric, which was maximized through transistor sizing techniques, specifically by increasing the bias currents by increasing the width of M9. This presents a design tradeoff between process sensitivity and operational speed.

Results

Fig. 5 displays the transient simulation results from this design. The worst case delay is 575 ps from the *read_en* to the *isValid* output. All other outputs have approximately equal delay, which is 475 ps. Table 1 has the pertinent timing and voltage specs in it. These timing values compare well with industry standards. Today's computer memory operates at clock speeds around 400 MHz, which translates to a total delay of 2.5 ns. With this sense amp the actual memory read completes in approximately 20% of this time, which leaves 80% of the read latency for the necessary decoding and I/O conditioning. Further work will include studies on larger memory arrays.

Initially, we thought we could achieve even lower delays with our circuitry, but we did not fully understand the effects of transistor parasitics on timing delays. Without the inclusion of parasitics, this circuitry operates approximately twice as fast.

A Monte Carlo analysis of our design indicates that to achieve 6σ yield, the inputs must exceed a differential of 40mV, because a worst case offset voltage of 40mV is expected. This offset voltage is extremely small, especially considering the system noise, so this design was successful. Through careful timing design we ensured that this was met. The worst case differential input to a sense amp is 50mV, shown in Fig. 6.

References

[1] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier," IEEE J. Solid-State Circuits, vol. 39, pp. 1148-1158, Jul., 2004.

[2] S. Hong, S. Kim., J-K. Wee., et al., "Low-Voltage DRAM Sensing Scheme with Offset-Cancellation Sense Amplifier," IEEE J. Solid-State Circuits, vol. 37, pp. 1356-1360, Oct., 2002.

[3] J. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits: A Design Perspective," Pearson Education, ed. 2, 2003.

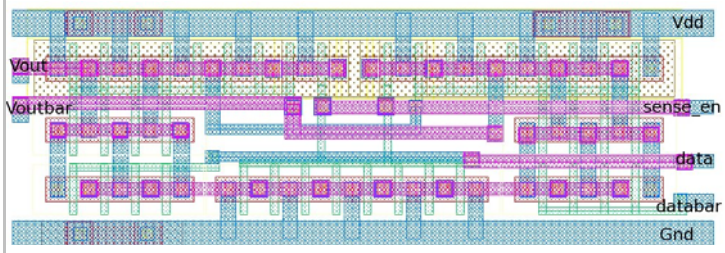

Figure 1 Layout of the sense amplifier

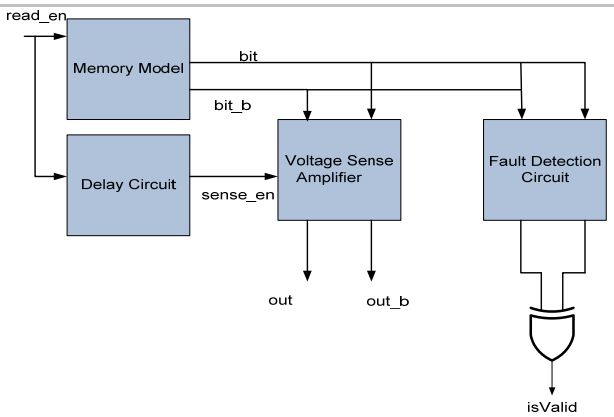

Figure 2 Block Diagram of the design

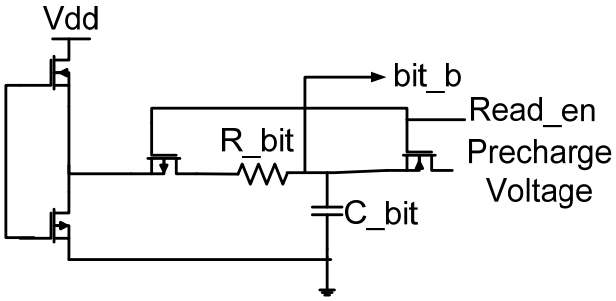

Figure 3 Schematic of the memory model

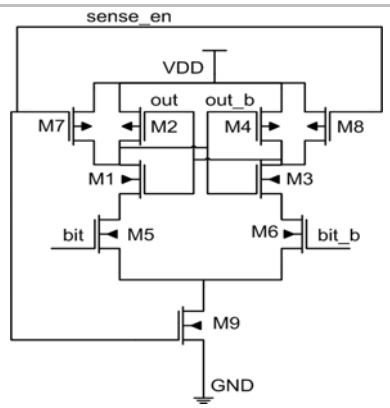

Figure 4 Schematic of the sense amplifier

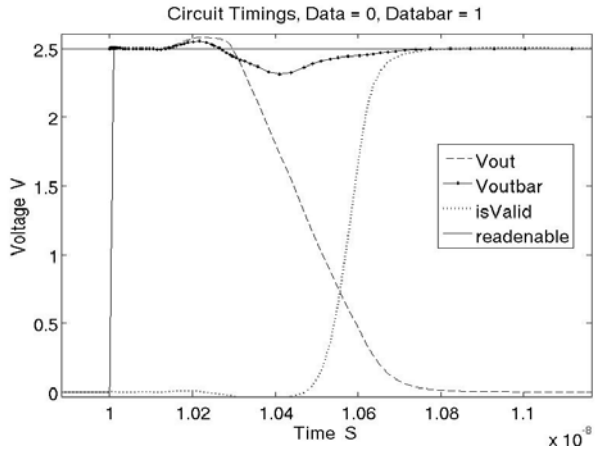

Figure 5 Transient response of the sense amplifier

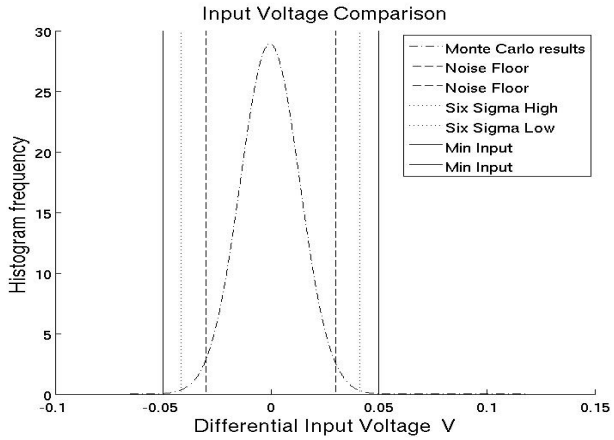

Figure 6 Monte Carlo Results and critical voltage comparison

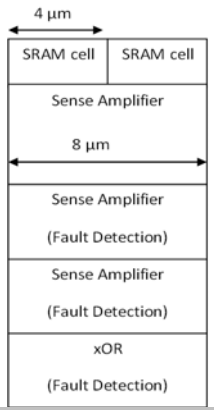

Figure 7 Layout Floor Plan

Characteristics	Simulated Results
Read enable- sense enable delay	200 ps
Read enable- fault detection delay	575 ps
Read enable- data output delay	475ps
XOR delay	100 ps
Sense amplifier differential Input	250 mV
Fault detection differential Input	50 mV
Noise Floor	30 mV
6σ offset voltage	±40 mV

Table 1 Results Summary