

# CAD Pitfalls

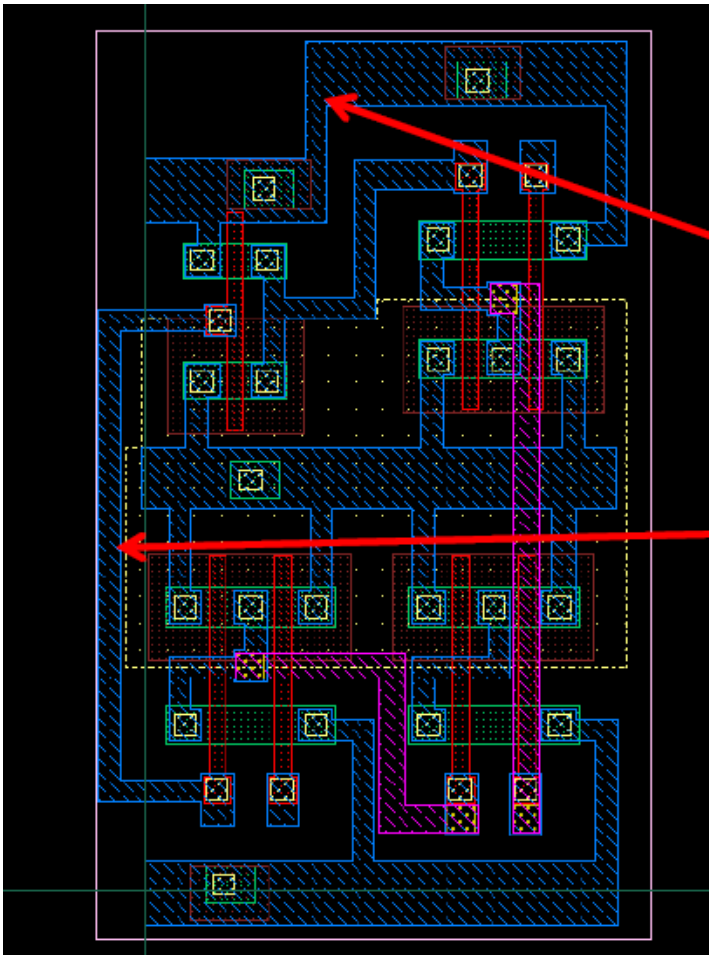
Bhavi, your friendly grader

# A few quick points

- CAD2 due on coming Monday(21<sup>st</sup> Sept).
- To help with the following CADs, we have some illustrations of some common pitfalls.
- Some may be completely unaware of these points for layout. So we may not deduct any points in CAD1 but make sure you take care of these issues from CAD2 onwards.
- Do mention which cell views to grade in your readme !(INV, INV2, INV3,INV\_back,INV\_backup,INV\_final,.....)
- M2,M4 and M6 are vertical while M3 and M5 are horizontal.

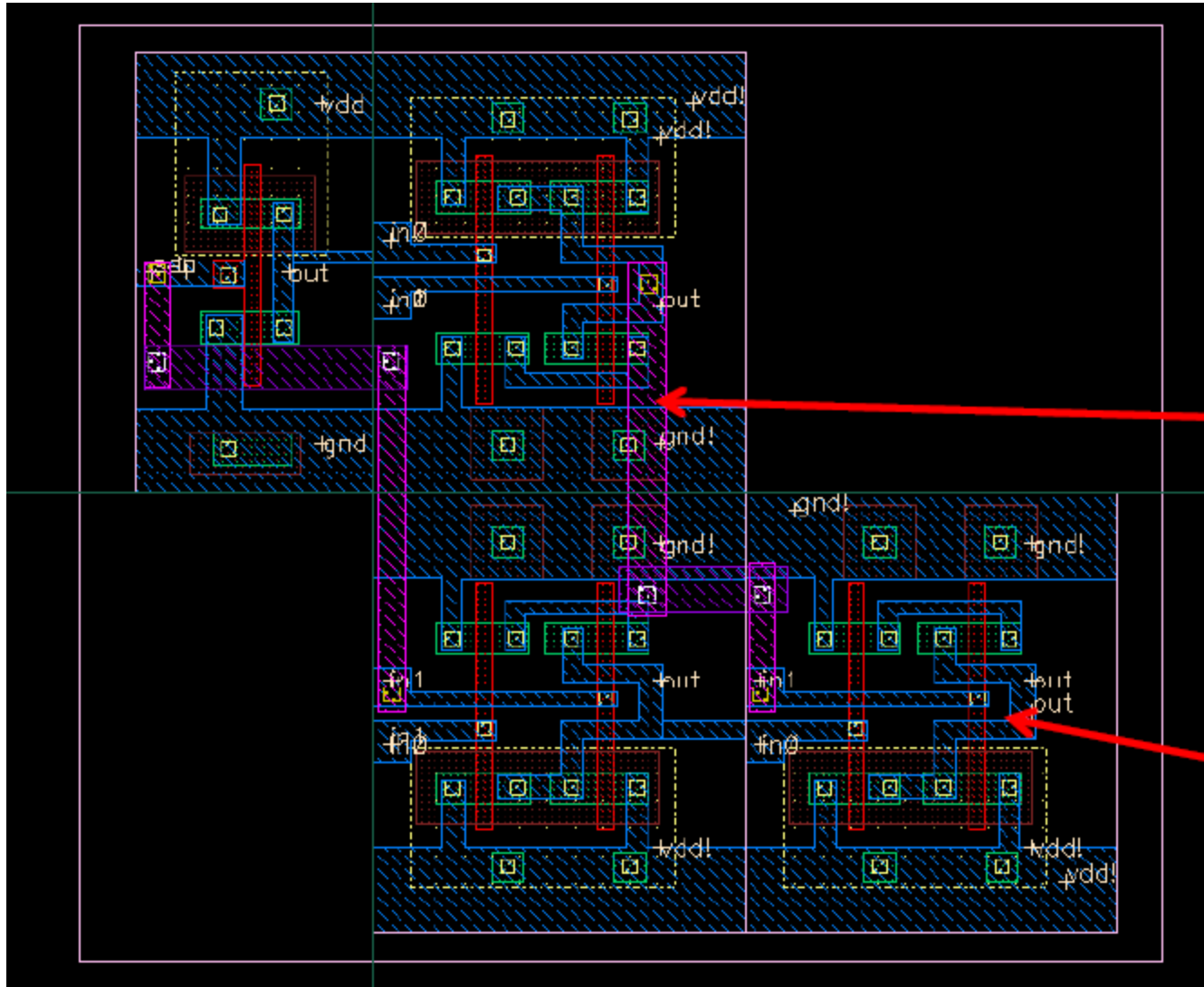


# Cell height mismatch/Outside Routing



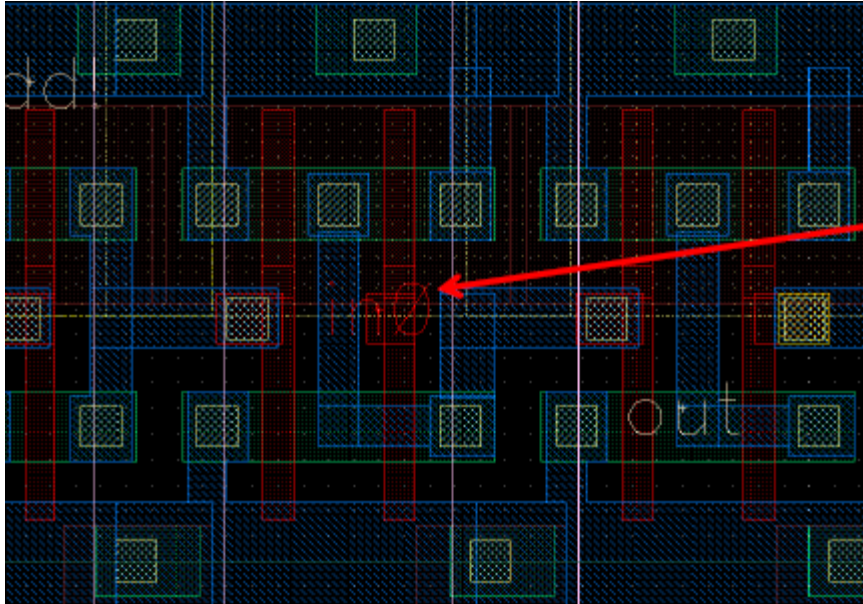
- GND and VDD planes should be matched
- Avoid external M1 routing.
- In case you want to connect VDD and GND, use names to connect (in LVS).

# Metal widths



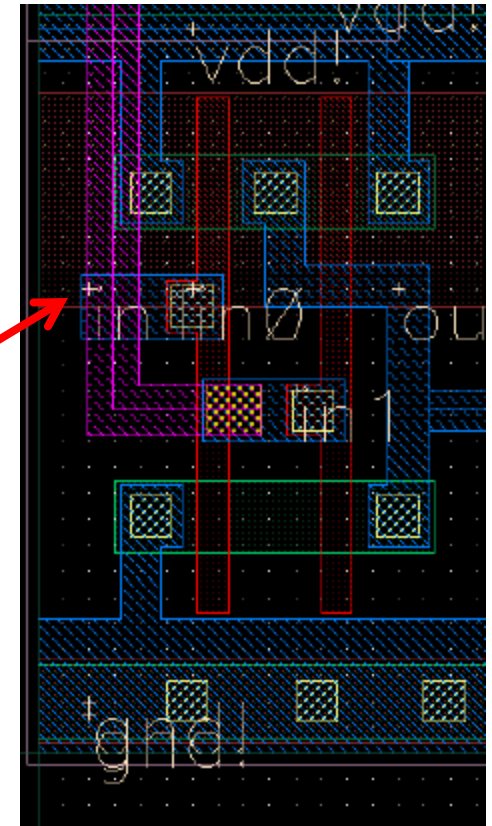
- Keep minimum (except VDD & GND)
- Twist n turn and experiment

# Routing and labeling pins

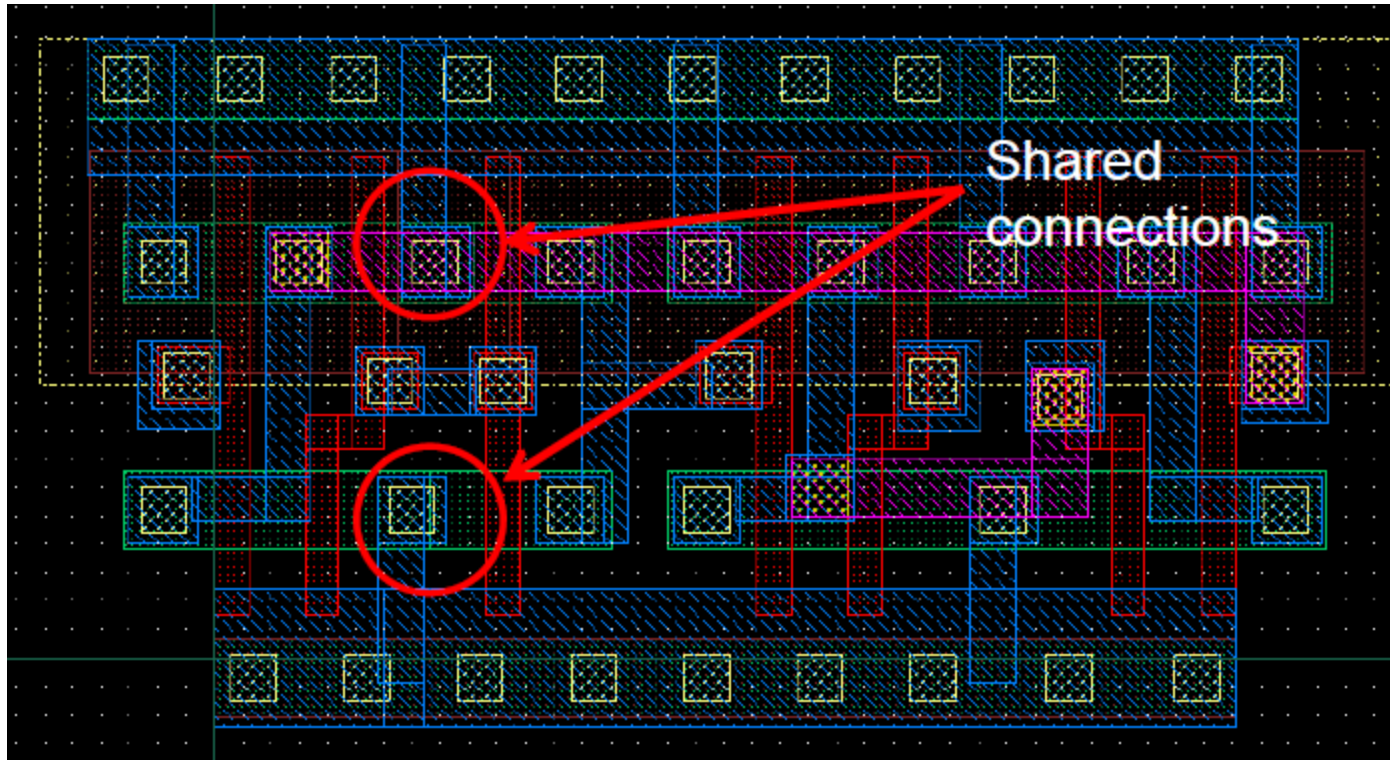


- No pins on the poly, as you cannot route it out directly.

- Pin labeled on M1 but lies below M2
- Always place labels on the grid.
- Keep at least the space of one VIA around the 'landing spot' without the need to add additional metal

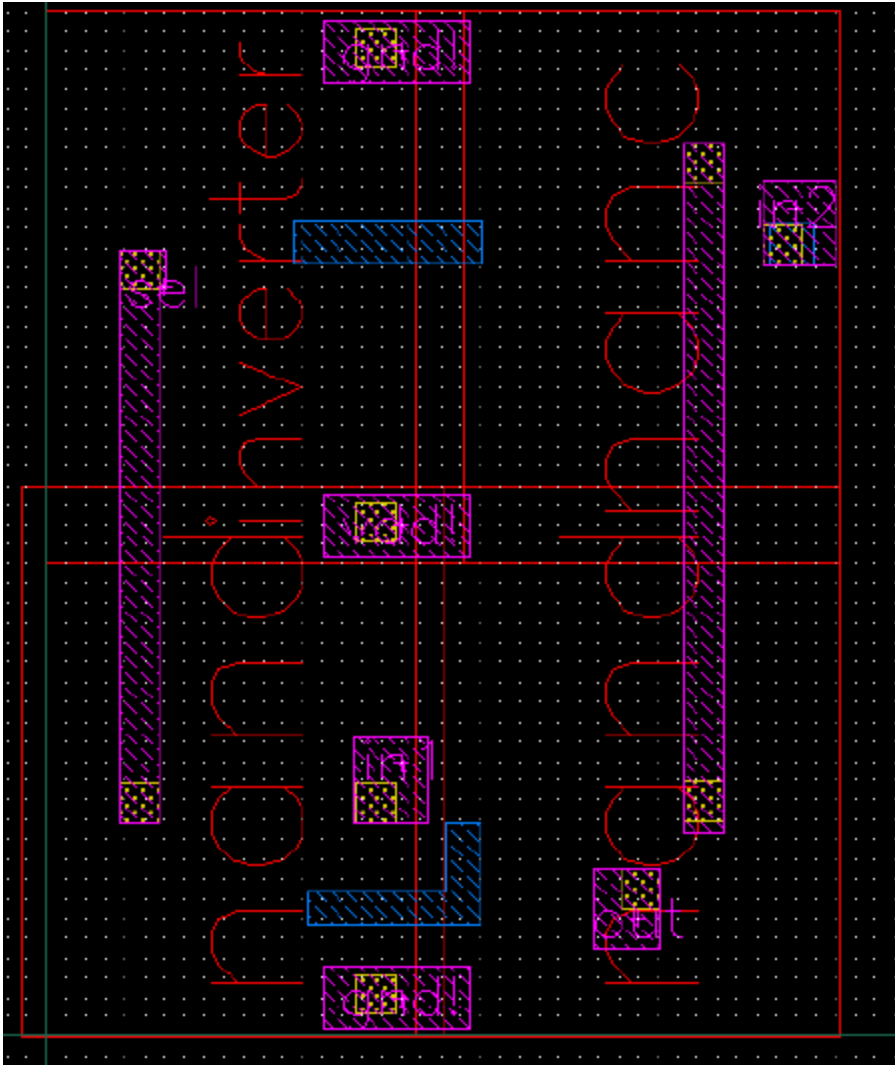


# Share and merge active areas



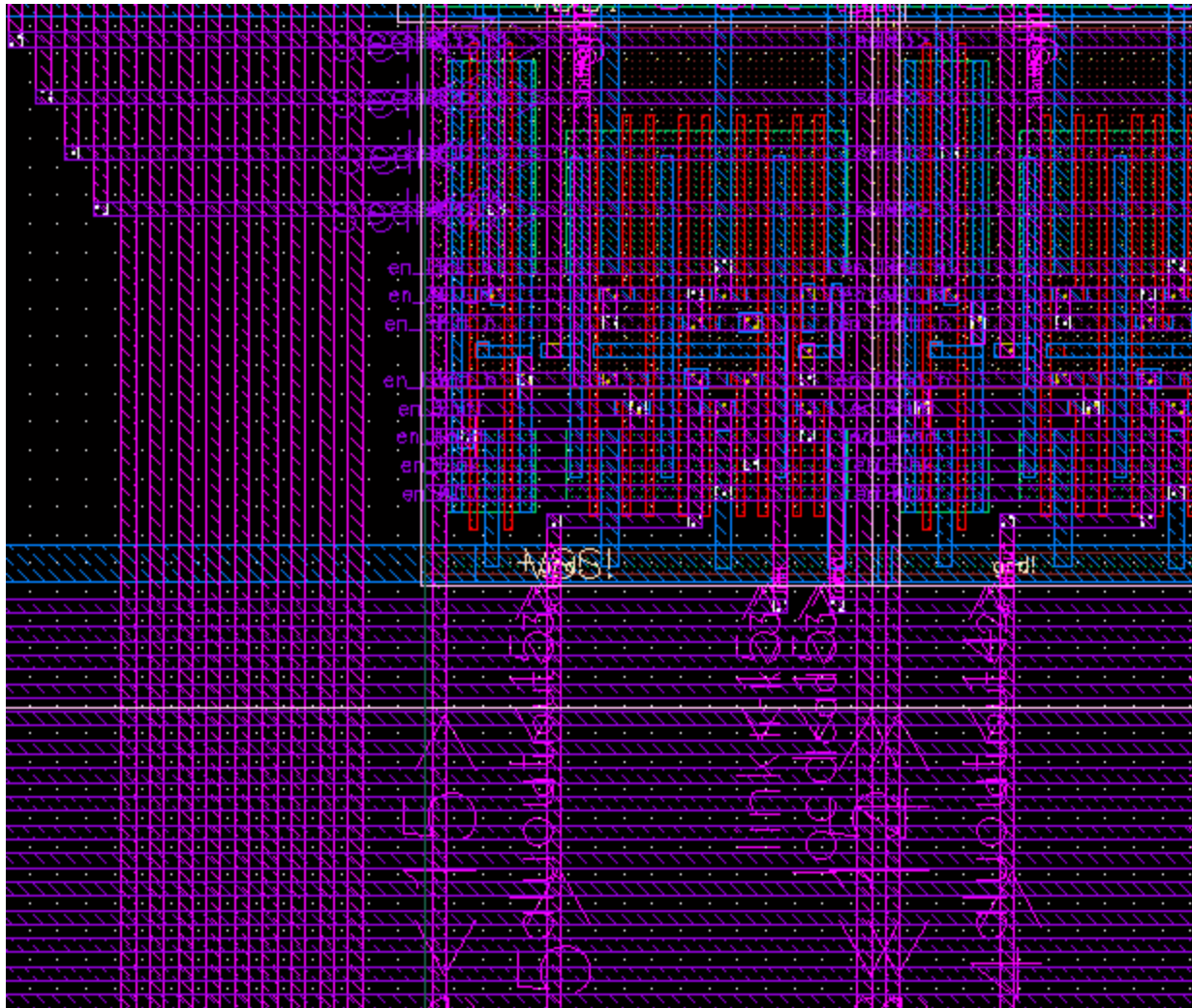
- A nand(leftmost) and inverter have been merged to have a common GND and VDD.
- Merge as many active areas as possible(may even jog poly) to get the maximum density.

# Good hierarchy => Easy life



- As the CAD gets more and more complex, a good hierarchy will save you the clutter later.
- Will also help in DRC and LVS error debug.

# Plan your Tracks and Grid usage



# Thanks for listening

- EECS 427 will become an integral part of your life in the coming days. So best of luck everyone.