

EECS 427 F09

Discussion 1

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2009/09/15

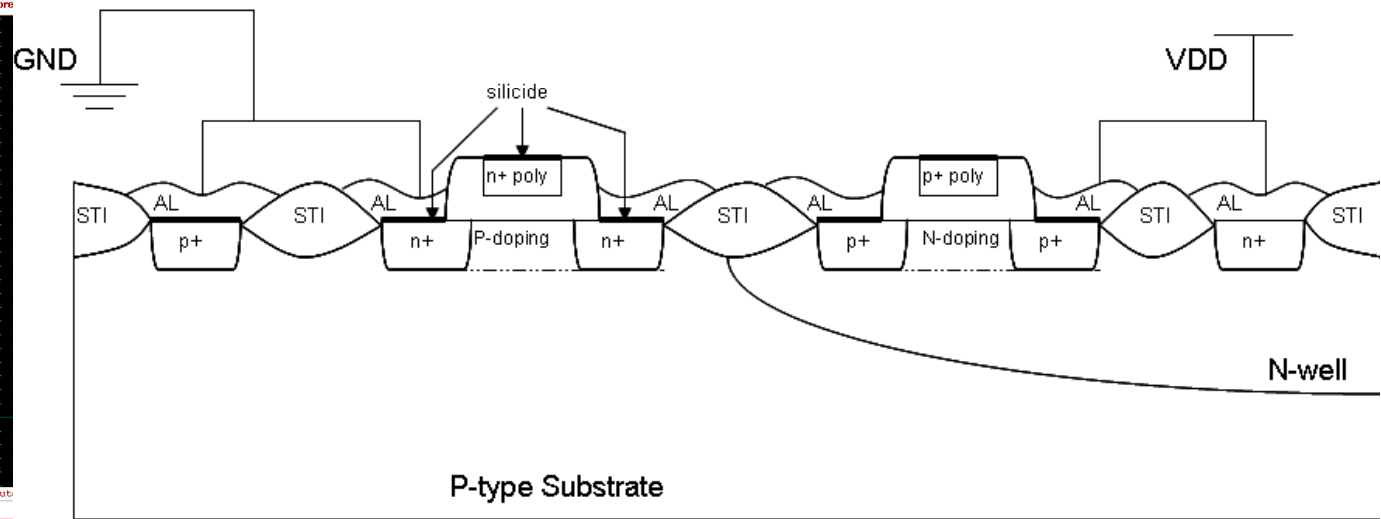
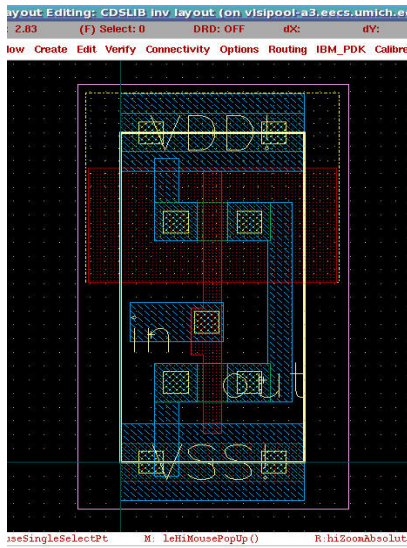
Announcement

- Office hour change:
 - Monday 4:30 – 6:30 pm
 - Tuesday 6:30 – 7:30 pm
 - Thursday 4:00 – 6:00 pm
- CAD2 / Tutorial 1.5 are online
- CAD1 due tomorrow

Today

- Cross section view for an inverter
- Routing Grid
- Tutorial 1.5 and CAD2

Cross section view for an inverter



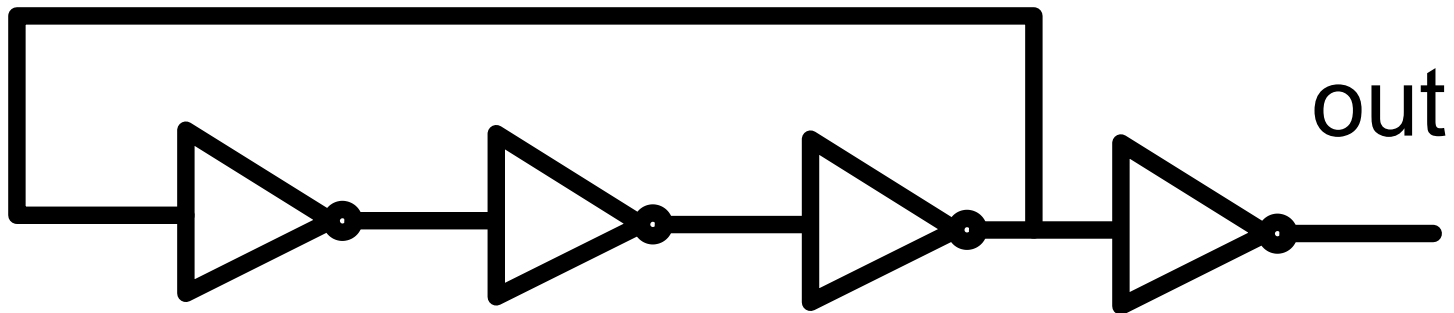
<http://www.eeinterview.com/>

Metal Usage

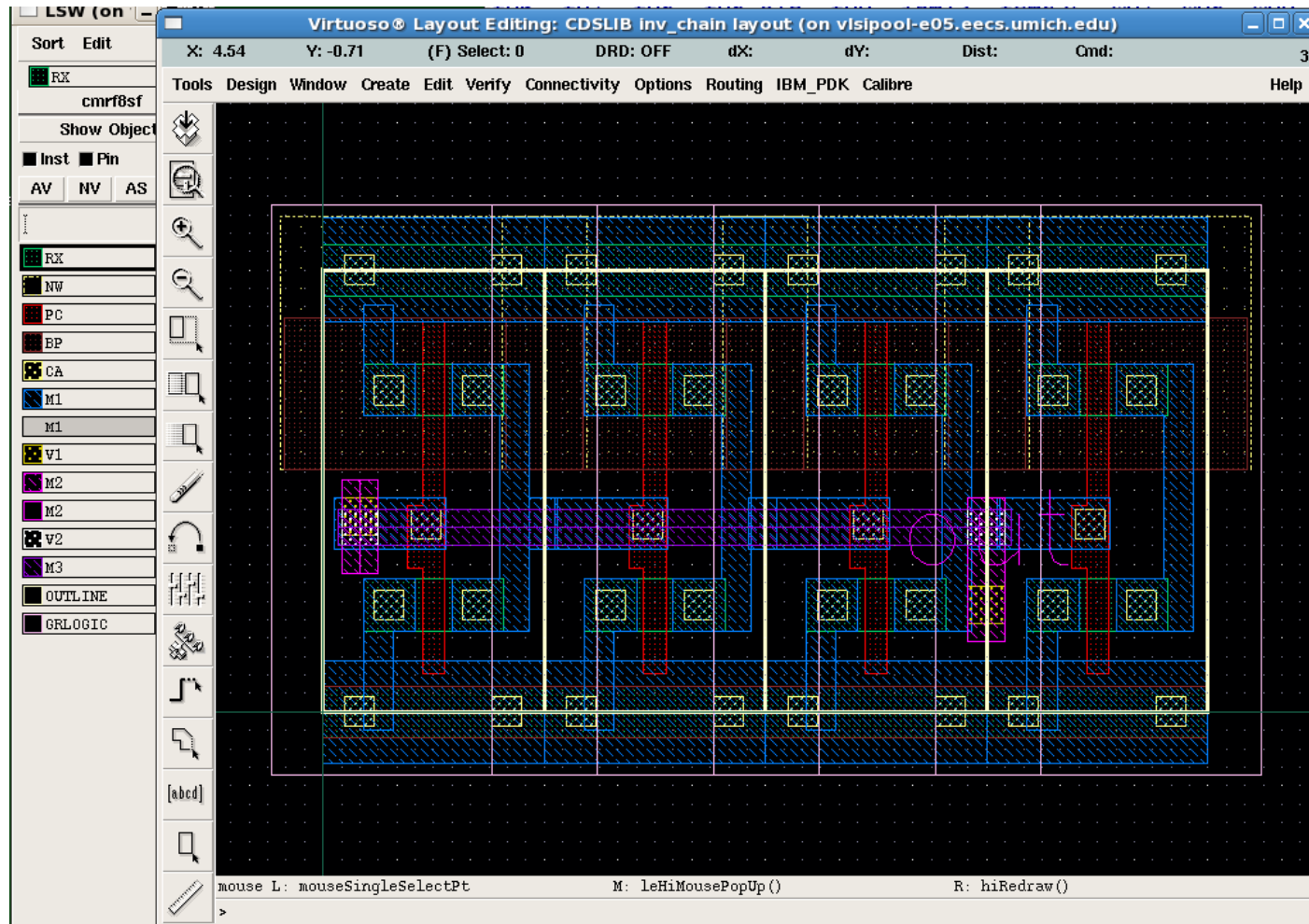
- Connection
 - Inside the cell:
 - PC and M1, M1 is preferred, since R is smaller
 - Connections between cells and cells
 - Vertical connection M2, M4, M6
 - Horizontal connection M3, M5
 - Virtual routing tracks
 - In design rules, Metal and Metal space is 0.2um, Metal minimum width is 0.2um.
 - 0.4um per track

Example(inverter chain)

- Schematic
 - inverter chain

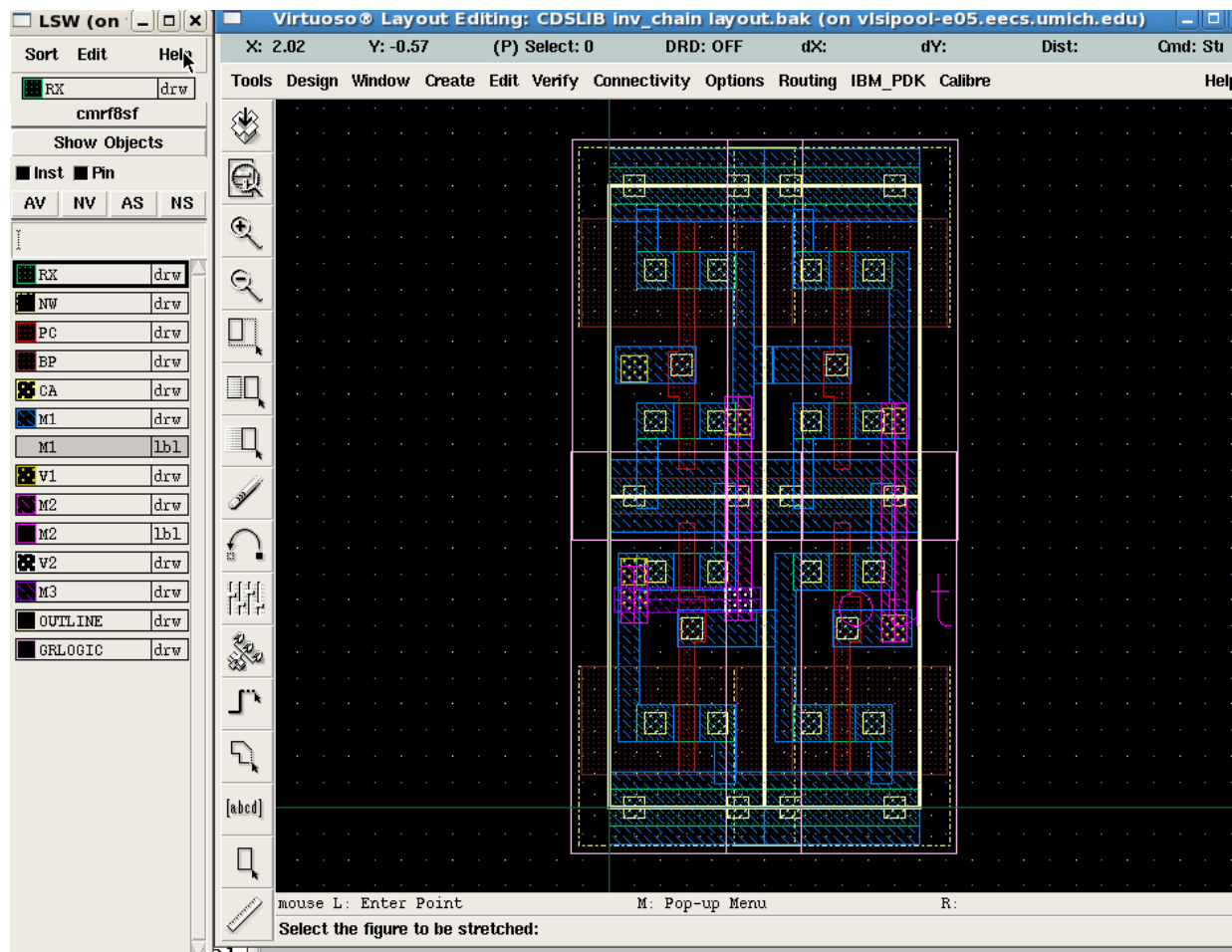


Example(inverter chain)



- AV, NV, AS, NS, minor grid

Example(inverter chain)



- Rotate, Flip, origin, virtual connect

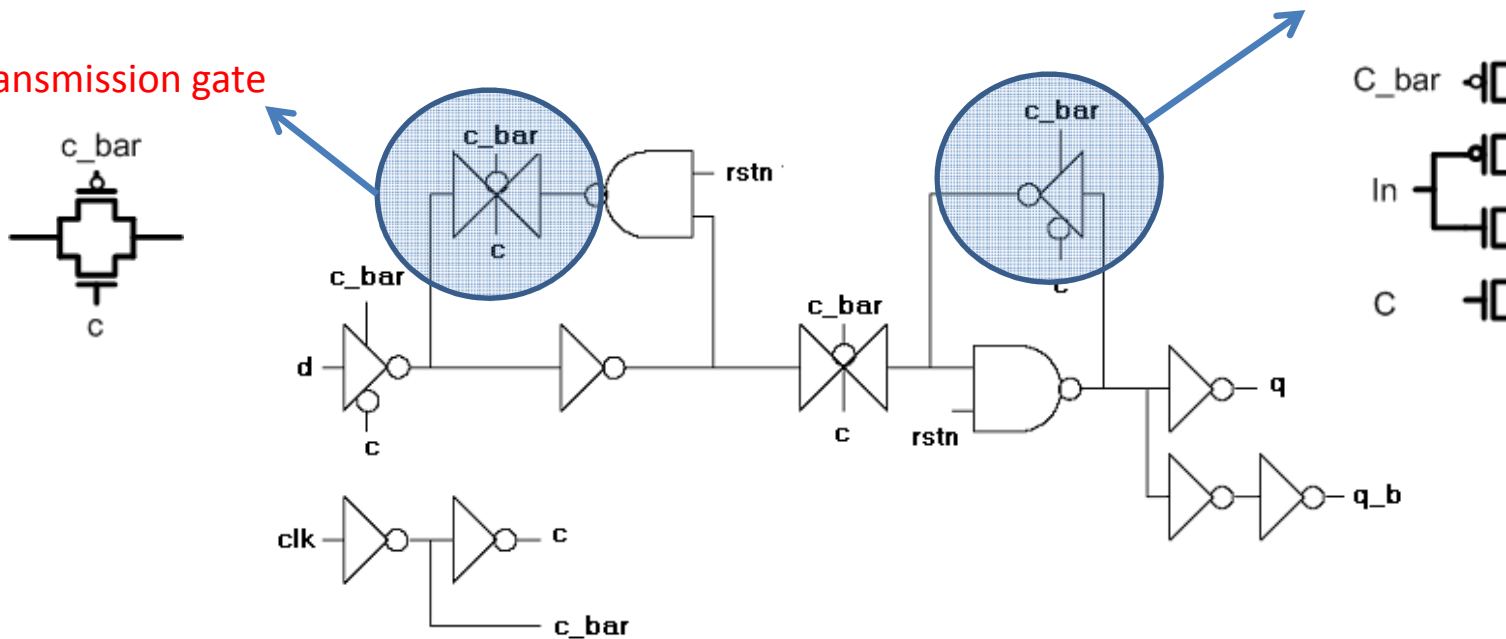
1-bit register (flip-flop)

- Schematic

- Clk= clock, d = input, rstn = reset
- Asynchronous reset: as reset goes low, q is set to 0 (this example)
- Synchronous reset: when clk goes high, it will check if reset is low, if it is, then set q to 0.
- Asynchronous v.s. Synchronous = reset triggered v.s. clk triggered

Tri-state buffer

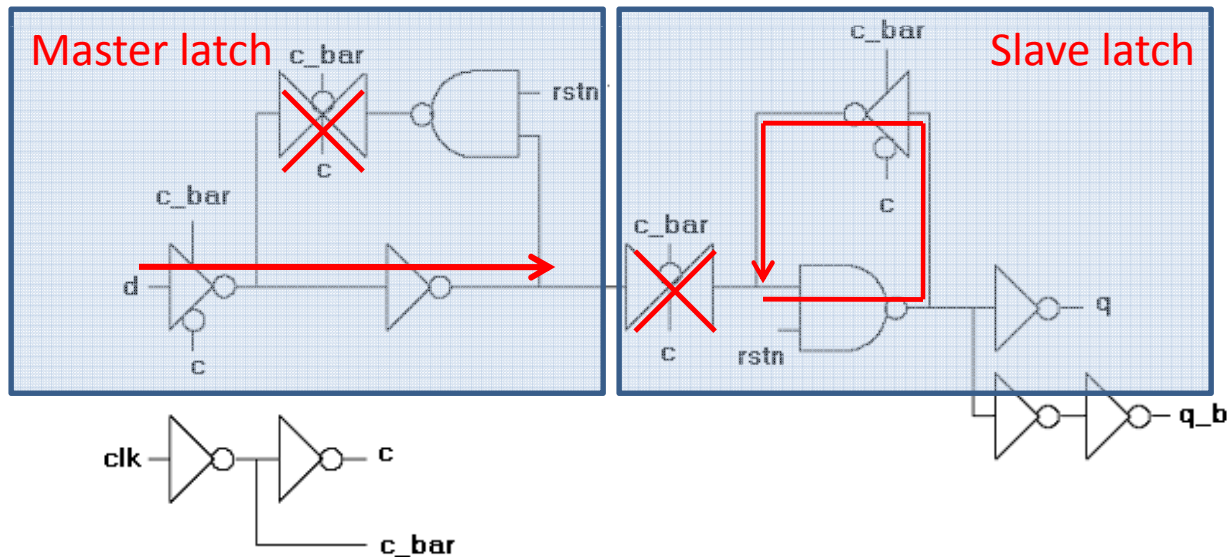
Transmission gate



Register (continue)

- How it works

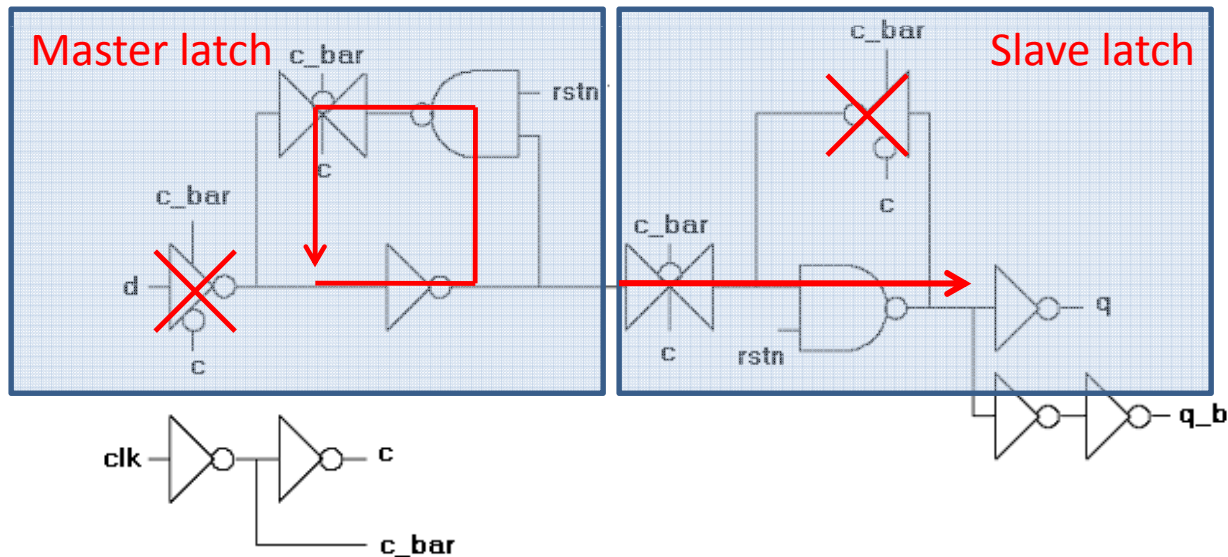
When C is equal to 0, the master latch is transparent, and the slave latch is closed.



Register (continue)

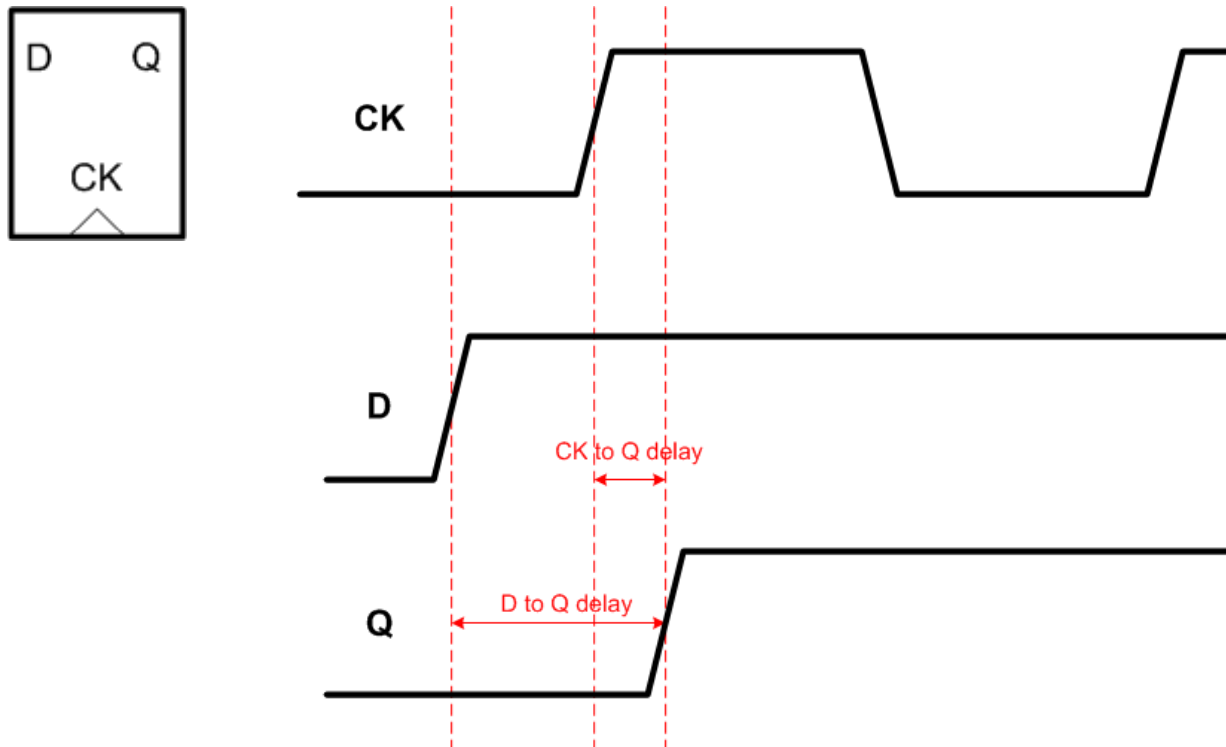
- How it works

When C is equal to 1, the master latch is closed, and the slave latch is transparent
When C switches from 0->1 (rising edge of the clock) the register captures the data .



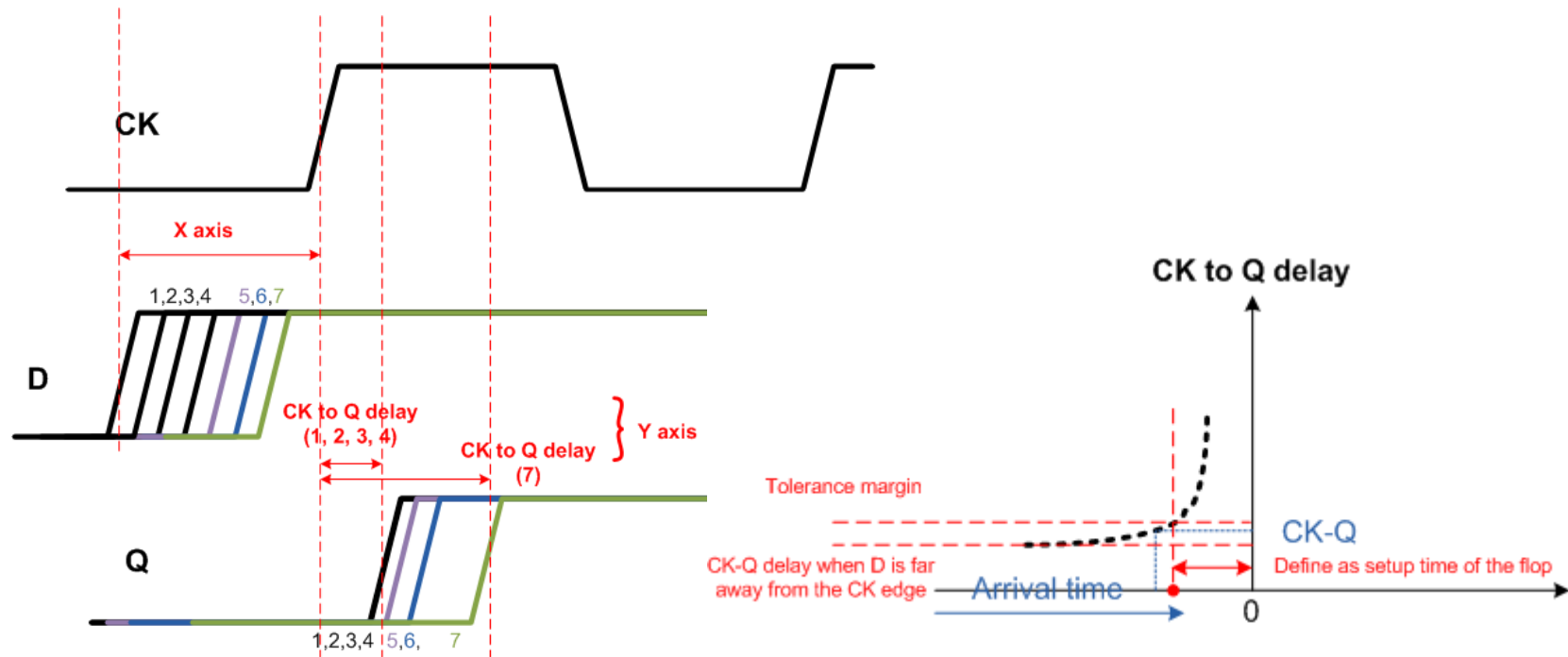
Register (continue)

- Important terms, (C-Q delay, D-Q delay)



Register (continue)

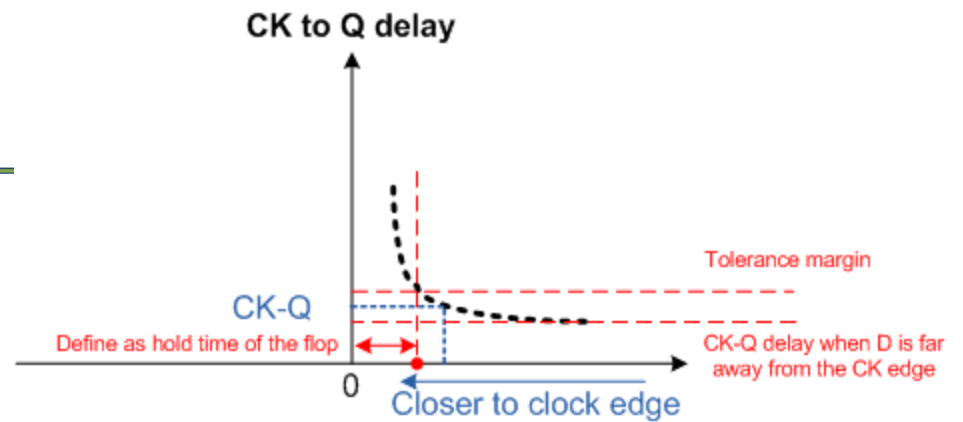
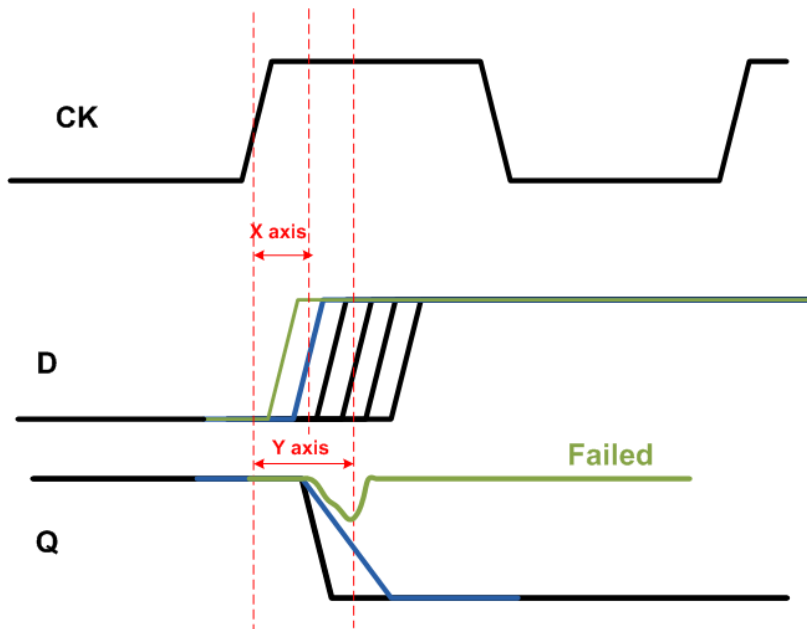
- Setup Time
- As D approaches to CK edge, C-Q delay goes up



When D arrives after the setup time point, we call it setup time violation

Register (continue)

- Hold Time
- Input should be stable for a period of time after the clk edge



What do u need to notice in CAD2

1.Weak transistor (tutorial 1.5)

You need to use weak transistors (rpfet, rnfet) on the feedback path. In this example, using weak transistor on the transmission gate of the master latch, and the tri-state buffer of the slave latch.

2.Transmission gate direction (tutorial 1.5)

Remember the arrow of the transistor symbol means the direction of the current flow (see page 2 of tutorial 1.5)

3.Adding delay to the transistor in Verilog simulation (tutorial 1.5)

Adding setup time in the first tri-state buffer

Adding ck-q delay at the output buffer

4.Measure the setup time/ hold time (tutorial 1.5)

Sweep the arrival time of the input, and set the margin to 5%, measuring the setup time and hold time
(The delay is measured between the 50% of amplitude of the signals)

Short key for Virtuoso

Adding geometries

Rectangle: r

Path: p

Label: l

Modifying geometries

Copy: c

Move: m (whole shape only)

Stretch: s (whole shape or edge)

Chop: shift + c

Merge: shift + m

Ruler

Create ruler: k

Delete all ruler: shift + k

Rotating and Flipping

After selecting copy , move, create instance, etc., HIT F3!

Hierarchy Edit

Descend edit: x

Return: b

Show all hierarchy: shift + f

Hide all hierarchy: ctrl + f

Create Instance: l

Other useful commands

Properties: q

Search: shift + s

Select all: ctrl + a

Deselect all: ctrl + d

Toggle on and off gravity: g

Redraw : ctrl + r

LSW

You can set the LSW to show only the layers that are in your layouts

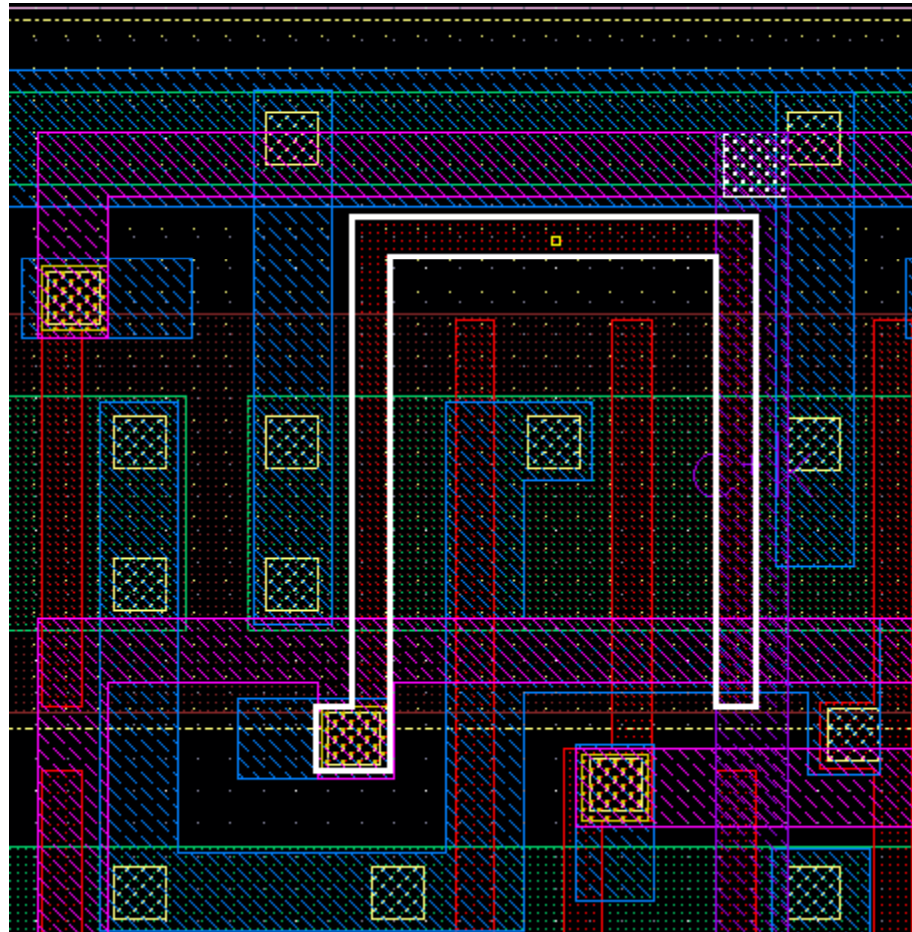
[In Virtuoso Window] IBM_PDK->LSW->Present Layers Only

To add more layers that are not in the LSW

[In LSW Window] Edit->Set Valid Layers

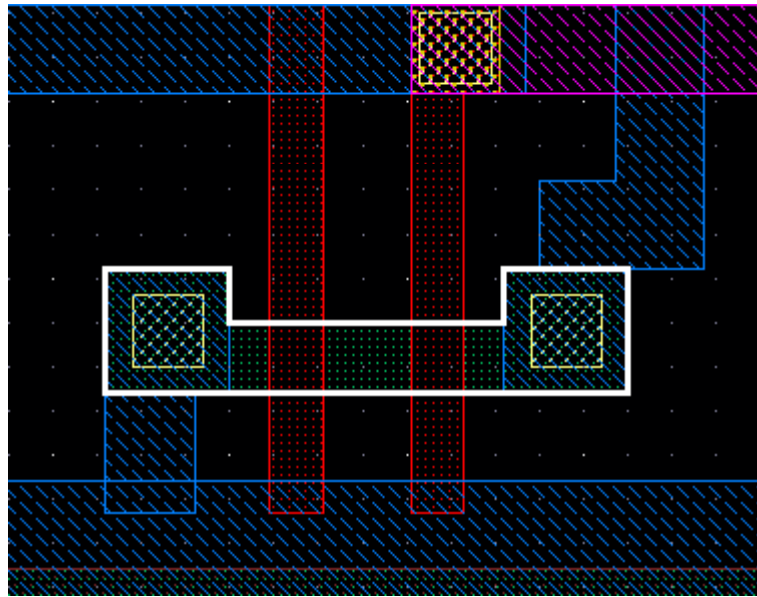
Layout Quality

- Avoid long PC connection



Layout Quality

- Avoid dumbbell shape RX



Q?