EECS 427 F09
Discussion 2

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Announcement

- CAD3 is on line (group project)
- Only 3 Groups for now

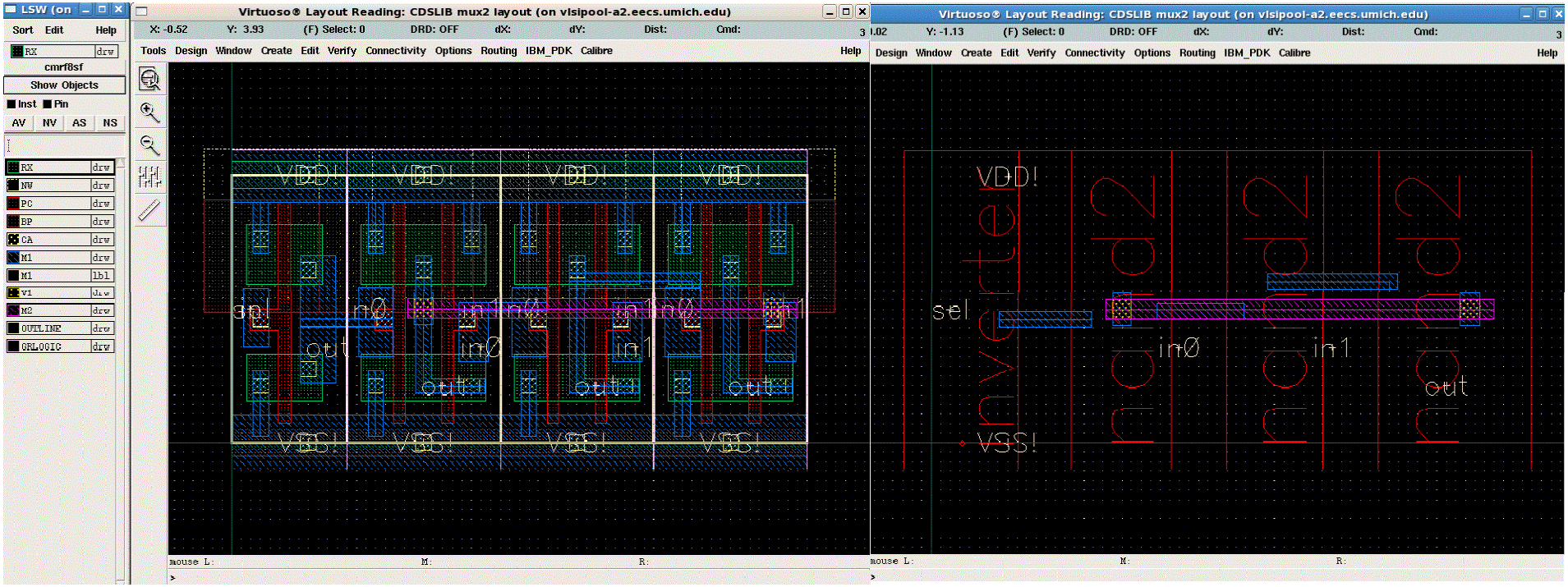
Today

- CAD1, CAD2
- CAD3 and more
  - Learn Design hierarchy in CAD1
  - Lean 1 bit register file in CAD2
  - You are going to make a 16x16 RF in CAD3

CAD1

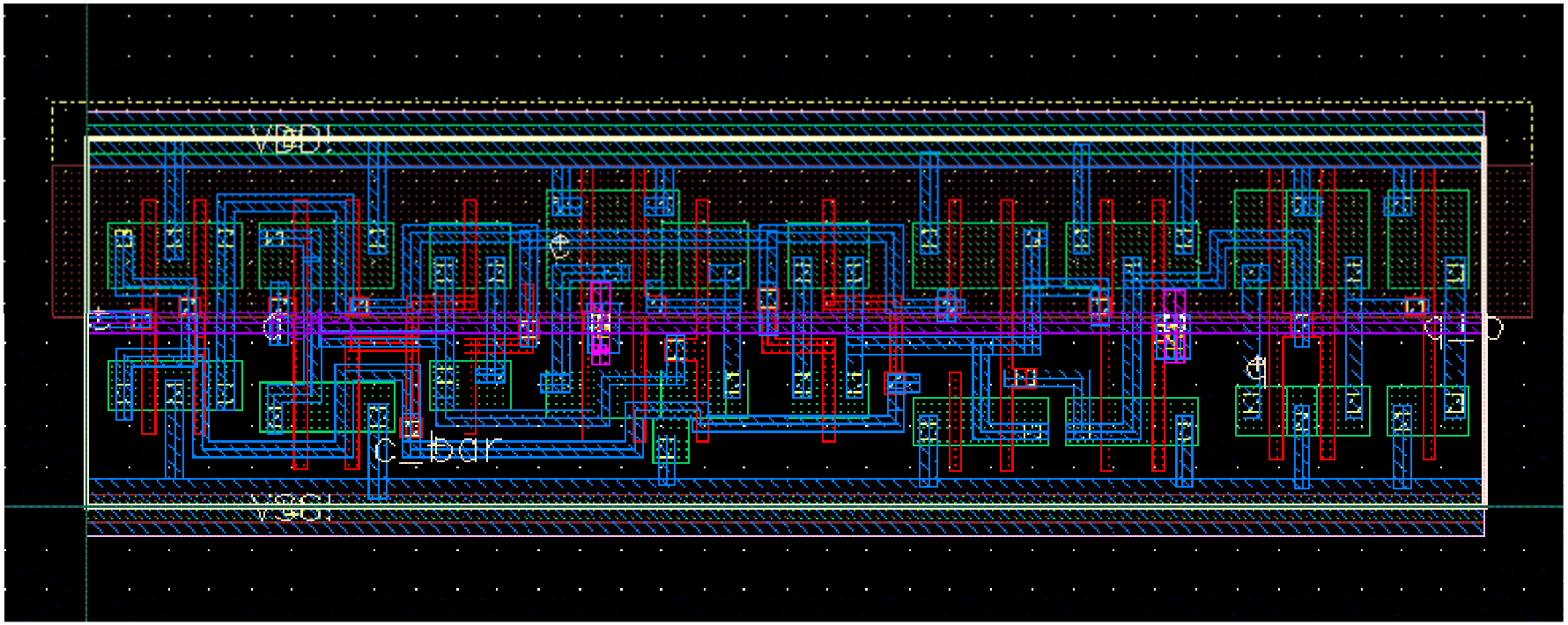
- Using Poly to actually route signals over two cells instead of metal.
- It seems that some(actually few) tried to access their CADS later and their time stamp has changed.
- M2 routed vertically and horizontally.

GSI’ CAD1



- Hierarchical Design
- Use M2/M3 tracks efficiently
- Only connections and labels are in this level

GSI’ CAD2

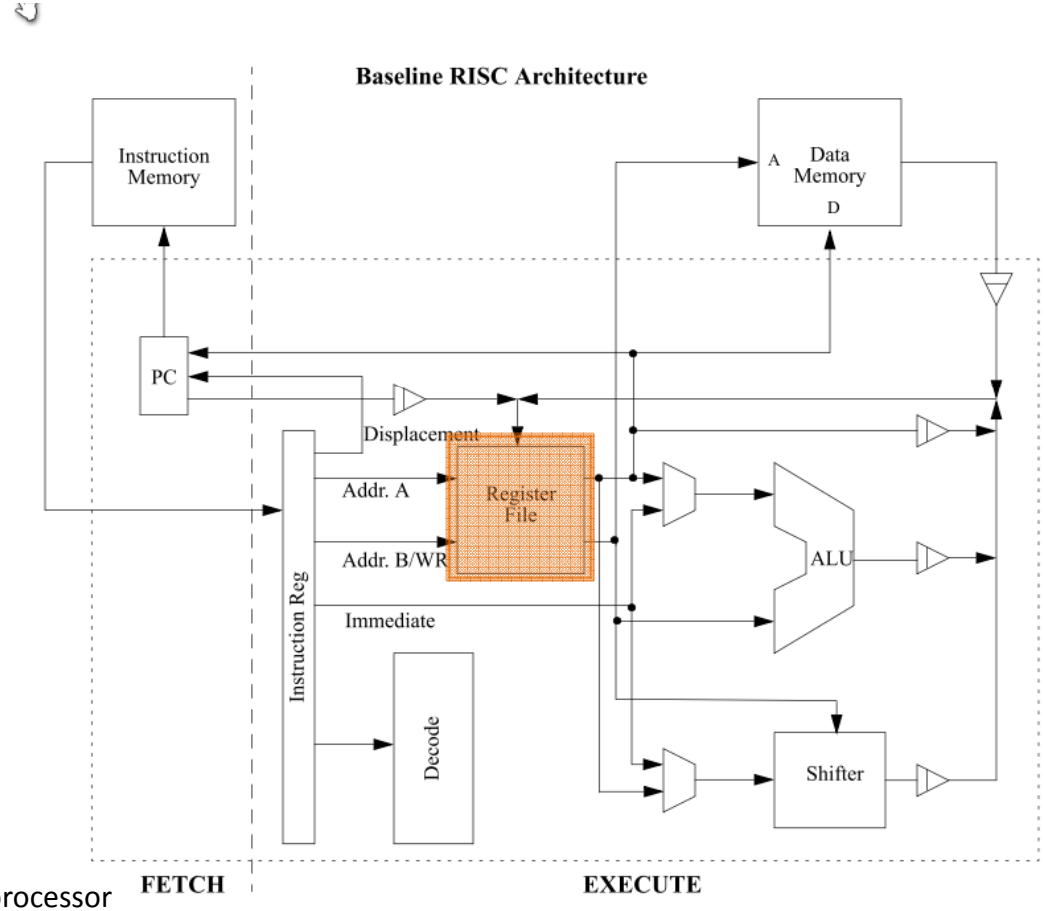


- Minimize the area
- Use M2/M3 tracks efficiently

Sizing Transmission Gate

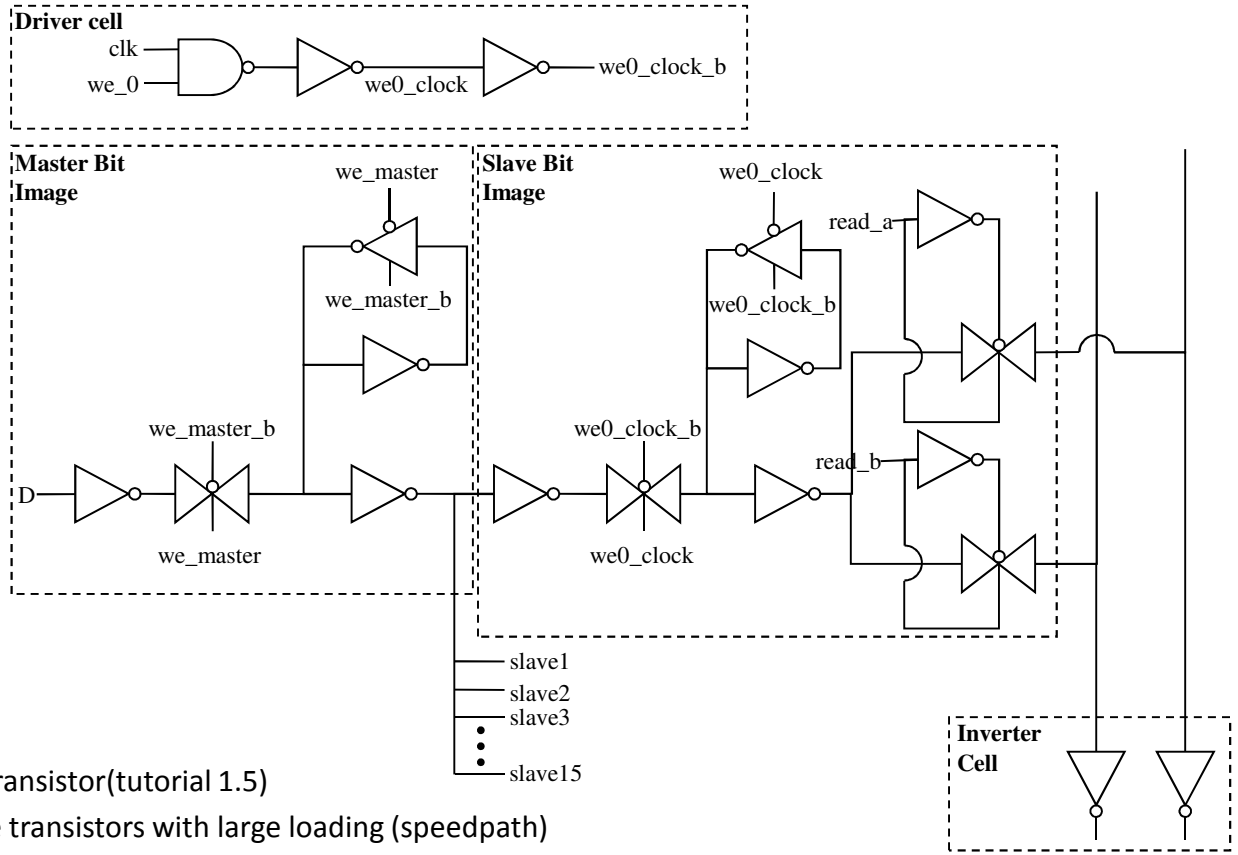
- Inverter:
  - Send 0 using nmos
  - Send 1 using pmos
- Transmission gate
  - Send 0 using both
  - Send 1 using both
  - Why do you need both nmos and pmos?

Baseline RISC Architecture



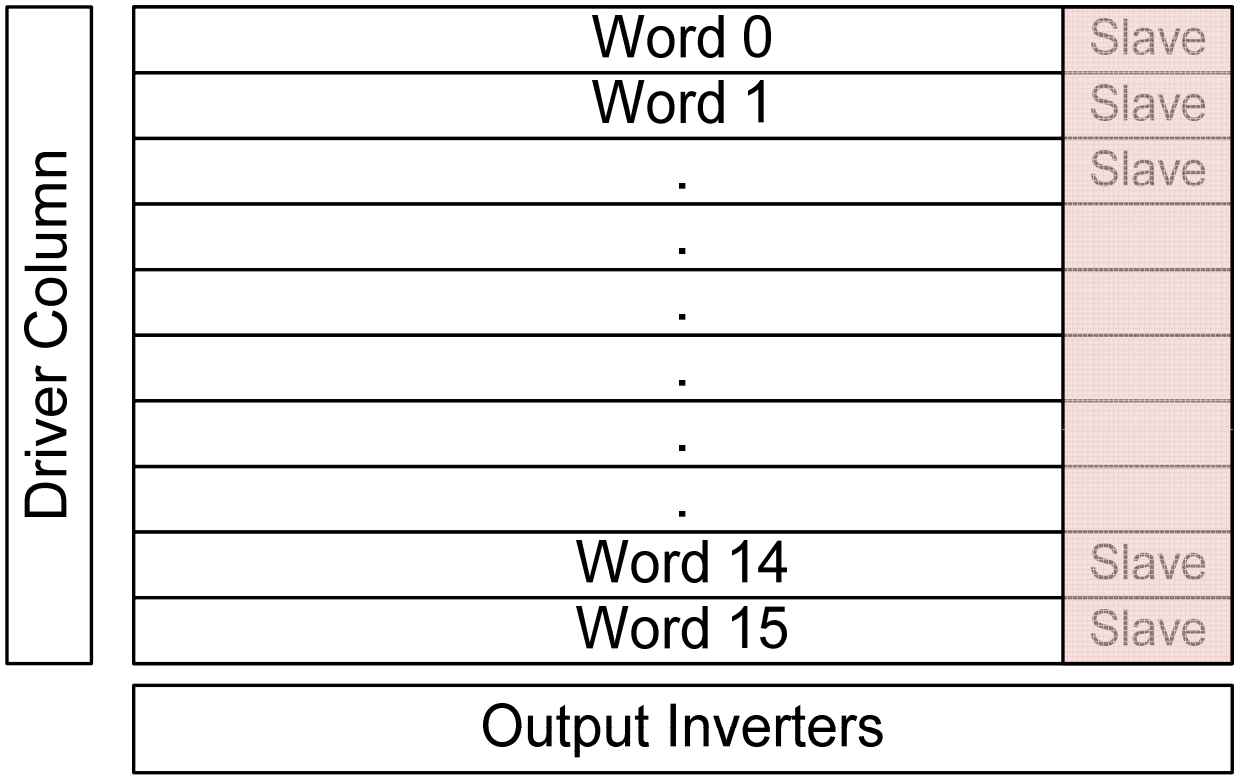
- 16 bit RISC processor
- Two stage pipeline (Fetch/WB and Execute)
- Baseline ISA

RF (16 bits)



- Tips:
  - Weak transistor(tutorial 1.5)
  - Size the transistors with large loading (speedpath)
  - Reset is not require, but you need a way to reset the RF
  - Which phase should we_0 be in ?? (this is important when you design your controller)
  - Inout instead of output
  - Even better, need keepers at floating nodes

RF (16 x 16 bits)

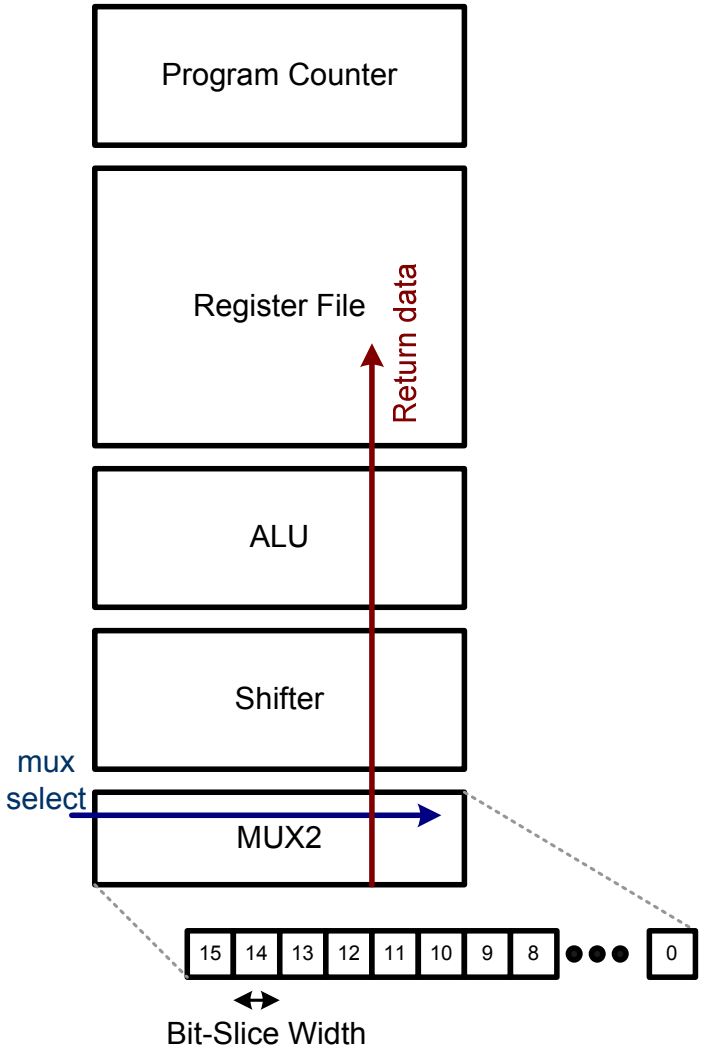


- Tips:
  - Bus notation
  - Input direction (top or bottom), where to place master latch?
  - Bit width (layout density and quality)
  - M1 – M3 are allowed
  - Even better, Power grid, Clock buffers?

Effect of the Bit-Slice Width

- A row of mux2's in the pipeline
- Large bit-slice width → long select line (blue wire)
- Small bit-slice width → long data line (red wire)

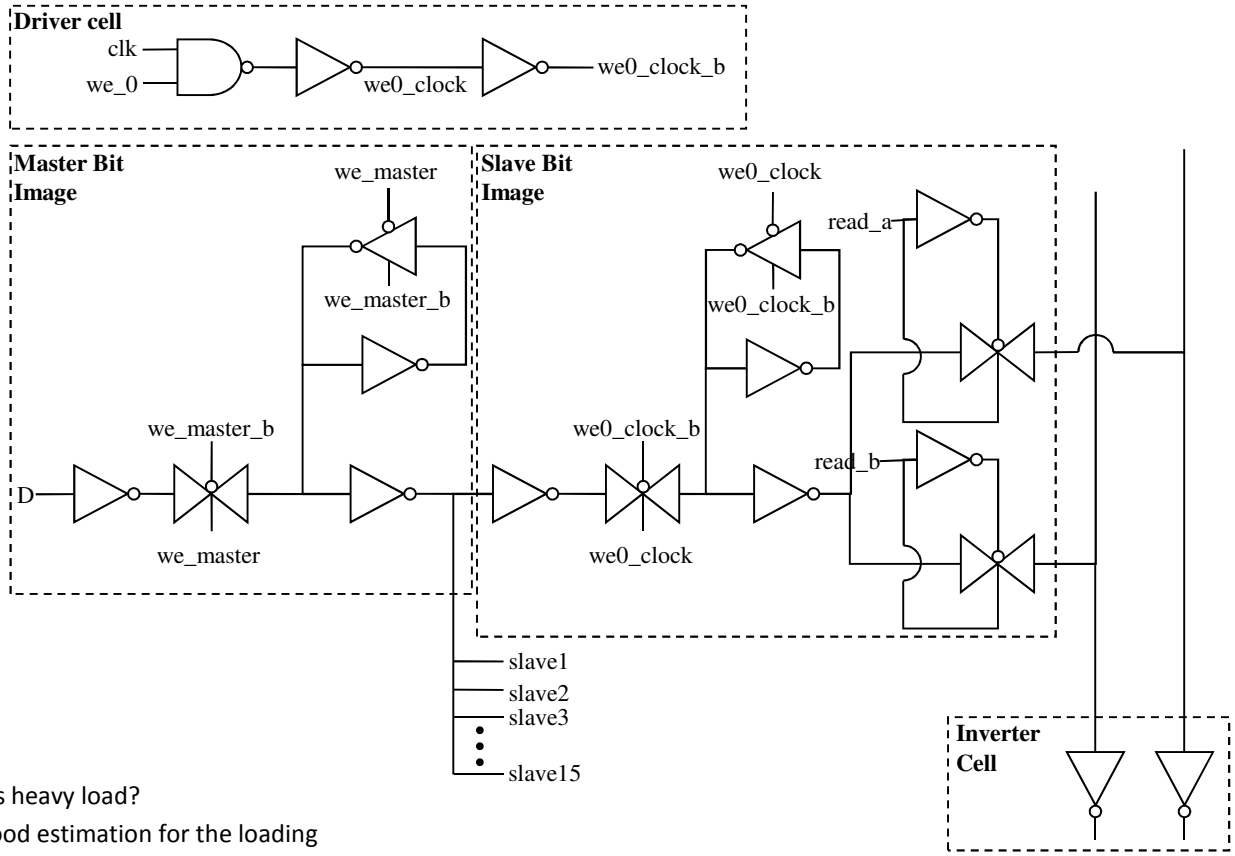
- Analyze your design to see how many wiring tracks are needed before deciding on a bit pitch



More Tips

- Reserve Track.
- Partition the work between your teammates.
- Design Hierarchy. (you should already leaned this in CAD1)
- Consist routing track between macros.
- Consist bit width for all macros.

Speedpath



- Which node has heavy load?
- How to get a good estimation for the loading
- Total load = wire load + gate load
- Be careful oversize (why?)
- Find a target and get a reasonable size (logic effort is a good reference, but iterations are also needed)

Also

- *.cdslck in your cadx folder
- *.cdslck in your HOME folder
- It is a lock file; means you are editing something.
- So, after you finish editing, be sure there is no such file. Usually, icfb will delete it after you close it; however, if not, please delete it.

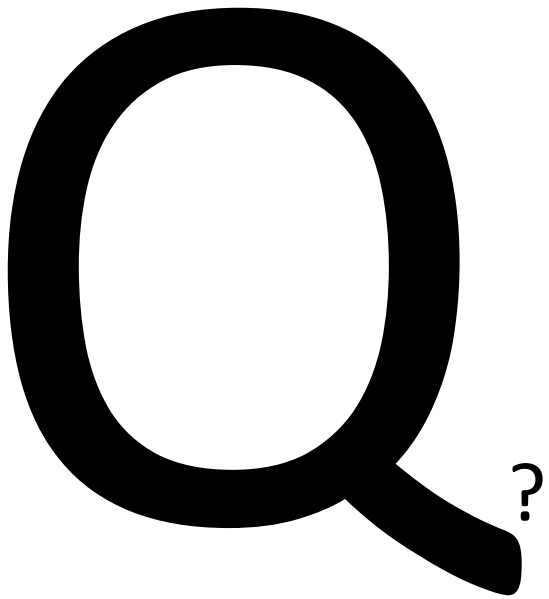
Make Hspice faster

- Turn off the log
- Analog Design Environment (ADE)

  -> Setup

  -> Environment

  -> un-click “output log”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