Today

• Presentation given by 2 groups from last semester
• CAD4
CAD4 requirements

• No metal4 and metal5 until datapath assignment
• Implement ADD, SUB, CMP, AND, OR, XOR, and immediate form of those functions
• Remember to implement the sign/zero extends
• Bit-slice width match with RF
• The VDD and GND metal2 power grid should use the same track as RF.
Logic functions

• 2 ways to implement the logic functions
  – Muxing: higher power, faster
  – Utilize part of the adder: lower power, slower.
    (Sum= A xor B xor C, Carry=AB+AC+BC)
    • XOR: output from sum, cin=0 for every bit
    • AND: output from Cout, cin=0
    • OR: output from Cout, cin=1
PSR
(Processor Status Register)

• Have signals ready for PSR
• PSR conditions: (Cn= carry out of MSB)
  – C: carry ( Cn for ADD, Cn_b for SUB)
  – F: overflow (Cn xor Cn-1)
  – Z: isZero (Nor bits of ALU output)
  – N: negative (Cn xor Cn-1 xor Sn-1) (signed)
  – L: low (Cn_b) (unsigned)

More detail, please look at “427 Baseline Arch.”
Future CAD/Discussion

• CAD Assignments
  – CAD4 is ALU (Custom)
  – CAD5 is Shifter (Custom)
  – CAD6 is Program Counter (Verilog)

• Discussion
  – 10/6: Baseline Architecture/ Verilog
  – 10/13: Tutorial2: Verilog/ Synthesis
  – 10/27: Tutorial2: Auto Place & Route (APR)
  – 11/3: Tutorial2.5: Integration