Discussion 5

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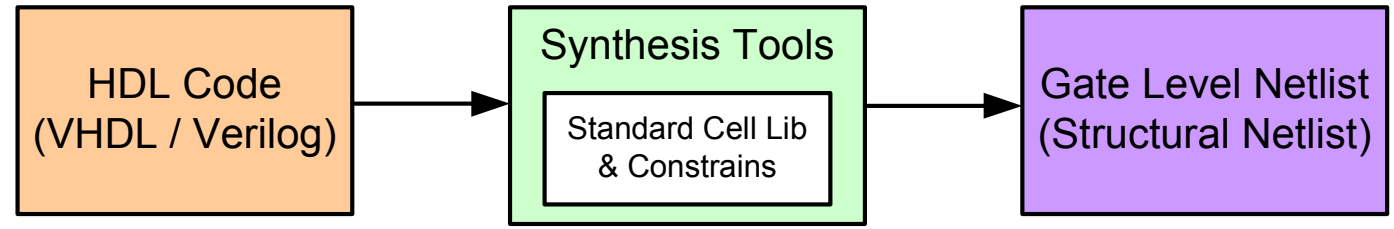
2009/10/13

Today

- Tutorial 2 (Synthesis + APR)

Synthesis Flow



add2.v

```
module add2 (Y, A, B);
input [1:0] A, B;
output [1:0] Y;

assign Y[1:0] = A[1:0] + B[1:0];

endmodule
```

Std Cells:

INVX1TR
INVX2TR
AND2X1TR
AND2X2TR
OR2X1TR
OR2X2TR

Constrains:

set input delay
set output delay
set output load
set clock period

add2.nl.v

```
module add2 (Y, A, B);
input [1:0] A, B;
output [1:0] Y;

XORX2X1TR I1 (.Y(Y[0]), .A(A[0]), .B(B[0]));
AND2X2TR I0 (.Y(C0), .A(A[0]), .B(B[0]));
XOR3X2TR I2 (.Y(Y[1]), .A(A[1]), .B(B[1]), . C(C0));

endmodule
```

- Synthesis tools will choose the size of the std cell according to the design constrains

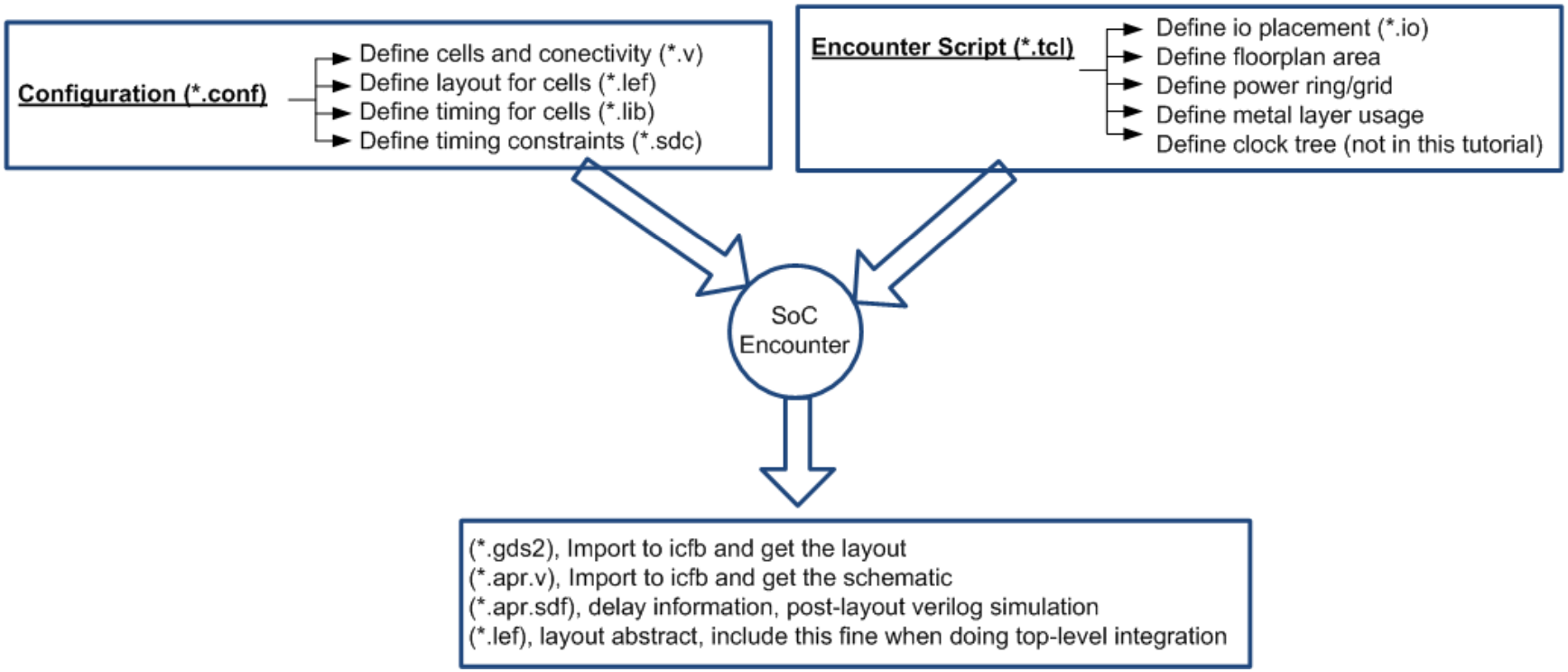
Preparation

- Behavioral Verolog
  - mult.v
- Script for ***Design Complier (DC)***
  - mult.tcl (define general constrains)
  - timing.tcl (define timing constrains)
  - common.tcl (define standard lib)
  - namingrules.tcl (key words reservation)
- What you get after ***Design Complier (DC)***
  - mult.nl.v (structural netlist)
  - mult.dc.sdf (delay info)
  - mult.dc.rpt (report)

Demo

- Netlist and Report

APR Flow


Configuration (*.conf)
Define cells and conectivity (*.v)
Define layout for cells (*.lef)
Define timing for cells (*.lib)
Define timing constraints (*.sdc)
Encounter Script (*.tcl)
Define io placement (*.io)
Define floorplan area
Define power ring/grid
Define metal layer usage
Define clock tree (not in this tutorial)
SoC Encounter
(*.gds2), Import to icfb and get the layout
(*.apr.v), Import to icfb and get the schematic
(*.apr.sdf), delay information, post-layout verilog simulation
(*.lef), layout abstract, include this fine when doing top-level integration

Preparation

- Netlist from ***DC***
  - mult.nl.v
- Script for ***Encounter***
  - mult.conf (configuration file)
  - mult.tcl (command script)
  - mult.sdc (timing constraint)
  - mult.save.io (io position)
- What you get after ***Encounter***
  - mult.gds2 (layout stream file)
  - mult.apr.v (post-apr netlist)
  - mult.apr.sdf (delay info after apr)
  - mult.lef (layout abstract file)

Demo

- APR in Encounter
- Import Stream/Netlist
- DRC/ LVS clean
- Post-layout verilog simulation

What you should do after demo

- Go through the tutorial 2 yourself!