

Discussion6

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2009/10/27

Announcement

- 11/2 (Mon), I will take about some basic charge-recovery concepts, and some of my previous work

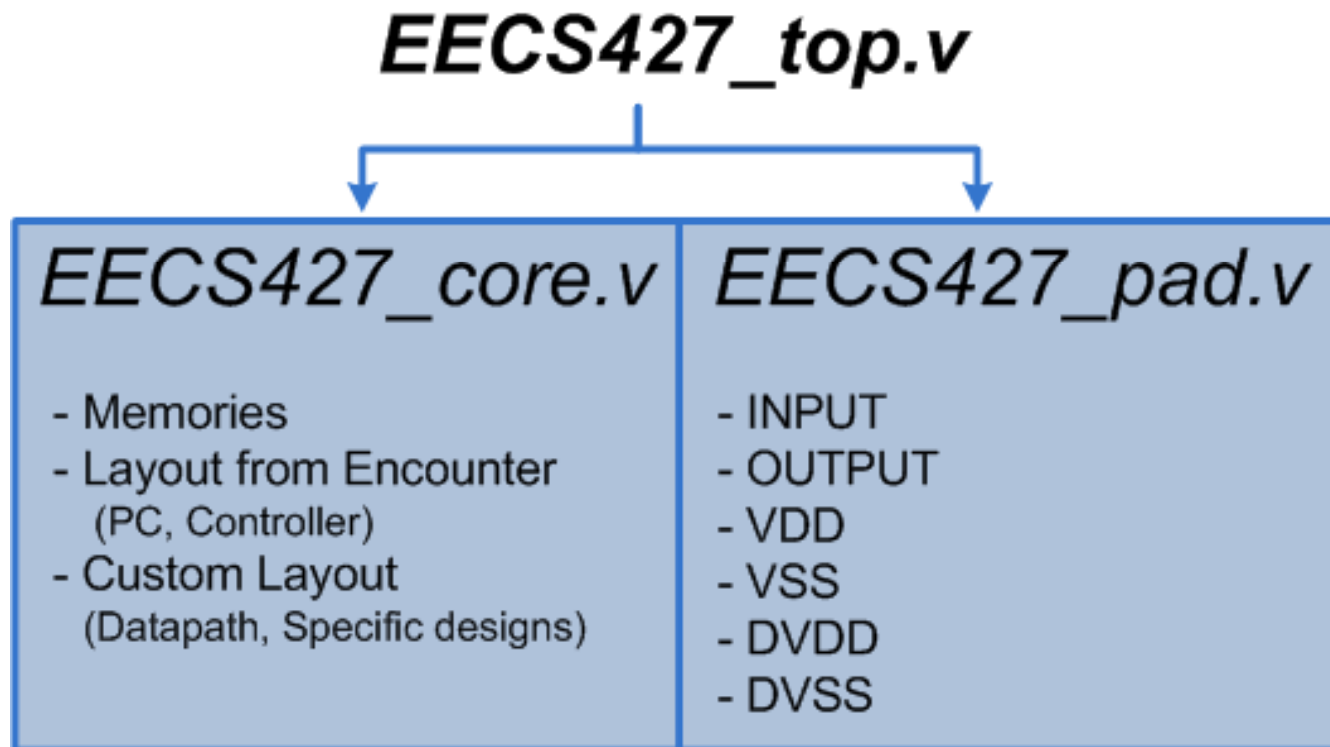
Today

- Finish Tutorial 2 (Post-layout simulation)
- Tutorial 2.5 (Integration Tutorial)
- Integrate everything together: memories, layout from Encounter, and layout from your CAD assignments.

Post-Layout Simulation

- Much faster than full spice simulation
- *.apr.v + *.apr.sdf
- Demo..

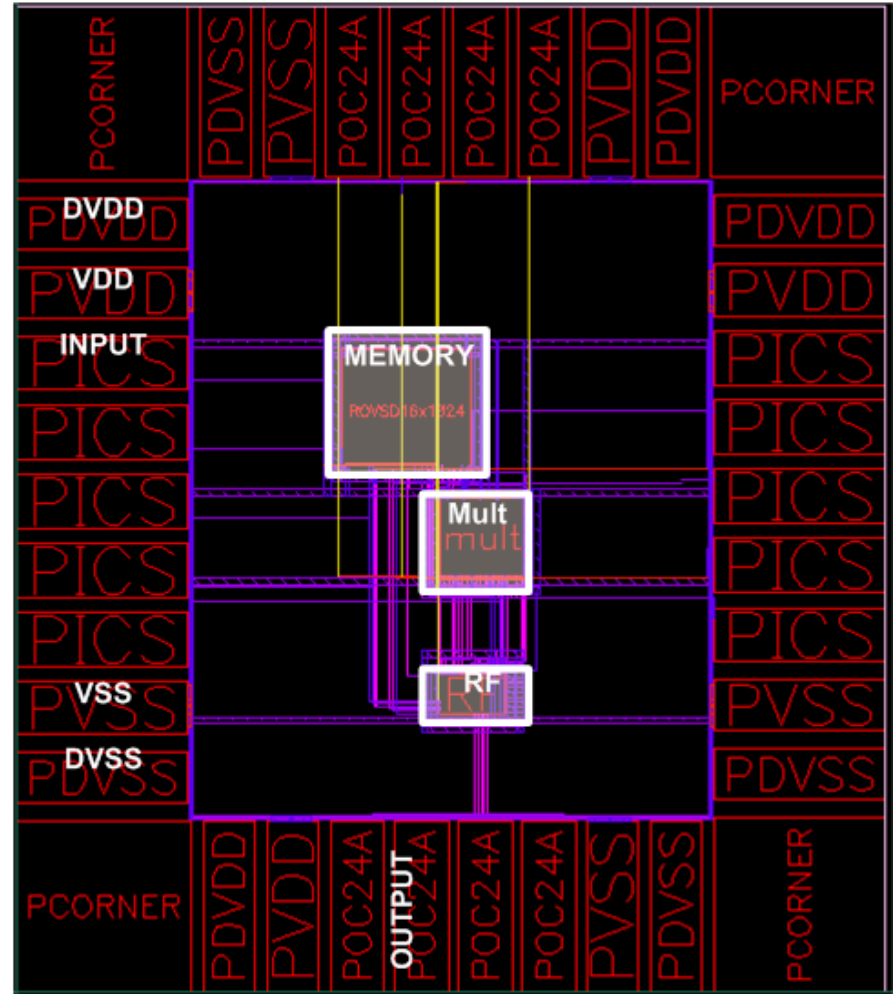
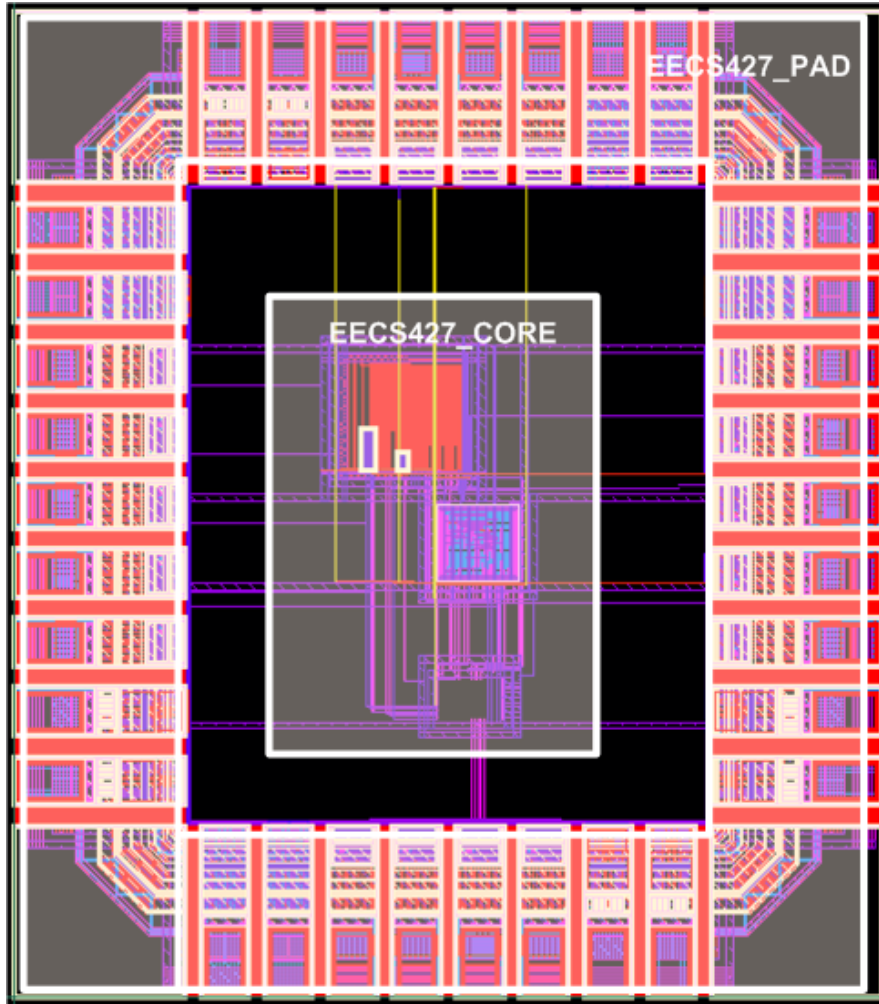
Integration Hierarchy



Dirty VDD, Dirty VSS

- Dirty VDD (DVDD) is a power supply to communicate with outside world.
 - DVDD has more noise.
 - DVDD is usually larger than VDD.
- Dirty VSS (DVSS) should be separated from VSS to avoid noise issue.

Layout



What do you need before integration?

- Decide which memory you want to use
- *.lef and *.apr.v after Encounter
- *.lef and *.v for your custom layout
- A verilog file that has the connectivity of all blocks (without pads)
- The order for your I/O pads

For your custom designs

- *How to make a verilog file for your custom designs?*

A: Make an empty module with all inputs, and outputs (you don't have to include VDD, VSS).

- *How to make a lef file for your custom designs?*

A: Please refer to the lef_example layout, and we also have the tutorial for you.

Demo

- LEF_EXAMPLE
- EECS427_CORE.v (Define the connectivity)
- EECS427_TOP.raw (Define the I/O pads)
- Encounter
- Stream in, Verilog in,
- Fix DRC.
- Add DVDD, DVSS labels and pass LVS.