CAD7 Datapath Assembly FALL 2009

Assignment

To assemble and simulate the pipelined datapath of your microprocessor.

Description

The datapath of your microprocessor stores, accesses, and computes the operands of your instructions, and interfaces with the external modules. A good starting point for this exercise would to be to look at the data flow for each of your instructions and make sure that you have all the components necessary to do the desired computations. By now, you have designed most of the components needed to achieve the desired functionality. You may need to design tristate drivers and/or muxes and pipeline registers if you need them. You must decide whether to locate modules on or off of the datapath. For example, you may decide to put the IR and PSR on the datapath. If so, you should design those and incorporate them into your datapath in CAD7. Otherwise they will be left until CAD8 when the controller is designed. You must also commit to either a tristate bus or multiplexor-based design; this decision together with the placement of modules on the datapath dictates the number of busses on your datapath. A natural next step is to assemble all of the modules together (in both the schematic and the layout) and simulate for functional and timing correctness. This requires that you present correct control signals to all of the control points in the simulation (these are input signals, since you do not yet have the control logic).

Procedure

The datapath is rather large and running *HSpice* on the whole design will take a long time. Instead, with the datapath **complete**, you may extract the load capacitance on each of your module outputs by looking at the parasitic (PEX) report. Place the load capacitance values into earlier circuit simulations of each datapath module for the OutCap and re-simulate your modules in *HSpice*. This should give you more accurate delays for that particular module. You should generate new *HSpice* waveform files for the delays you calculated in the previous CADs.

Simulate the entire datapath in *NCVerilog* for functional verification. You will have to force control variables and register file select signals by yourself since you do not, at present, have the decoder. You will have a lot of control signals to force. You may find it simpler to begin coding a simple controller in Verilog to provide the input stimulus, particularly if you have someone in your group that has written behavioral/functional Verilog in the past.

Run at least one simulation each for all instructions (both Reg-Reg and Reg-Immediate). Pay careful attention to the write-back portion of your “execute” pipeline stage. List and describe all of the control signals for the datapath in your README. Your description should include functional specifics for your individual components. You may include a truth-table if you like. This will be needed for the CAD8 assignment and will help the grader understand your verification.

Requirements

Please turn in the following in your **cad7** directory:

- Schematics of the entire datapath.
- Layout of the datapath. Please refer to the layout in **LEF_EXAMPLE**. You should extend all pins to the boundary and wire “VDD” and “VSS” pins together on the edges. **NO NETS ARE ALLOWED TO BE “*JOINED NETS WITH SAME NAME*” OR VIRTUALLY CONNECTED**, so you should NOT select that option in your final LVS run.
- *NCVerilog* simulation of the entire datapath. You should demonstrate a few examples of each arithmetic/logic operation, as well as important cases such as system reset. Please list in your

README file the path to the ***testfixture.verilog*** file you used to test the circuit so the grader can run the simulation.

- List of all the control signals with descriptions. You may include a truth-table.
- Documentation is important, so make sure you comment your report well. Important considerations that went into the design, and extra features, if any, should be documented.
- Create a table in your README showing the new delay number for each block (register file, ALU, shifter, PC, new blocks…) and the total delay by adding them up. Also compare the delay you got in the pre-CAD7 assignments with the new numbers.
- Reference *HSpice* files and associated schematics that were used in obtaining delays for any new blocks that were designed in CAD7.
- Report files (DRC and LVS) for the datapath should be placed in the CAD7 directory.

Deadline

You need to turn in CAD7 by **Tuesday, November 11, 2009, 7pm**.