EECS 427 Fall 2009
HW1 (review)
Due date: Monday, 9/21 at 1:30 pm in class

1. Scaling

An embedded microprocessor consumes 0.72 mW/MHz (excluding leakage power) when fabricated using a 0.18 µm process. With typical standard cells (gates), the area of the processor is 2 mm^2. Assume a 600 MHz clock frequency, and 1.8 V power supply. Its leakage power is 50 µW. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

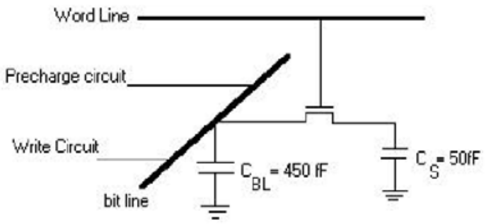
a) Power density is important for cooling the chip and packaging. Scale the circuit so that the power density decreases to 150 mW/mm^2 but the current density remains constant. What is the new frequency of the circuit?

b) Go back to the original processor and calculate the scaling required for the circuit to dissipate 0.54 mW/MHz. If there are many ways to do that, choose the one that gives maximum frequency without affecting the power density more than 20%. What is the die area of the new circuit?

c) If the threshold voltage in the 0.18 µm process is 0.4V, what should be the threshold voltage in 0.13 µm process with 1.3V supply voltage? Assuming 90 mV/dec subthreshold slope, what would be the leakage power of the new processor?

2. Memory

A 1-T DRAM cell consists of a single transistor connected in series with a capacitor. For a read, the bit line is precharged to $V_{DD}/2$ by a clocked precharge circuit. Then, the access transistor is turned on by applying V_{DD} to the word line. A write is performed by applying V_{DD} or GND to the bit line and V_{DD} to the word line. Assume that $V_{To} = 0.4$ V, $\gamma = 0.3$ V$^{1/2}$, $|2\phi_F| = 0.6$ V.

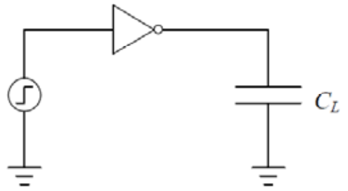


a) Find the maximum voltage across the storage capacitor C_s after a writing a 1 into the memory cell (i.e., bit line is driven to $V_{DD} = 2.5$V).

b) Ignoring leakage currents, find the voltage on the bit line when this “1” is read from the memory cell.

3. Sizing

Consider a standard CMOS inverter shown above driving a capacitive load $C_L = 80$ fF with a relatively fast step at its input. Assume that a minimum size “unit” inverter has symmetric high and low drive strength $R_{eq,u} = 20$ kΩ, intrinsic output capacitance $C_{int,u} = 3$ fF, and input capacitance $C_{in,u} = 4$ fF. Also assume that inverter resistances and capacitances scale linearly with size.



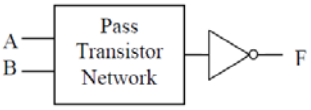
a) What is the shortest t_p that can possibly be attained for the above circuit by sizing the inverter, and how would it be sized? Call this delay t_{pmin}.

b) What size should the inverter be, relative to the unit inverter, to obtain $t_p = 1.3t_{pmin}$? What are the input and intrinsic output capacitances of this inverter?

c) Now consider the dynamic energy consumed driving C_{in}, C_{int}, and C_L over a complete input cycle (one logic transition in each direction). What inverter size minimizes the energy delay product of this circuit? How do the inverter capacitances compare to C_L in this case?

4. Logic

The function F = A XOR B is to be implemented in pass transistor logic according to the diagram below.



a) How would you implement the pass transistor logic with NMOS-only switches? Assume both true and complimentary input signals are available.

b) What is the minimum voltage at which this circuit will operate correctly (and why)? For the NMOS switches use $V_{TH0} = 0.5V$, $\gamma = 0.4V$, $2\varphi_F = 0.6V$. Assume that the inverter has an ideal VTC that switches when its input is at $V_{DD}/2$.

c) A level restoring PMOS transistor is now added as shown in the figure below. What are the benefits and drawbacks of this modification?