EECS 427 Homework 4, Fall 2009

Due Monday, November 16, 2009 at 7 pm

In this homework assignment, your group is to write a formal proposal for your chip. The proposal must be no more than 6 pages (less than 3000 words). See http://www.acm.org/sigs/publications/proceedings-templates for the Microsoft Word or LaTeX templates that you can use for this and your final report format. There is also a link on the course webpage to past project reports using these formats and a pdf version of the baseline processor block diagram for your use in the detailed proposal/final report. The proposal must include:

- An overview of the chip application.
- A register-level block diagram showing off-chip and on-chip components
- Discussion of why you propose to implement the chip in this way.

The proposal should be submitted to the instructor by email. Figures must be computer-generated. Be sure to cite any references you've used in your proposal, including those from web sources. Plagiarism will result in no credit and the honor council will be notified.

You should write this proposal so that at least some of it (possibly edited) can be used in your final written report, which must conform to the format used in the DAC Student Design Contest. It is not required that the title and abstract be on a separate page for this proposal. If you enter the contest, please refer to the information on the contest web site, http://www.dac.com/47th/studcon.html for any updates to the format and rules (this website is for DAC 2010, you would be submitting to DAC 2011).

The following are guidelines for the design contest entry - NOT the detailed proposal. But since a good portion of the detailed proposal may be appropriate for the design contest entry, you may be interested in these guidelines at this point.

DAC Contest Entry Requirements

The purpose of this contest is to promote excellence in education for integrated circuit designers at universities. It provides competition between students participating in classes and in research who design and fabricate integrated circuits.

The contest will be split into two groups, a "conceptual" class and an "operational" class. The conceptual class is for designs that are not fabricated. The report should include detailed instructions on how the design will be tested. The operational class is intended for designs that have been fabricated and tested. The final report must include a die photograph.

Both contests will be for the most innovative VLSI project created by a student or team of students who are or have been enrolled in VLSI classes or research at any university in the

world. A panel of judges from industry, representing the companies that donate prize money, and DAC will evaluate the entries and decide how the money will be divided.

CRITERIA FOR ENTERING THE CONTEST

The contest is for any full time graduate or undergraduate students and the design must have been completed within 18 months of the contest.

To be eligible for the contest, a chip must meet functional needs and be non-proprietary. If your chip is tested, you must report the results even if they were negative. A testing procedure should be included whether or not you have tested the chips.

All work on the project must be done using facilities, equipment and design tools provided by the respective university. Any design style supported at the university may be used, including full-custom, standard-cell, symbolic, compiled, FPGAs, etc.

REPORT SPECIFICATIONS AND HINTS

Judging will be based upon the written report. Each report shall have an abstract of no more than 60 words and a report body of no more than 6000 words, with a recommended length of 4000 words. The pages must all be 8.5 x 11 inches. A figure showing your layout should be included.

Since projects are judged solely upon the written reports, clarity and completeness of the report are of paramount importance. Spelling and grammatical errors will not be impressive. Writing style should be clear and concise. Remember that the judges' expertise may not be in the area of your project. Make your explanations straightforward and understandable.

Design for testability is a critical issue and must be included in your final report if the device is not going to be fabricated. Discuss testing issues you have considered in the design and approaches you took or will take in testing. Engineering specifications and performance statistics can be efficiently presented in tabular form.

REPORT OUTLINE

1. Abstract (no more than 60 words, italicized).

2. System Overview. Include motivation for designing the chip. Is VLSI appropriate? Does this design satisfy the system requirements? What is unique about this project? What novel ideas or elegant solutions does the design include?

3. Implementation and engineering considerations (bulk of the report):

- Specifications: functional, timing, electrical, and environmental (temperature).
- Tradeoffs: architectural and circuit tradeoffs, I/O considerations, floor-planning and interconnect approaches. Emphasis should be placed on why you did what you did.

- Timing and Critical Paths. What clocking scheme is used? Why? Which paths are critical? Have you simulated or measured their delays?
- Block Diagram, Logic / Circuit Diagrams, and Algorithms.
- Die Photo or Layout Plot (annotate so various blocks can be identified).
- Verification and Simulation (keep it brief): how did you assure that the chip would work as specified?
- Testing: how did you, or will you, test this part with I/O pins only? What test equipment did you use? Actual test results, if available, should be summarized.
- Chip statistics: die size, total power, number of transistors, density of layout, maximum clock speed, etc.

4. Summary

5. References

JUDGING CRITERIA

Entries will be judged on the following criteria:

1. Soundness of engineering, including evaluation of tradeoffs and ingenuity at all levels of design activity (note that ingenuity is usually seen in simplicity, rather than added complexity).

2. Clarity of the functional specification, system description, and chip description.

3. Producibility and testability of the chip including explanations of any special test procedures you have included to make the part producible.

CONTEST DATES

1. Entries are estimated to have a submission deadline of Nov. 2010.

2. Winners will probably be notified late Feb. 2011.