EECS 427 Homework 5, Fall 2009

Presentation in class on Monday, December 14, 2009 1:40 – 4 pm
Final report due Monday, December 14, 2009 at 7 pm

FINAL REPORT

Use HW4 as the basis in building up your final report. Add layout picture and final simulation results. The report should be no longer than 6 pages. You can use the outline below as guidance.

1. Abstract (no more than 60 words, italicized).

2. System Overview. Include motivation for designing the chip. Is VLSI appropriate? Does this design satisfy the system requirements? What is unique about this project? What novel ideas or elegant solutions does the design include?

3. Implementation and engineering considerations (bulk of the report):

- Specifications: functional, timing, electrical, and environmental (temperature).
- Tradeoffs: architectural and circuit tradeoffs, I/O considerations, floor-planning and interconnect approaches. Emphasis should be placed on why you did what you did.
- Timing and Critical Paths. What clocking scheme is used? Why? Which paths are critical? Have you simulated or measured their delays?
- Block Diagram, Logic / Circuit Diagrams, and Algorithms.
- Die Photo or Layout Plot (annotate so various blocks can be identified).
- Verification and Simulation (keep it brief): how did you assure that the chip would work as specified?
- Testing: how did you, or will you, test this part with I/O pins only? What test equipment did you use? Actual test results, if available, should be summarized.
- Chip statistics: die size, total power, number of transistors, density of layout, maximum clock speed, etc.

4. Summary

5. References

Please also append 1 to 2 pages to your final report to include the following items:

1. System diagram showing interconnection of major system blocks such as: microcontroller core (controller + datapath), on-chip peripherals and off-chip devices needed to realize the system. The microcontroller core should be a module by itself. There's no need to explicitly show datapath, control or datapath submodules. (If this diagram is already included in your final report, you can simply omit it.)

2. Bond pad diagram and pin assignment. This simple diagram should show all pads necessary for your design arranged around the periphery of the chip in the order you intend. Each pin should have a name or label. A table should accompany this diagram showing pin name, function and what external device pins the pin will connect to. For power and ground, plan on at least one of each for each side of the chip (minimum of 8 pins for power and ground).

Please send your final report along with the appendix in Word to the instructor by email.

PRESENTATION

We will use the final lecture (December 14) for design presentations. These will consist of a 15-20 minute presentation that includes a small amount of time allotted to questions/answers (aim for 12 minutes + 3 minutes for Q/A). You should provide an introduction to your application, and a discussion of your changes/additions to the baseline including particular emphasis on a portion of your design that you feel is unique or implemented well. This will often be one of your datapath components, or something specific to your application. Provide layout and critical path analysis information of whichever component you choose to emphasize. Examples might include a tree-style adder, the register file design, a unique custom designed peripheral, or the use of any novel design techniques described in class (pulsed registers, bus encoding, gated clocks, sleep transistors, etc.).

Describing and reviewing a design is a common step in any design flow. Design reviews can take on many forms, from formal high-level reviews with customers in attendance to more informal reviews in which a designer's peers will review the design in an effort to uncover any potential problems that were overlooked. This presentation is not really a design review in that typically you would need a lot more time to adequately review a design of this size. Also, reviews are usually done at an earlier time such that changes resulting from the review can still be incorporated into the design. Nonetheless, this exercise serves as a good opportunity to practice the same skills used in conducting a design review.

A grade will be assigned based on the effectiveness of your talk, including your use of the presentation materials. You must attend in order to receive full credit for this assignment.

Excessively short (e.g., <10 minutes) or long (e.g., >15 minutes) will affect your grade. You may assign one person to speak for the group, or at most two may speak provided it is done within the allotted time period. Please send your presentation slides to the instructor by 1:30 pm on the day of your presentation. A laptop will be provided for the presentation, or you can use your own.

Time slots:

1:40-2:00: Group 1
2:00-2:20: Group 2

2:20-2:40: Group 3
2:40-3:00: Group 4
3:00-3:20: Group 5
3:20-3:40: Group 6
3:40-4:00: Group 7