EECS 427
VLSI Design I

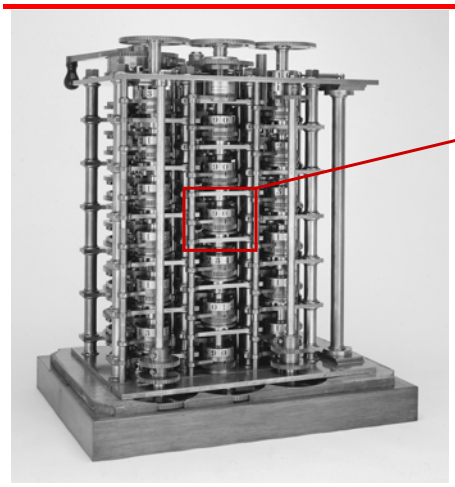
MW 1:30-3:00pm
Disc: Tu 5:30-6:30pm
Zhengya Zhang
http://www.eecs.umich.edu/courses/eecs427

Slides based on lectures by Prof. Blaauw, Sylvester and Prof. Nikolic, UCB

Outline

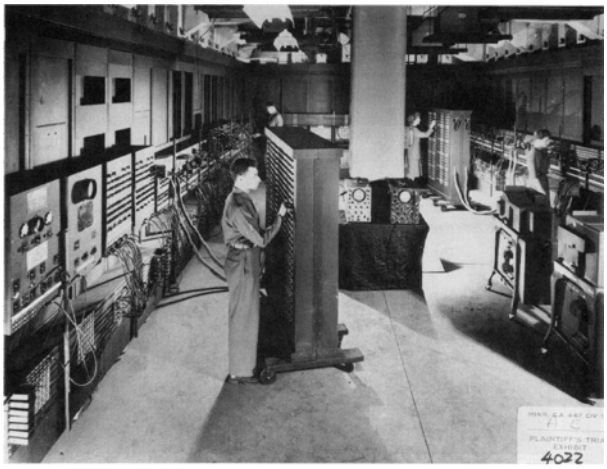
- What you can expect to learn in this class
- Logistics – syllabus, deliverables, grading
- CMOS manufacturing process

The First Computer

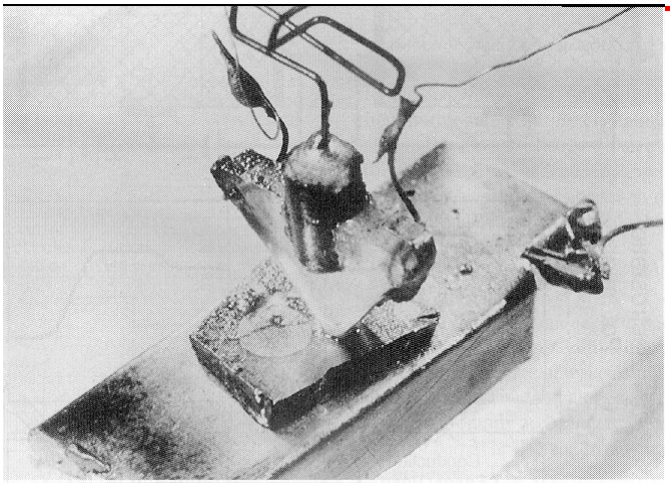


- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470

ENIAC

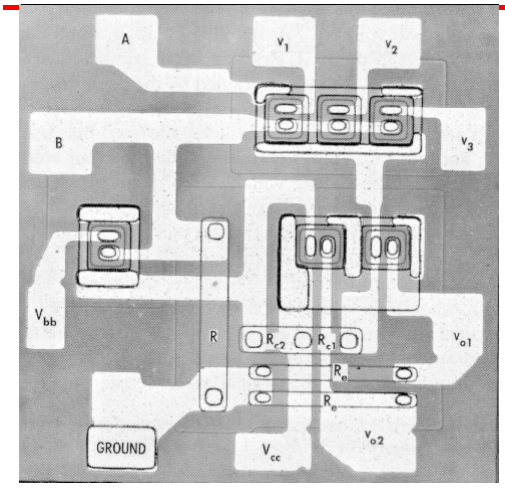


The First Transistor



First transistor
Bell Labs, 1948

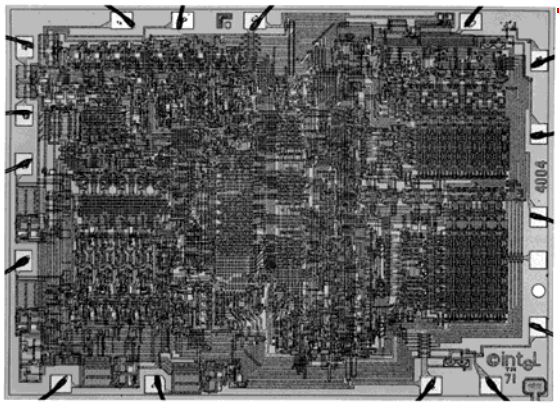
The First Integrated Circuits



Bipolar logic
1960's

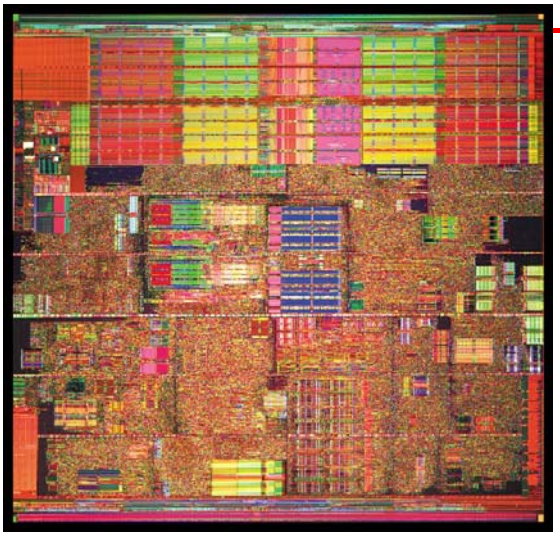
ECL 3-input Gate
Motorola 1966

Intel 4004



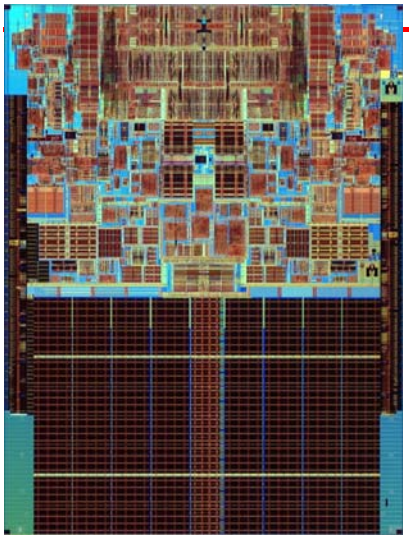
Intel, 1971.
2,300 transistors (12mm^2)
740 KHz operation
(10μm PMOS technology)

Intel Pentium 4



Intel, 2005.
125,000,000 transistors
(112mm^2)
3.8 GHz operation
(90nm CMOS technology)

Intel Core2

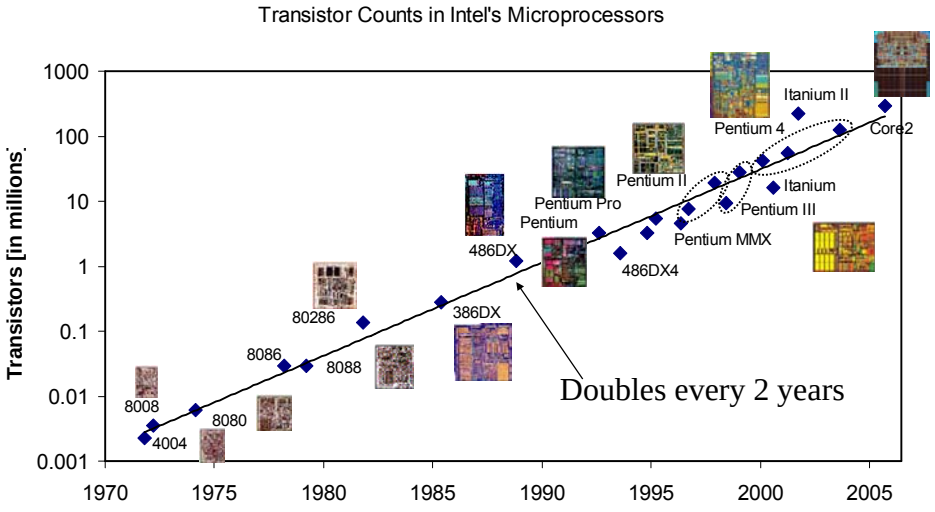


Intel, 2006.
291,000,000 transistors
(143mm^2)
3 GHz operation
(65nm CMOS technology)

Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Transistor Counts

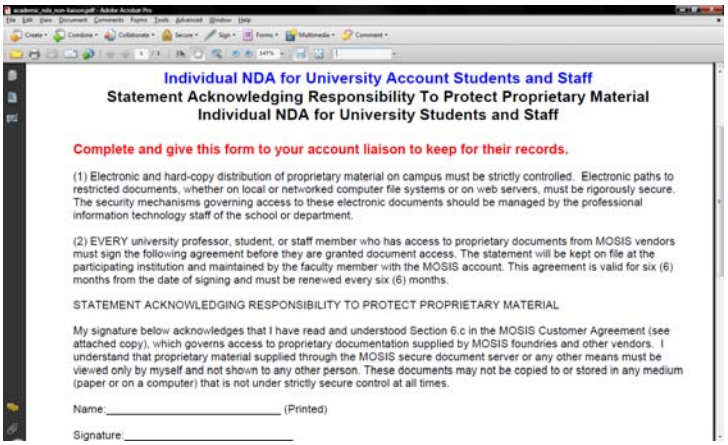


What you will learn in 427

- 312 – Transistors design and behavior
- 270 – Logic design – combining transistors
- 370 – Architecture – high level organization

- *427* – VLSI: realization of circuits in silicon:
  - The entire process of very large-scale integration
  - Generation of custom layout
  - Sub-system design such as adders, register files..
  - Synthesis + automated place/route design flow
  - Advanced circuit design topics: pulsed latches, memory decoder and sense amplifiers, power, etc.
  - *Project – Focus on Custom Design – Teamwork*

Non-Disclosure Agreement



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Name:_____ (Printed)

Signature:_____

Teaching Staff

- Primary instructor:
  - Zhengya Zhang
    - 2416 EECS, zhengya at eecs.umich
    - Office hours: MW 3-4pm (tentative). Both lecture material and project.
- GSI:
  - Wei-Hsiang Ma
    - 2713 CSE, wsma at umich
    - Office hours: MTh 4-6pm, Tu 6:30-7:30pm
    - Support of CAD (Computer-Aided Design) tools and project related issues as well as lecture material.
- Reader:
  - Bhavi Bhadviya
    - bhavi at umich
- Staff support:
  - Joel Van Laven
    - Major CAD tool issues (pertaining to the project); consult *after* Wei-Hsiang

Course Setup

- Mon and Wed lectures in 185 EWRE
- Tuesday discussion section led by Wei-Hsiang Ma (1003 EECS)
  - Purpose of discussion: review lecture topics, review CAD assignments and answer project related questions
- Homework assignments
  - Only 1 'typical' HW, others handle planning issues of project (groups, initial proposal, etc.)
- CAD assignments
  - Roughly weekly, several 2+week assignments
  - Each assignment represents a component of your final microprocessor design
  - First 2 are individual, rest are in groups
- Quizzes: 2 - roughly every 6 weeks, non-cumulative.

Project

- Main component of class, 70+% of your grade
- Design a 16-bit RISC (reduced instruction set computing) processor
  - Groups of 4 (you choose)
    - Good to have a mix of EE and CE
    - Baseline architecture (instruction set) given to you; you choose and implement a circuit-level enhancement technique
  - Time requirements: 30-40 hrs/week avg. 427 → 24/7
  - Peer contribution forms; must pull your weight
- Learn full-custom design (datapath) and automation tools (logic synthesis + custom router + place/route)
- You can send this design off to be fabricated and then test it later as a directed study or possibly in EECS 579 (encouraged!)

Logistics

- Course Textbook:
  Digital Integrated Circuits: A Design Perspective, 2nd edition by Rabaey, Chandrakasan, and Nikolic
- Lecture notes will be posted online shortly after class sessions and I will bring copies to class for note taking
- Book will be supplemented with several handouts from other sources throughout the semester
- Other books on reserve at Media Union (Weste, Chandrakasan)
  - Weste/Harris in particular is recommended if you want to pursue a career/graduate studies in digital circuits

Grade Breakdown

- Your project, in the form of CAD assignments and final report/presentation, is the dominant part of your grade

Homework	10%
CAD assignments	35%
Quizzes	24% (12% each)
Final project/report, indiv. contrib.	31%

CAD late policy: within 24 hours = 25% penalty, 24-48 hours = 50% penalty, see course info handout

Project Schedule

- All CAD assignments due at 7 pm except CAD9
- *Tutorial* (CAD): Wednesday, September 9, 7-9pm at CSE 1620
- CAD1 (inverter/nand/mux): Wednesday, September 16
- CAD2 (D flip-flop): Monday, September 21
- CAD3 (register file): Wednesday, September 30
- CAD4 (ALU): Wednesday, October 14
- CAD5 (shifter): Wednesday, October 28
- *Tutorial* (synthesis, place & route): Tuesday, November 3
- CAD6 (datapath): Wednesday, November 4
- CAD7 (program counter): Wednesday, November 11
- CAD8 (controller): Wednesday, November 18
- CAD9 (completion):
  - Presentation & demo: Monday Dec 14 in class
  - Report due: Same day (Dec. 14) at 1:30pm

Homework Schedule

- All HW assignments due at 1:30 pm in class
- HW1 (problem set): Monday, September 21
- HW2 (form a team): Monday, September 28
- HW3 (initial proposal): Wednesday, October 7
- HW4 (detailed proposal): Monday, November 16
- HW5 (final report): Monday, December 14
- HW6 (presentation): Monday, December 14

Quiz and Holiday Schedule

- Quiz 1: Wednesday, October 14 in class
- Fall student break: October 19, 20

- Quiz 2: Monday, November 23 in class
- Thanksgiving break: November 26, 27

- Last day of class: Monday, December 14
- No final exam

Lecture Schedule

Date	Topic	Reading/Coverage	Notes, assignments due
September 9	Course Introduction, Manufacturing	1.1-1.3 (review), 2.2, WH 3.2	Tutorial1 (7-9pm)
9/14	Design Rules & Layout	2.3, Insert A, WH 1.5, WH 3.3	
9/16	CMOS Review	5.4, 6.2	CAD1 due
9/21	Logical Effort	handouts	HW1 due CAD2 due
9/23	Logical Effort	handouts	
9/28	Logic Styles	6.2	HW2 due (teams)
9/30	Adders	11.1-11.3.1	CAD3 due
October 5	Adders	11.3.2-11.3.3	
10/7	Shifters	11.5, WH 10.8	HW3 due (initial proposal)
10/12	Multipliers	11.4	
10/14	Quiz 1		CAD4 due
10/19, 10/20 - Fall Study Break, No Classes			

Lecture Schedule

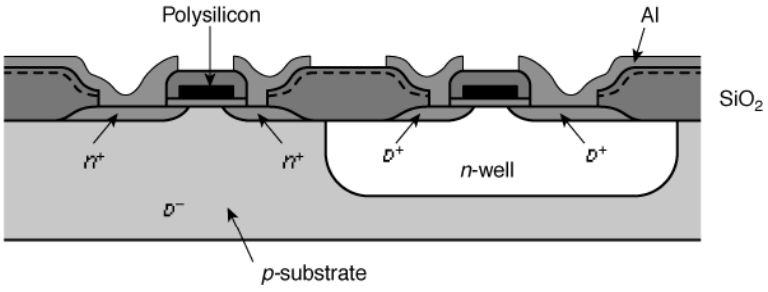
10/21	Power and Energy	5.5, 6.3, CBF 7	
10/26	Dynamic Power Reduction	11.7	
10/28	Leakage Power Reduction	6.4.2, CBF 4	CAD5 due
November 2	Dynamic Logic	6.3	
11/4	Interconnects	4.3.1, 4.3.2, 4.4.1-4.4.3, 9.3.3	CAD6 due
11/9	Design Styles, Synthesis	8.1-8.4	
11/11	Timing, skew/jitter	10.1-10.3	CAD7 due
11/16	Timing cont., D-Q, pulsed latches	10.3, 7.4	HW4 due (detailed proposal)
11/18	Memory Core and Peripherals	12.1-12.3	CAD8 due
11/23	Quiz 2		
11/25	Memory Reliability and Power	12.4, 12.5	
11/26, 11/27 - Thanksgiving Break, No Classes			

Lecture Schedule

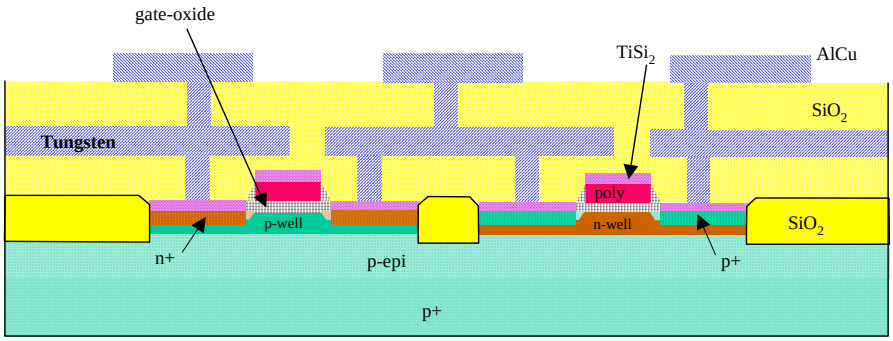
11/30	Design-for-Test (DFT)	Insert H.3, CBF Ch. 25	
December 2	Clock Distribution & Robustness	10.3.3, 10.6, CBF Ch. 13	
12/7	Advanced Interconnect Techniques	9.5	
12/9	Power Grid and Other Issues	WH 12.3, CBF 24	Course evaluations in class
12/14	Final Project Demos Final Project Presentations		CAD9: final due HW5 due (report) HW6 (presentation)

5 Minute break!

CMOS Process

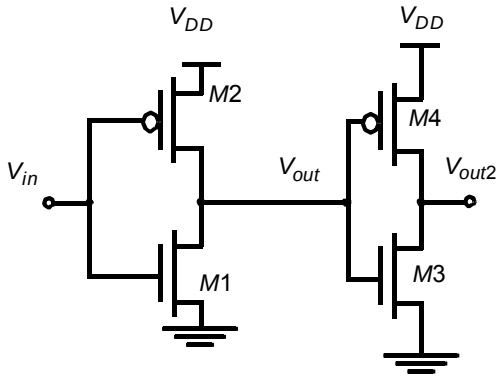


A Modern CMOS Process

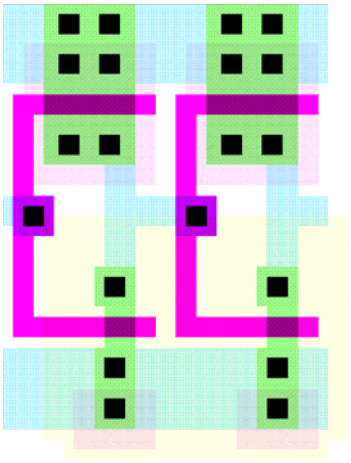


Dual-Well Trench-Isolated CMOS Process

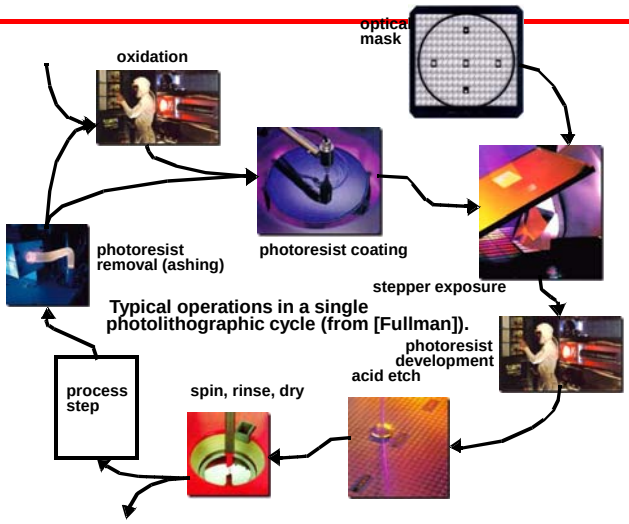
Circuit Under Design



Its Layout View

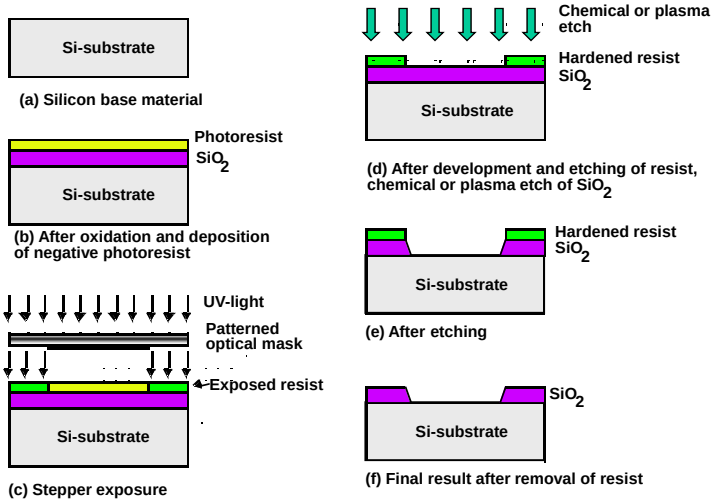


Photolithographic Process

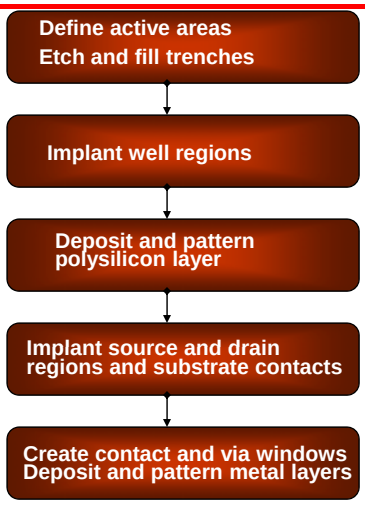


Typical operations in a single photolithographic cycle (from [Fullman]).

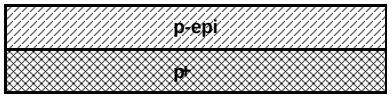
Patterning of SiO_2



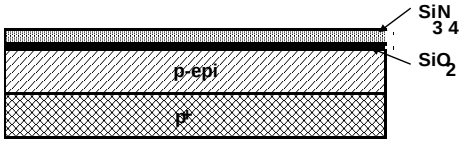
CMOS Process at a Glance



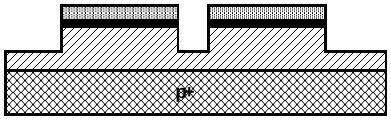
CMOS Process Walkthrough



(a) Base material: p+ substrate with p-epi layer

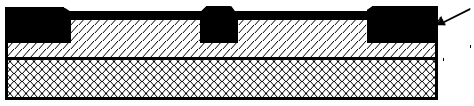


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

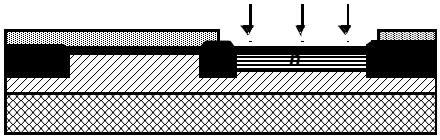


(c) After plasma etch of insulating trenches using the inverse of the active area mask

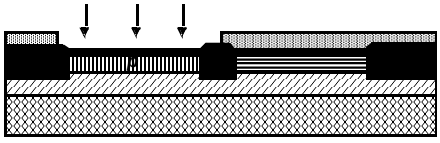
CMOS Process Walkthrough



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

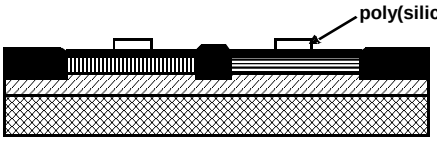


(e) After n-well and Vthp adjust implants

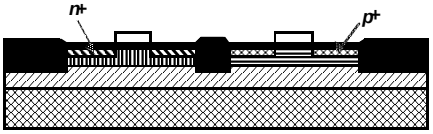


(e) After p-well and Vthn adjust implants

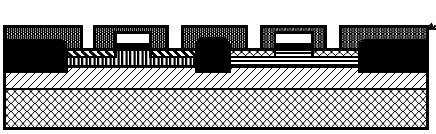
CMOS Process Walkthrough



(g) After polysilicon deposition and etch

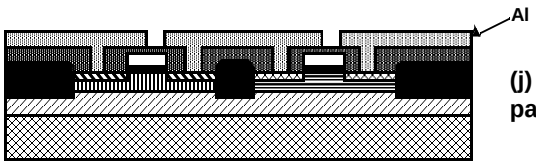


(h) After n+ source/drain and p+ source/drain implants. These steps also dope poly.

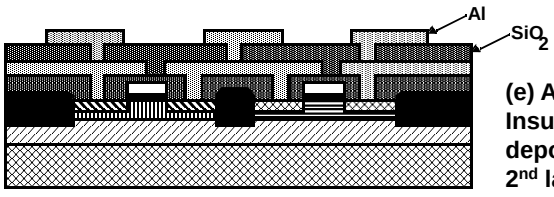


(i) After deposition of SiO2 insulator and contact hole etch

CMOS Process Walkthrough



(j) After deposition and patterning of first Al layer.



(e) After deposition of SiO_2 Insulator, etching of vias, deposition and patterning of 2^{nd} layer of Al

Looking Ahead

- http://jas.eng.buffalo.edu/education/fab/invFab/index.html
- Read Sections 1.1, 1.2, 1.3.2-1.3.4, and 2.2 of Rabaey (mostly review)
- Next lecture: we'll cover design rules and layout styles

- Logistics and due dates:
- Go to tutorial tonight
- CAD1 is due 9/16
- HW1 is due 9/21
- Form your group!