EECS 427
Lecture 11: Power and Energy
Reading: 5.5

[Adapted from Irwin and Narayanan]

Reminders

- CAD5 is due Wednesday 10/28
  - You can submit it by Thursday 10/29 at noon
- Lecture on 11/2 will be taught by Wei-Hsiang
  - Topic: ultra-low-power charge-recovering circuits
- HW4 (detailed proposal) is due 11/16
  - You should be working on your project concurrently

Overview

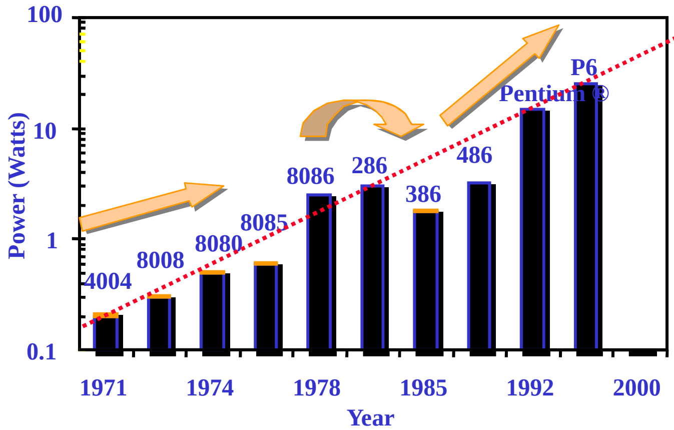
- Quiz 1 recap

- Power and energy
- Dynamic, short-circuit, and leakage

Why Power Matters

- Packaging costs
- Power supply rail design
- Chip and system cooling costs
- Noise immunity and system reliability
- Battery life (in portable systems)
- Environmental concerns
  - Office equipment accounted for 5% of total US commercial energy usage in 1993

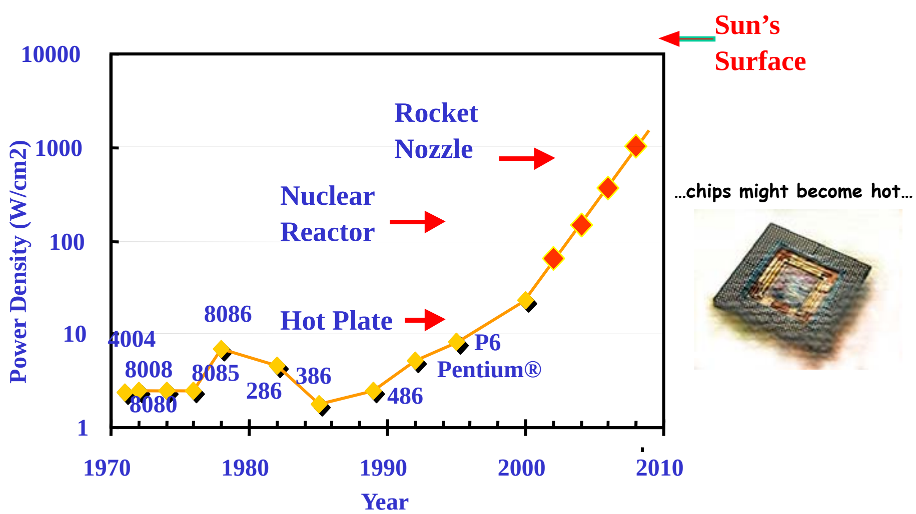
Power Dissipation



Power delivery and dissipation will be prohibitive

Source: Borkar, De Intel®

Power Density

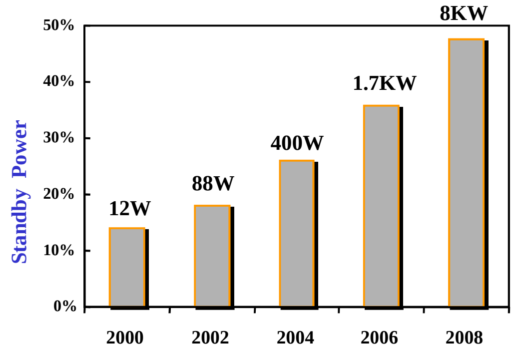


Source: Borkar, De Intel®

Standby Power

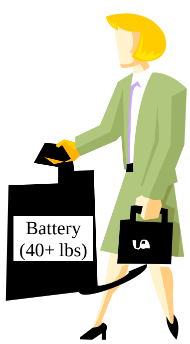
Year	2002	2005	2008	2011	2014
Power supply V_{dd} (V)	1.5	1.2	0.9	0.7	0.6
Threshold V_T (V)	0.4	0.4	0.35	0.3	0.25

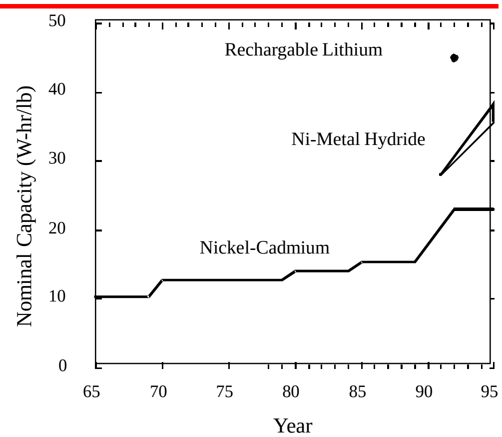
- Drain leakage will increase as V_T decreases to maintain noise margins and meet frequency demands, leading to excessive battery draining standby power consumption.



Source: Borkar, De Intel®

Battery Size/Weight





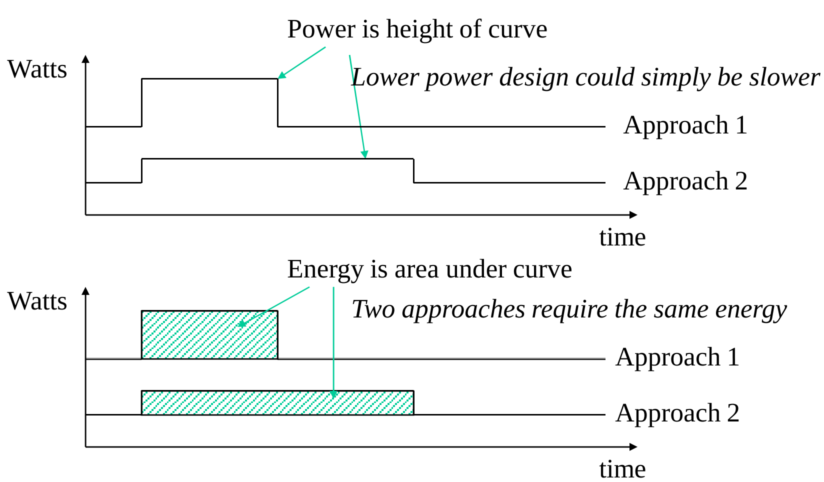
Expected battery lifetime increase over the next 5 years: 30 to 40%

From Rabaey, 1995

Power and Energy

- Power consumption in Watts
  - – determines battery life in hours
- Peak power
  - – determines power ground wiring designs
  - – sets packaging limits
  - – impacts signal noise margin and reliability analysis
- Energy in Joules
  - – Energy = power * delay
  - – Joules = Watts * seconds
  - – lower energy number means less power to perform a computation at the same frequency

Power versus Energy



Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

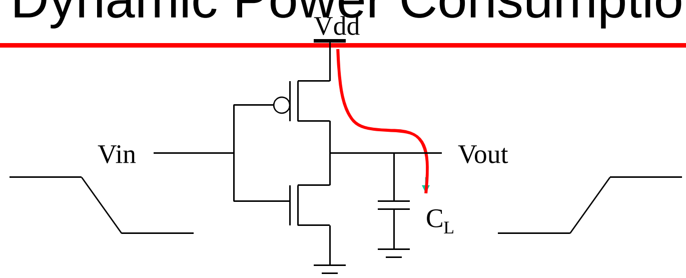
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Consumption



$f_{0\to1}$

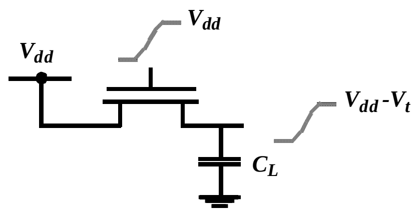
Energy/transition = $C_L * V_{DD}^2 * P_{0\to1}$

P_{dyn} = Energy/transition * f = $C_L * V_{DD}^2 * P_{0\to1} * f$

$P_{dyn} = C_{EFF} * V_{DD}^2 * f$ where $C_{EFF} = P_{0\to1} C_L$

Not a function of transistor sizes!
Data dependent - a function of switching activity!

Modification for Circuits with Reduced Swing

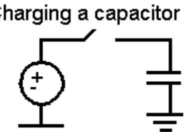


$$E_{0\rightarrow 1} = C_L \bullet V_{dd} \bullet (V_{dd} - V_t)$$

- **Can exploit reduced swing to lower power (e.g., reduced bit-line swing in memory)**

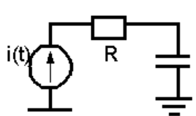
Adiabatic Charging

Charging a capacitor



$CV_{dd}^2/2$

Consider



$$v_c = \frac{1}{c}\cdot\int_0^T i\,dt = \frac{1}{c}\cdot I_{av}\cdot T \qquad I_{av} = \frac{C\cdot v_c}{T}$$

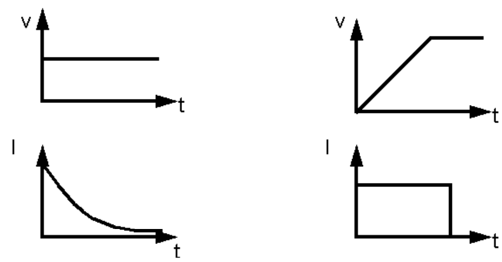
$$E_{dis} = R\cdot\int_0^T i^2(t)\,dt \ge R\cdot\int_0^T I_{av}^2\,dt = R\cdot I_{av}^2\cdot T = \frac{RC}{T}\cdot C\cdot V_c^2$$

Adiabatic Charging

$$V_I = RI + V_c = RC\frac{dv_c}{dt} + V_c$$

V_I = cst -> Exponential current

$I = I_{av}$ -> Linear ramp on V_I



wins if T > 2RC

$E_R = CV_c^2/2$

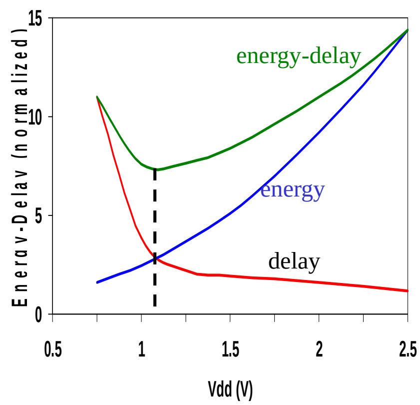
mimimal energy

$E_R = RC/T\ CV_c^2$

PDP and EDP

- Power-delay product (PDP) = $P_{av} * t_p = (C_L V_{DD}^2)/2$
  - PDP is the average energy consumed per switching event (Watts * sec = Joule)
  - lower power design could simply be a slower design

- Energy-delay product (EDP) = PDP * $t_p = P_{av} * t_p^2$
  - EDP is the average energy consumed multiplied by the computation time required
  - takes into account that one can trade increased delay for lower energy/operation (e.g., via supply voltage scaling that increases delay, but decreases energy consumption)



Lowering Dynamic Power

Capacitance:
Function of fan-out, wire length, transistor sizes

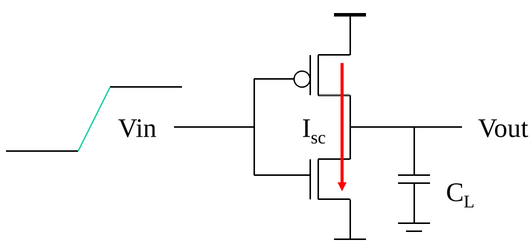
Supply Voltage:
Has been dropping with successive generations

$$P_{dyn} = C_L V_{DD}^2 P_{0\rightarrow 1} f$$

Activity factor:
How often, on average, do wires switch?

Clock frequency:
Increasing...

Short Circuit Power Consumption



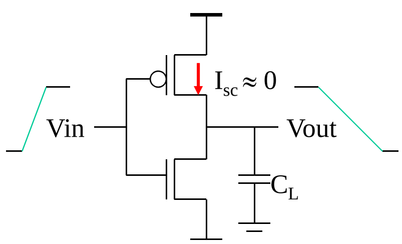
Finite slope of the input signal causes a direct current path between V_{DD} and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

Short Circuit Currents

$$P_{sc} = t_{sc} V_{DD} I_{peak} f$$

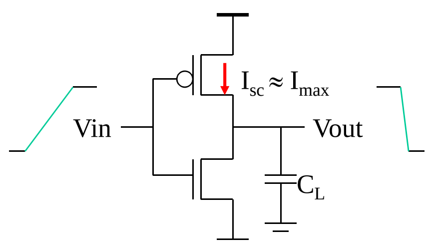
- Duration and slope of the input signal, t_{sc}
- I_{peak} determined by
  - the saturation current of the P and N transistors which depend on their sizes, process technology, temperature, etc.
  - strong function of the ratio between input and output slopes
    - a function of C_L

Impact of C_L on P_{sc}



Large capacitive load

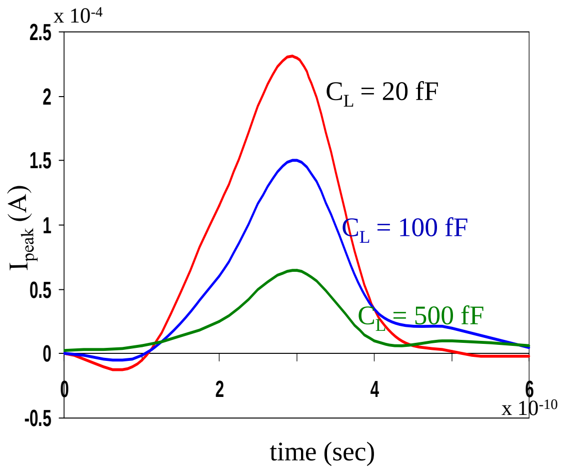
Output fall time significantly larger than input rise time.



Small capacitive load

Output fall time substantially smaller than the input rise time.

I_{peak} as a Function of C_L

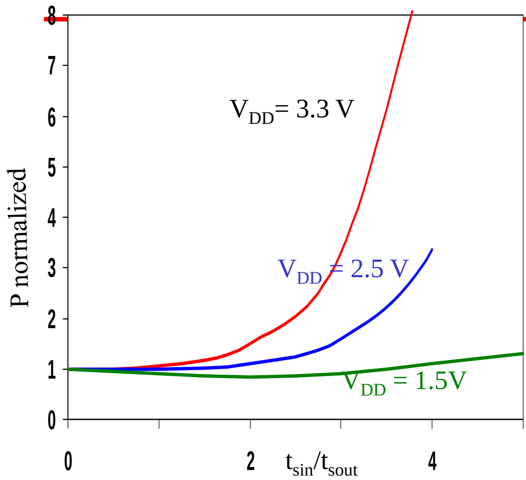


500 psec input slope

When load capacitance is small, I_{peak} is large.

Short circuit dissipation is minimized by matching the rise/fall times of the input and output signals - slope engineering.

P_{sc} as a Function of Rise/Fall Times



W/L_p = 1.125 μm/0.25 μm
W/L_n = 0.375 μm/0.25 μm
C_L = 30 fF

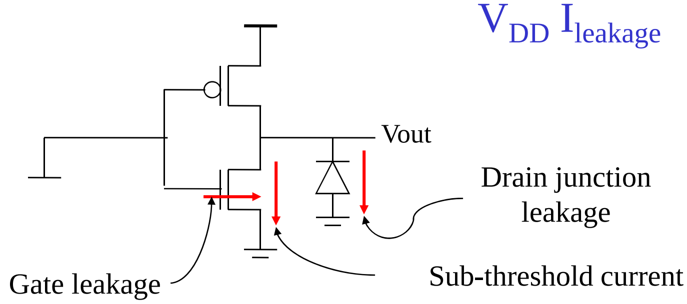
normalized wrt zero input rise-time dissipation

When load capacitance is small ($t_{sin}/t_{sout} > 2$ for $V_{DD} >$ 2V) the power is dominated by P_{sc}

If $V_{DD} < V_{Tn} + |V_{Tp}|$ then P_{sc} is eliminated since both devices are never on at the same time.

Leakage Power

$V_{DD}\ I_{leakage}$



Sub-threshold current is the dominant factor.

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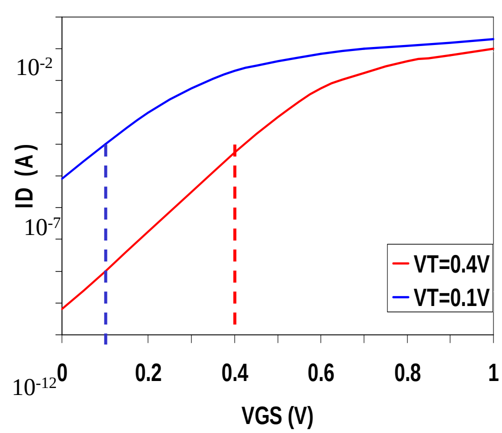
Leakage as a Function of V_T



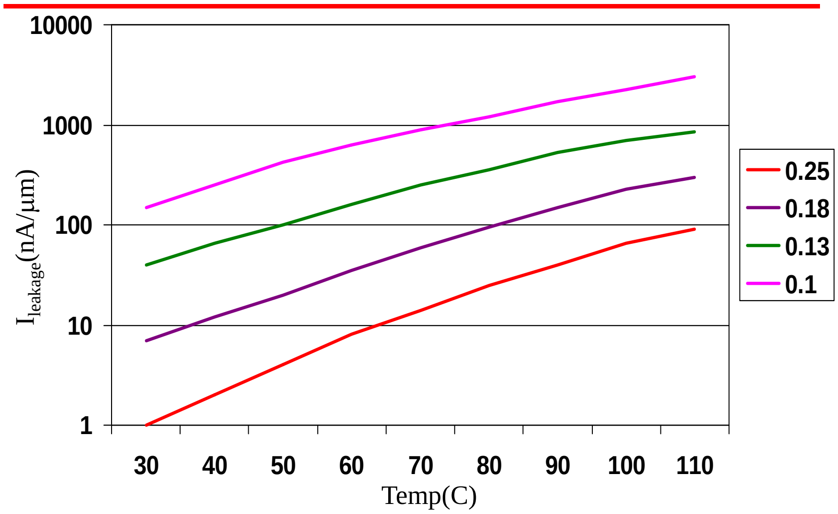
- An 90mV/decade V_T roll-off - so each 90mV increase in V_T gives 1 order of magnitude reduction in leakage (but adversely affects performance)

TSMC Processes Leakage and V_T

	CL018 G	CL018 LP	CL018 ULP	CL018 HS	CL015 HS	CL013 HS
V_{dd}	1.8 V	1.8 V	1.8 V	2 V	1.5 V	1.2 V
T_{ox} (effective)	42 Å	42 Å	42 Å	42 Å	29 Å	24 Å
L_{gate}	0.16 μm	0.16 μm	0.18 μm	0.13 μm	0.11 μm	0.08 μm
I_{DSat} (n/p) (μA/μm)	600/260	500/180	320/130	780/360	860/370	920/400
I_{off} (leakage) (pA/μm)	20	1.60	0.15	300	1,800	13,000
V_{Tn}	0.42 V	0.63 V	0.73 V	0.40 V	0.29 V	0.25 V
FET Perf. (GHz)	30	22	14	43	52	80

From MPR, 2000

Exponential Increase in Leakage Currents



From De,1999

Power and Energy Design Space

	Constant Throughput/Latency	Variable Throughput/Latency
Energy		
Leakage		

Summary

- Power and energy
  - Power (energy consumption per second) matters in package design, cooling, power rail design, and noise immunity etc.
  - Energy matters in battery-powered, portable devices
- Dynamic power
  - Due to switching – reduce VDD, lower capacitance, reduce switching probability
- Leakage power
  - Mainly due to subthreshold currents – increase V_T, sleep
- Short-circuit current
  - Both pull-up and pull-down are on at the same time – control input/output slopes, less important now at lower VDD