
EECS 427

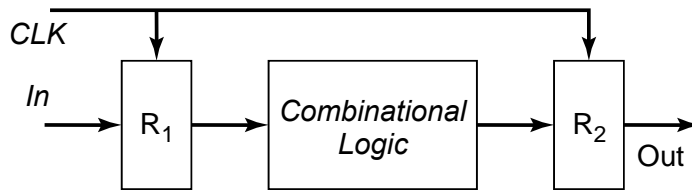
Lecture 14: Timing

Readings: 10.1-10.3

Reminders

- CAD assignments
 - Please submit CAD6 by tomorrow noon
 - CAD7 is due in a week
- Seminar by Prof. Bora Nikolic
 - SRAM variability in space and time
 - 11 am, Friday 11/6, 3427 EECS
- HW4 (detailed proposal) is due 11/16 – 1.5 weeks away
 - You should have completed your schematic design and simulation and started block layouts by then
- Quiz 2 on Monday 11/23 – 2.5 weeks away
 - Your chance to improve your performance in Quiz 1

Synchronous Timing

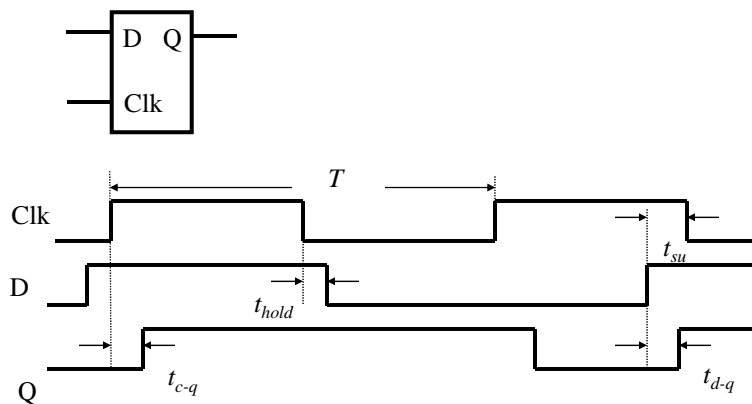


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Latch Parameters



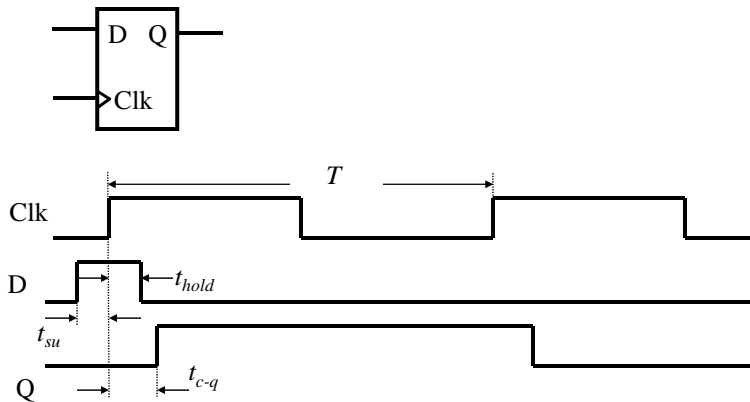
Delays can be different for rising and falling data transitions

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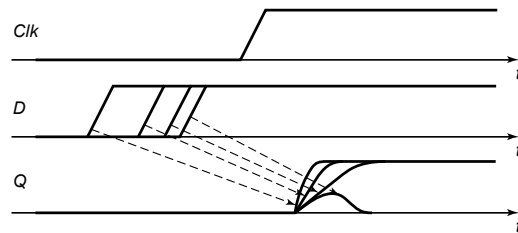
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Register (FF) Parameters



Delays can be different for rising and falling data transitions

More Precise Setup Time Definition



Setup time is a fairly vague concept

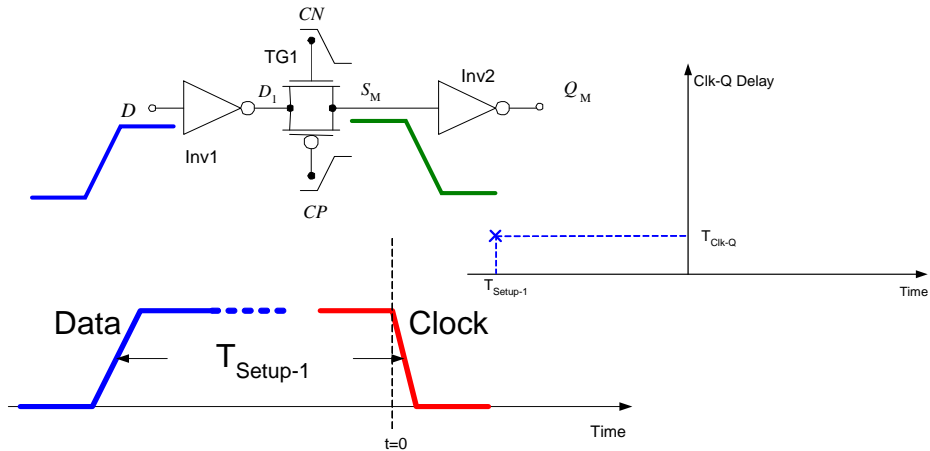
The correct data can be captured but the delay can be greatly affected

Where is the threshold?

Minimum D-Q delay is the fastest possible way to transfer input to output, related to the sum of T_{setup} and T_{clk-Q}

Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



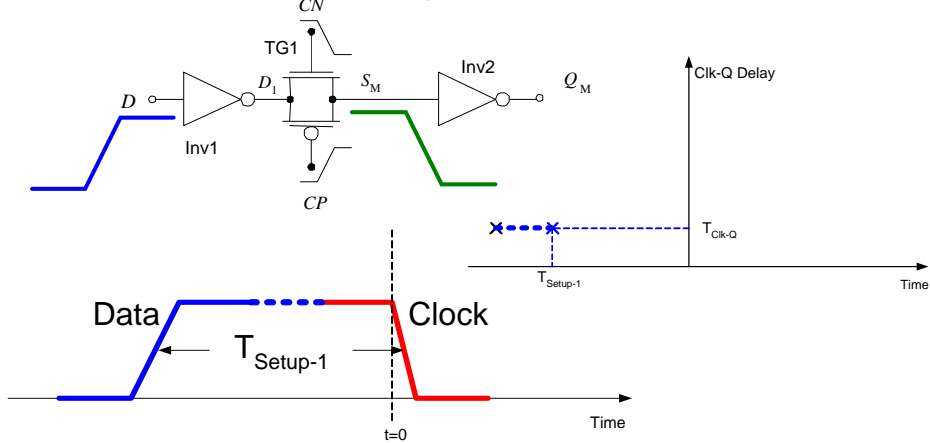
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Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



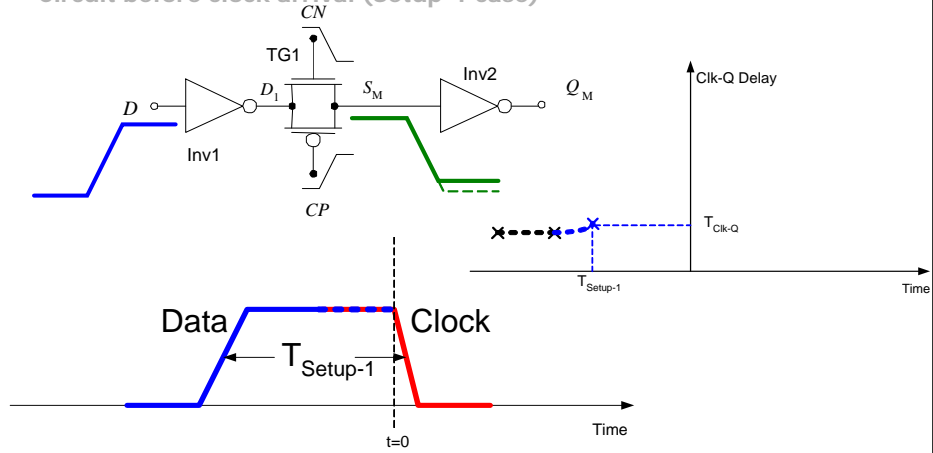
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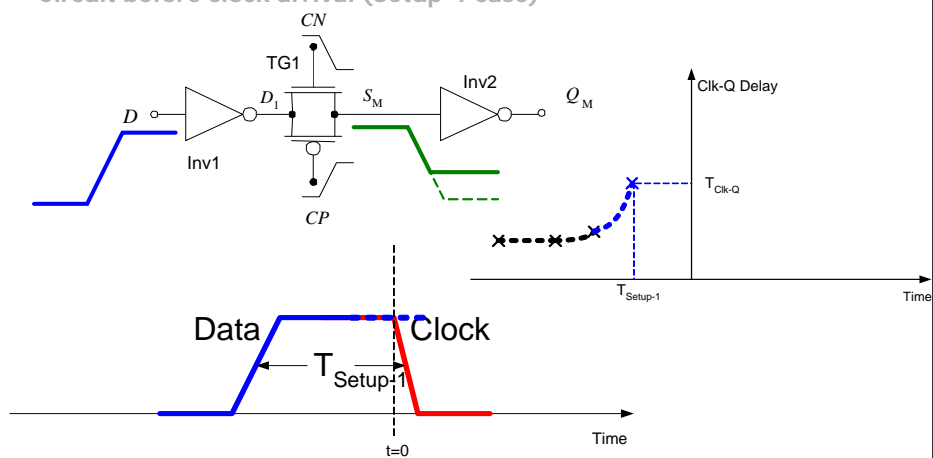
Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



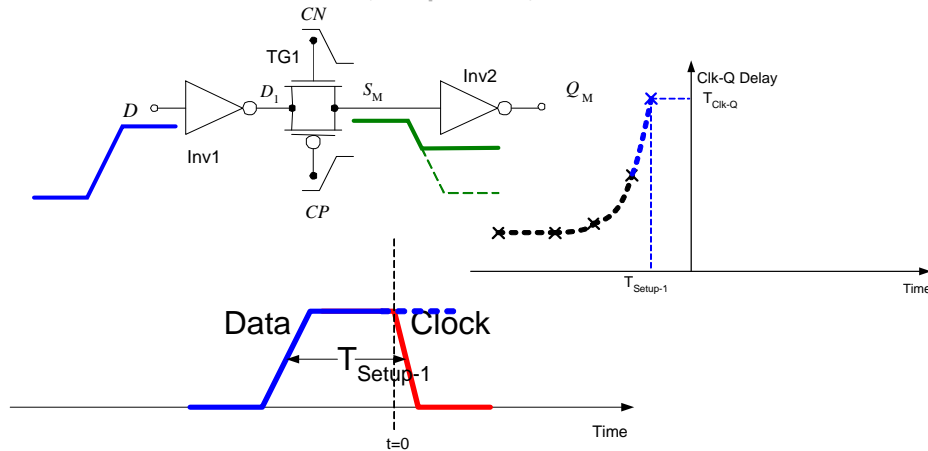
Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



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D-Q and setup time summary

- Define setup time as the point at which CLK-Q delay rises 5% beyond nominal
 - Nominal is measured when data arrives much earlier than CLK edge
 - This corresponds roughly to where the total D-Q delay is minimized

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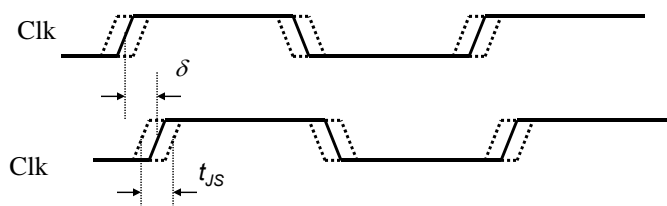
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Clock Waveform Nonidealities

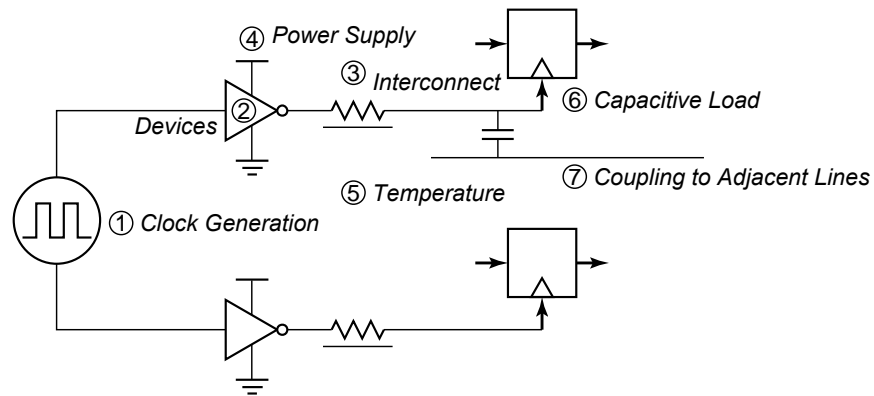
- **Clock skew**
 - Spatial variation in temporally equivalent clock edges, δ
- **Clock jitter**
 - Temporal variations in consecutive edges of the clock signal
 - Cycle-to-cycle (short-term) t_{JS}
 - Long term t_{JL}
- **Variation of the pulse width (duty cycle)**
 - Important for level sensitive (latch-based) clocking

Clock Skew and Jitter



- Both skew and jitter impact the effective cycle time

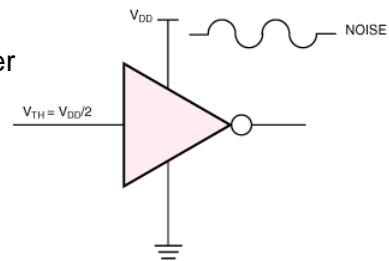
Clock Uncertainties



Sources of clock uncertainty

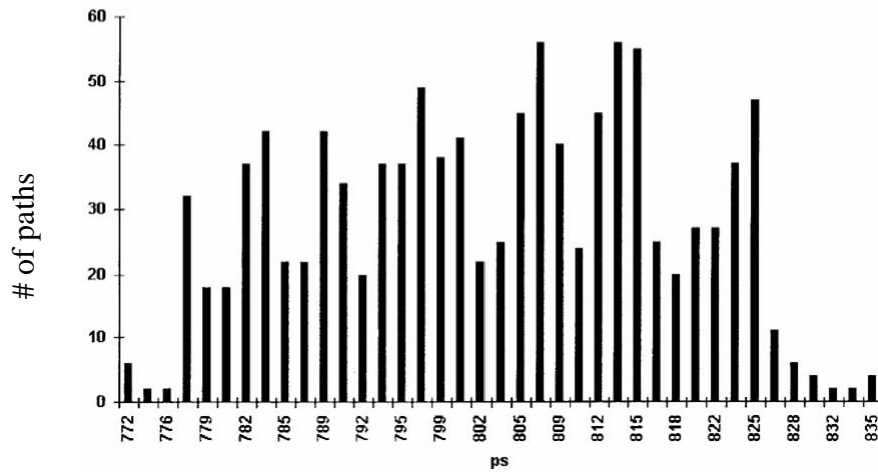
Jitter Sources

- Caused by variations in clock period that result from:
 - Phased-lock loop (PLL) oscillation frequency
 - Various noise sources affecting clock generation and distribution
 - Ex. Power supply noise which dynamically alters the drive strength of intermediate buffer stages



Cypress Semi

IBM microprocessor clock skew

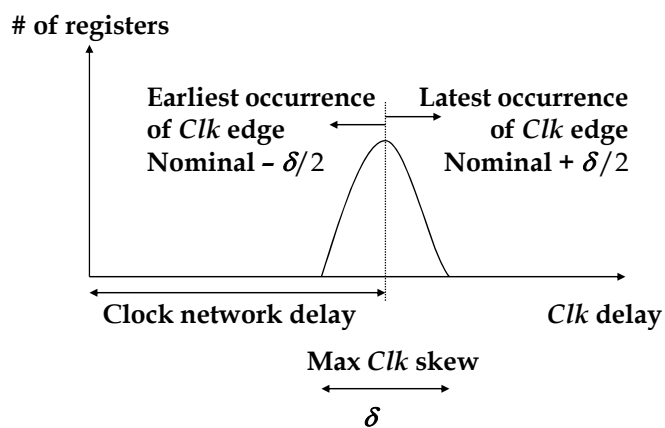


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Idealized View of Clock Skew

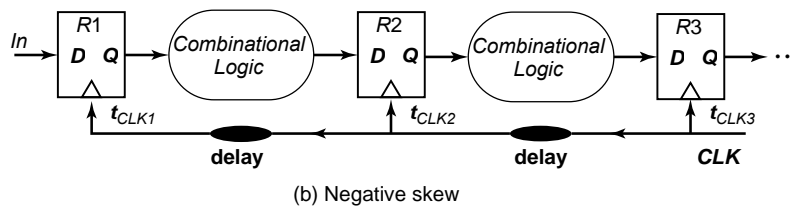
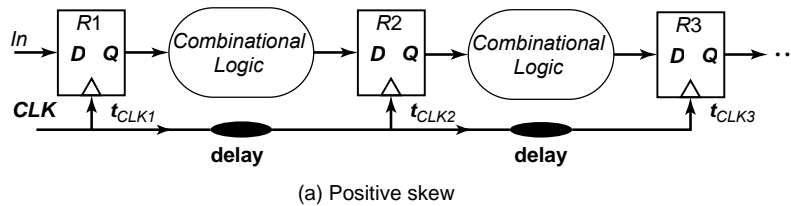


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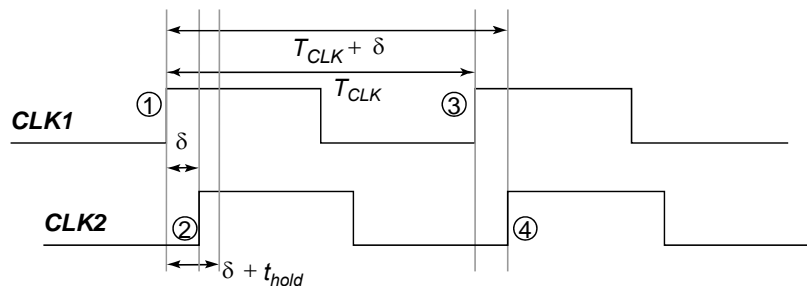
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Positive and Negative Skew



Positive Skew, $\delta > 0$

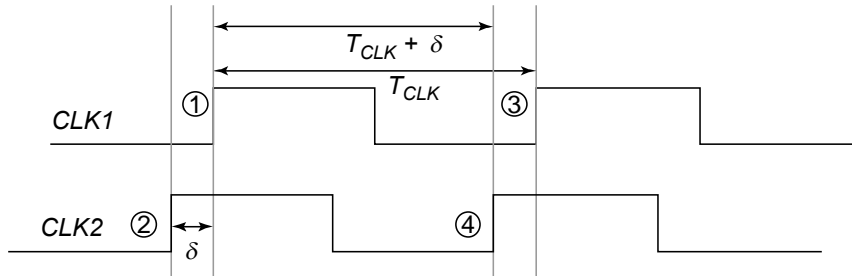


Launching edge arrives before the receiving edge

Good for performance, bad for hold time

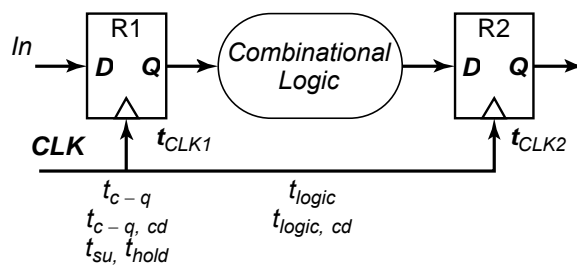
Key: Hold time violations cannot be fixed by running the clock slower!

Negative Skew, $\delta < 0$



Receiving edge arrives before the launching edge
Bad for performance, good for hold time violations

Timing Constraints

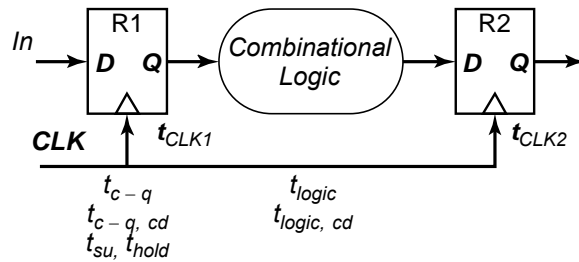


Minimum cycle time:

$$T \geq t_{c-q} + t_{su} + t_{logic} - \delta$$

Worst case is when receiving edge arrives early (negative δ)

Timing Constraints



Hold time constraint:

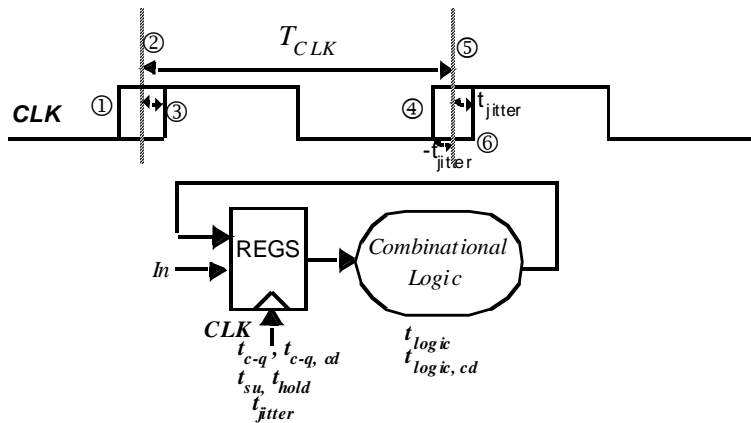
$$t_{(c-q, cd)} + t_{(logic, cd)} > t_{hold} + \delta$$

Worst case is when receiving edge arrives late (positive skew)

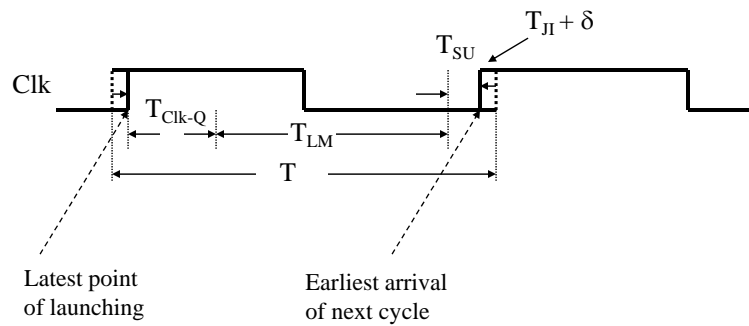
Race between data and clock

cd: contamination delay (fastest possible delay)

Impact of Jitter



Longest Logic Path



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Clock Constraints

If launching edge is late and receiving edge is early, the data will not be too late if:

$$T_{\text{c-q}} + T_{\text{LM}} + T_{\text{SU}} < T - T_{\text{JI},1} - T_{\text{JI},2} - \delta$$

Minimum cycle time is determined by the maximum delays through the logic

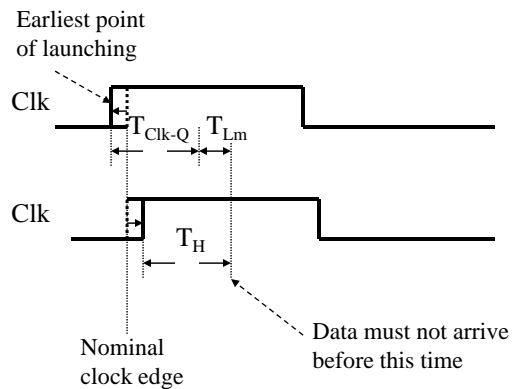
$$T_{\text{c-q}} + T_{\text{LM}} + T_{\text{SU}} + \delta + 2 T_{\text{JI}} < T$$

Skew can be either positive or negative

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Shortest Path



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Clock Constraints

If launching edge is early and receiving edge is late:

$$T_{\text{c-q}} + T_{\text{LM}} - T_{\text{JI},1} < T_{\text{H}} + T_{\text{JI},2} + \delta$$

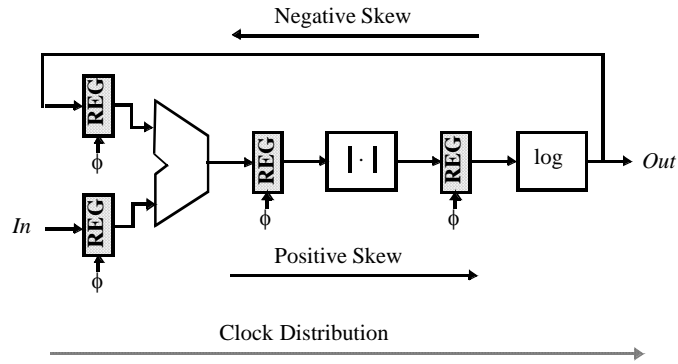
Minimum logic delay

$$T_{\text{c-q}} + T_{\text{LM}} < T_{\text{H}} + 2T_{\text{JI}} + \delta$$

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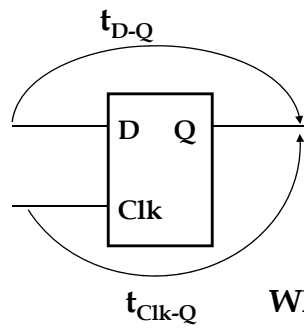
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How to counter Clock Skew?



Data and Clock Routing

Latch timing



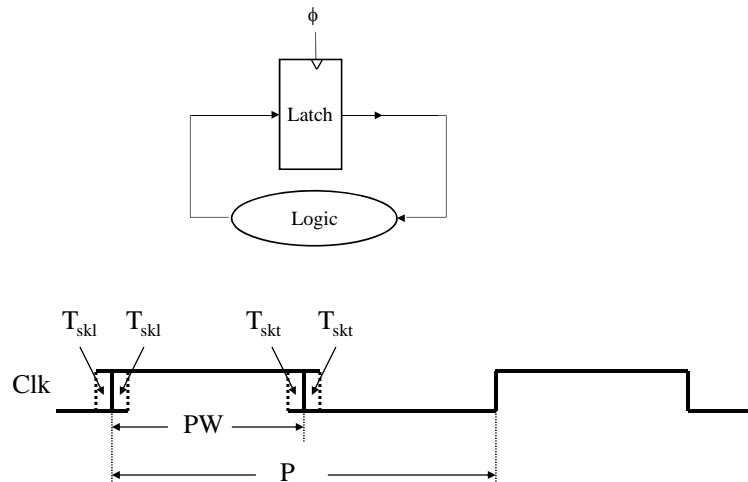
When data arrives to transparent latch

Latch is a 'soft' barrier

When data arrives to closed latch

Data has to be 're-launched'

Single-Phase Clock with Latches



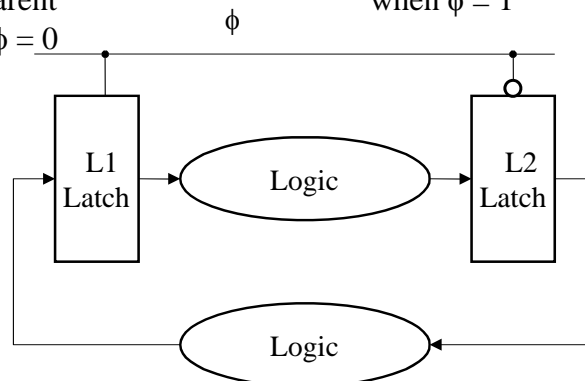
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Latch-Based Design

L1 latch is transparent when $\phi = 0$

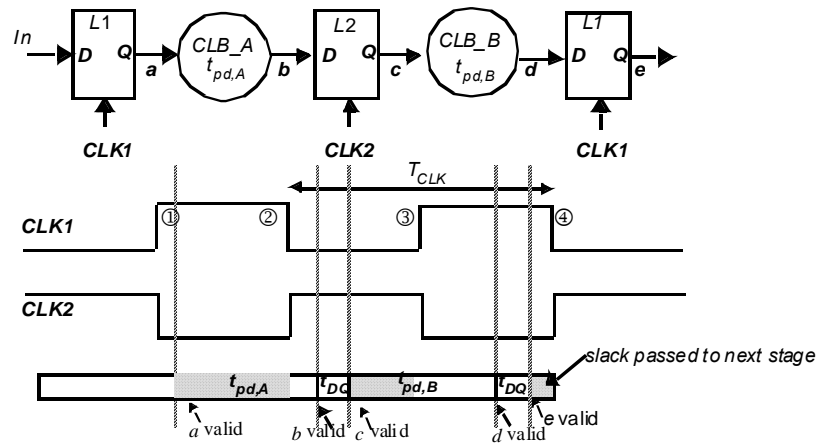
L2 latch is transparent when $\phi = 1$



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Slack-borrowing



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Conclusions

- Clocks strongly impact IC performance (timing) and are not ideal
 - Skew and jitter are commonly discussed non-idealities
 - Skew is typically larger and more heavily focused on
 - More on skew later in class when we discuss clock distribution techniques
- Rough rule of thumb: skew should be kept $< 10\%$ of clock period
- Sequential elements eat up a significant amount of total timing budget + power resources
 - They are therefore extremely important to design carefully
 - Robustness is critical as well

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