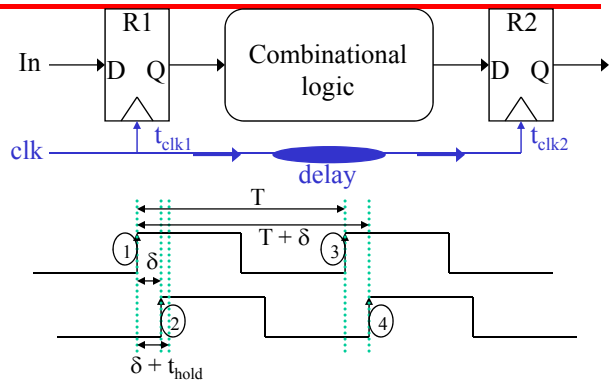
EECS 427
Lecture 15: Timing, Latches, and Registers
Reading: Chapter 7

Reminders

- CAD assignments
  - CAD7 is due Thursday at noon
- ECE Graduate Symposium
  - Poster session in ECE Atrium on Friday
- HW4 (detailed proposal) is due Tuesday 11/17 (one day extension)
  - You should have completed your schematic design and simulation and started block layouts by then
  - Send your proposal (in Word or LaTeX) by email to the Zhengya, cutoff time: 11:59 pm on 11/17
- Quiz 2 on Monday 11/23?
  - Your chance to improve your performance in Quiz 1
  - The other option: review session (problem solving, Q&A) on Monday 11/23 in class, Quiz 2 on Tuesday 11/24 5:40 pm – 7:00 pm during the discussion slot

Positive Clock Skew

- Clock and data flow in the same direction



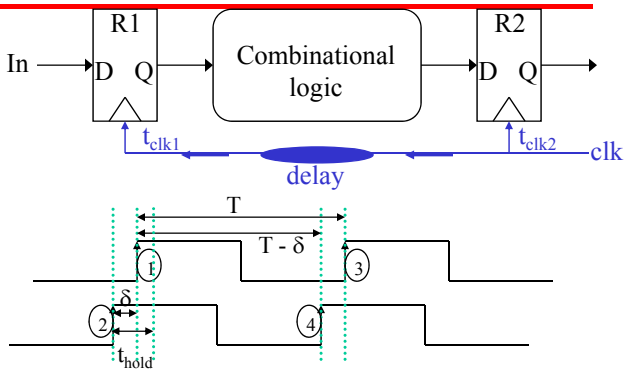
T : $T + \delta \geq t_{cq,max} + t_{logic,max} + t_{su}$ so $T \geq t_{cq,max} + t_{logic,max} + t_{su} - \delta$

t_{hold} : $t_{hold} + \delta \leq t_{logic,min} + t_{cq,min}$ so $t_{hold} \leq t_{logic,min} + t_{cq,min} - \delta$

- Positive skew: Improves performance, but makes t_{hold} harder to meet. If t_{hold} is not met (race conditions), the circuit malfunctions independent of the clock period!

Negative Clock Skew

- Clock and data flow in opposite directions



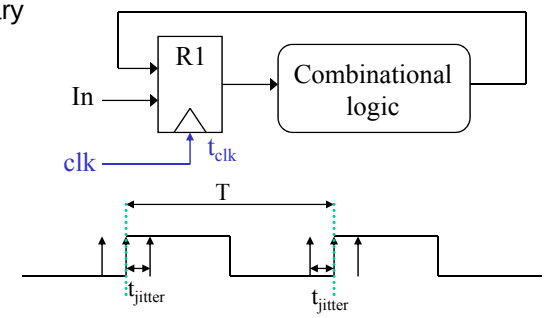
T : $T - \delta \geq t_{cq,max} + t_{logic,max} + t_{su}$ so $T \geq t_{cq,max} + t_{logic,max} + t_{su} + \delta$

t_{hold} : $t_{hold} - \delta \leq t_{logic,min} + t_{cq,min}$ so $t_{hold} \leq t_{logic,min} + t_{cq,min} + \delta$

- Negative skew: Degrades performance, but t_{hold} is easier to meet (eliminating race conditions)

Clock Jitter

- Jitter causes T to vary on a cycle-by-cycle basis



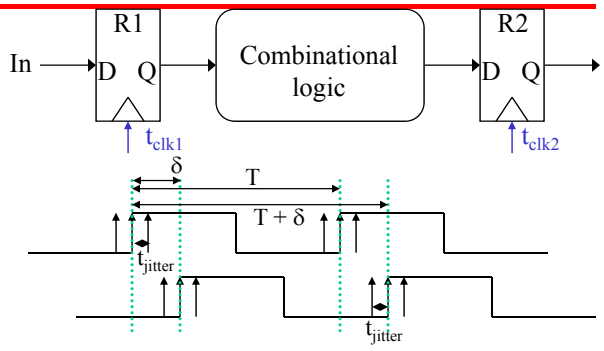
T : $T - 2t_{jitter} \geq t_{cq,max} + t_{logic,max} + t_{su}$ so $T \geq t_{cq,max} + t_{logic,max} + t_{su} + 2t_{jitter}$

t_{hold}: $t_{hold} + 2t_{jitter} \leq t_{logic,min} + t_{cq,min}$ so $t_{hold} \leq t_{logic,min} + t_{cq,min} - 2t_{jitter}$

- Jitter directly reduces the performance of a sequential circuit
- Jitter makes race condition worse

Combined Impact of Skew and Jitter

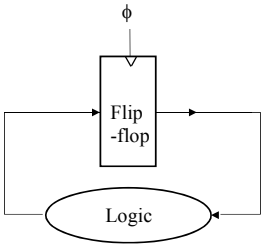
- Constraints on the minimum clock period ($\delta > 0$)

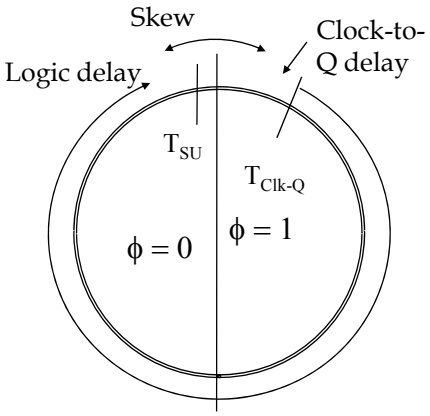


$T \geq t_{cq,max} + t_{logic,max} + t_{su} - \delta + 2t_{jitter}$ $t_{hold} \leq t_{logic,min} + t_{cq,min} - \delta - 2t_{jitter}$

- Positive skew with jitter: Degrades performance, and makes t_{hold} even *harder* to meet. (The acceptable skew is reduced by jitter.)

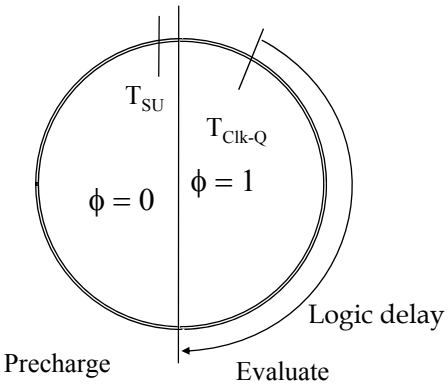
Register–Based Timing

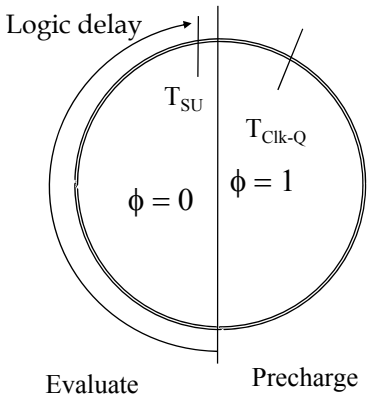




Representation after
M. Horowitz, VLSI Circuits 1996.

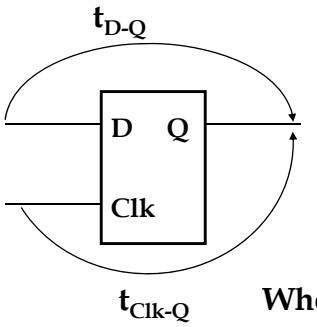
Registers and Dynamic Logic





Registers are used only with static logic

Latch timing



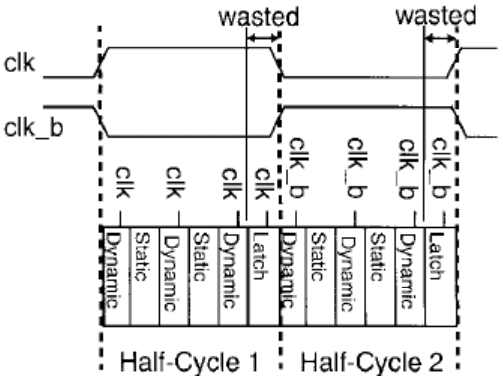
When data arrives to transparent latch

Latch is a 'soft' barrier

When data arrives to closed latch

Data has to be 're-launched'

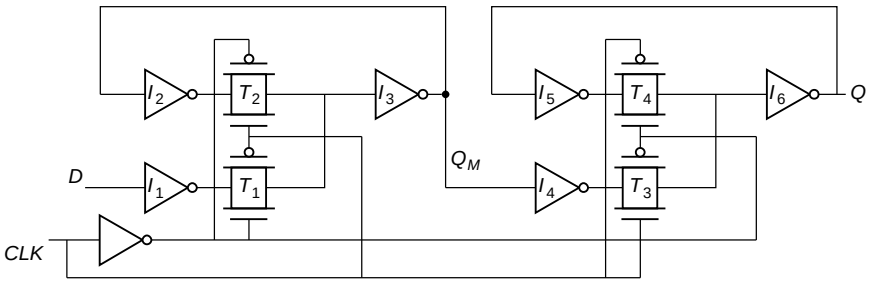
Domino Logic with Latch Timing



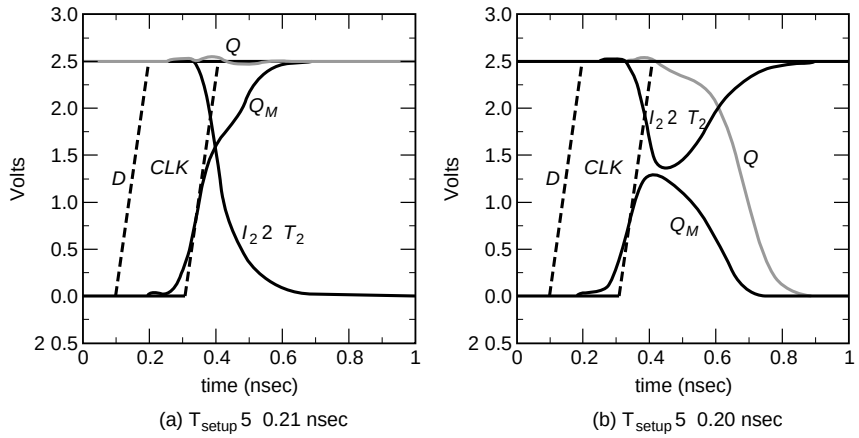
Harris, JSSC97

Master-Slave Register

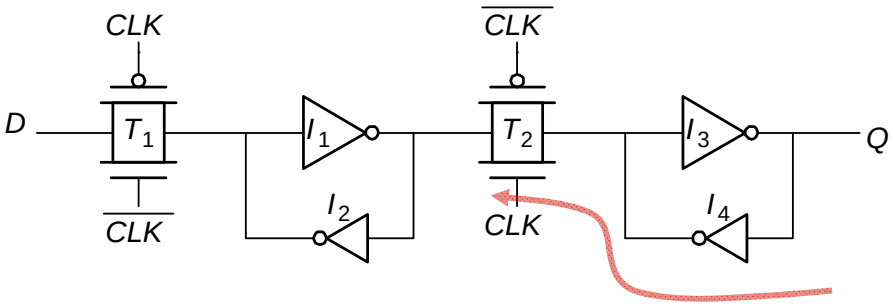
Multiplexer-based latch pair



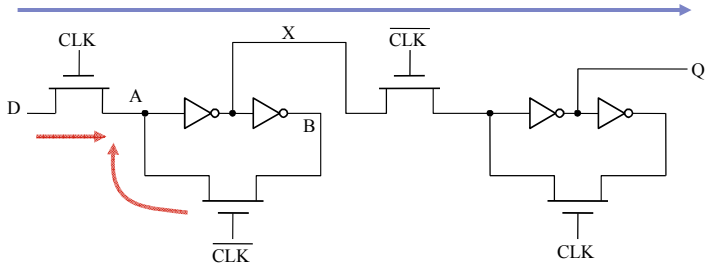
Setup Time



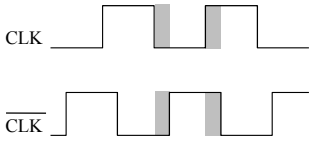
Reduced Clock Load



Avoiding Clock Overlap



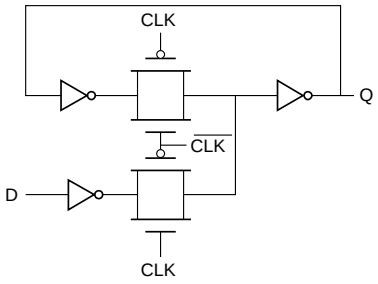
(a) Schematic diagram



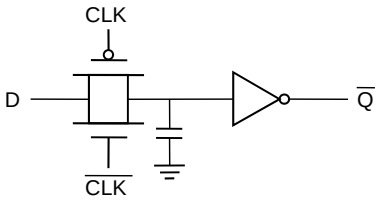
(b) Overlapping clock pairs

Dynamic Latch

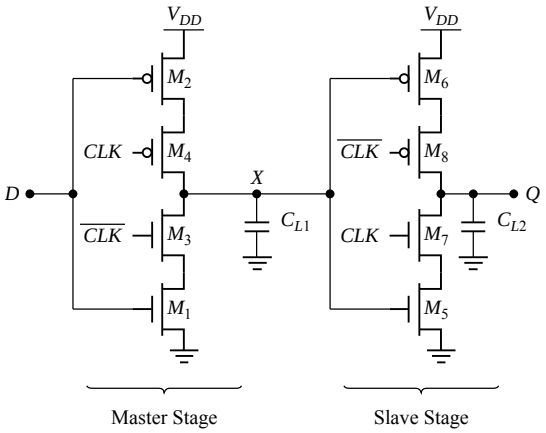
Static



Dynamic (charge-based)

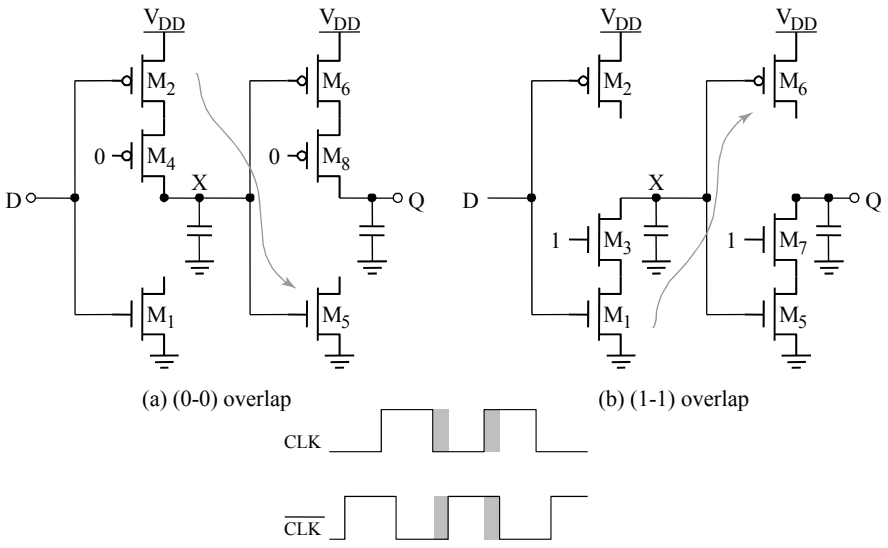


C²MOS

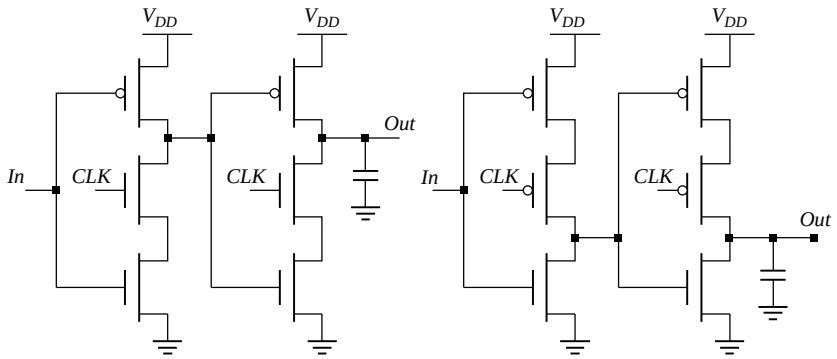


"Keepers" can be added to make circuit pseudo-static

Insensitive to Clock-Overlap



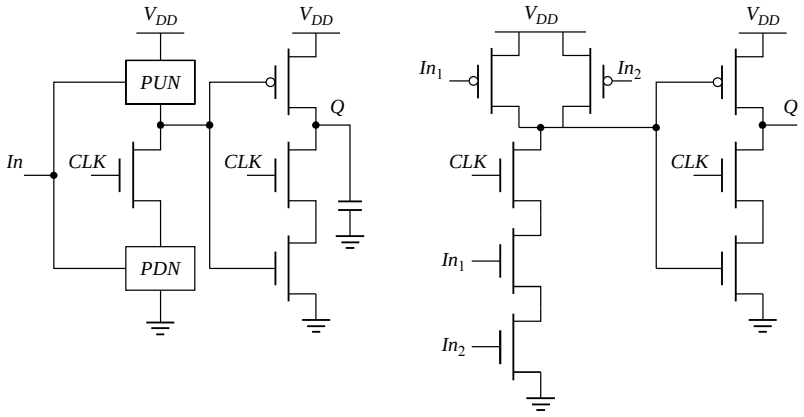
TSPC



Positive latch (transparent when CLK= 1)

Negative latch (transparent when CLK= 0)

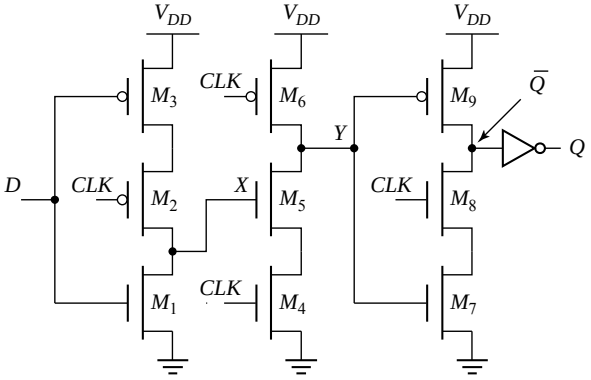
Including Logic in TSPC



Example: logic inside the latch

AND latch

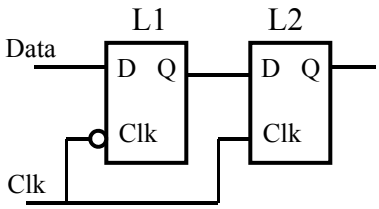
TSPC Register



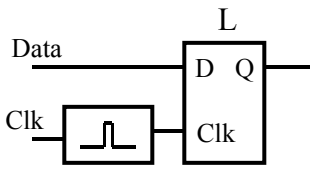
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:

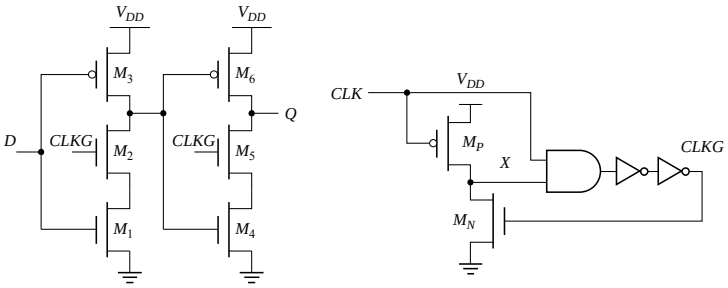
Master-Slave Latches



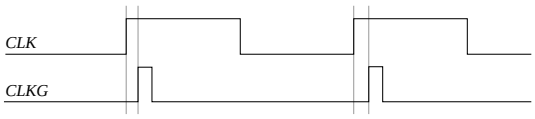
Pulse-Triggered Latch



Pulsed Latches



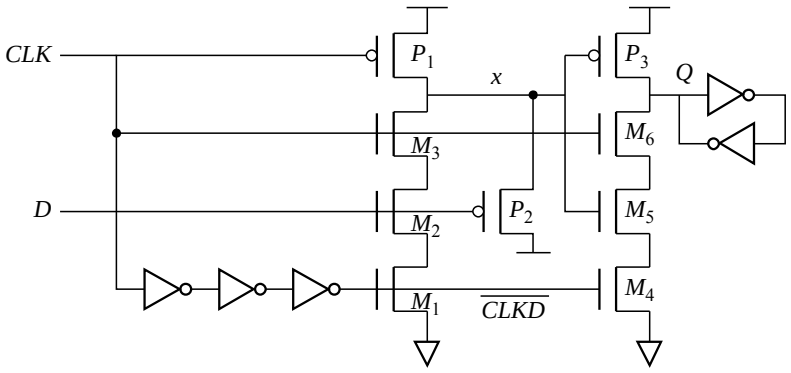
(a) register *(b) glitch generation*



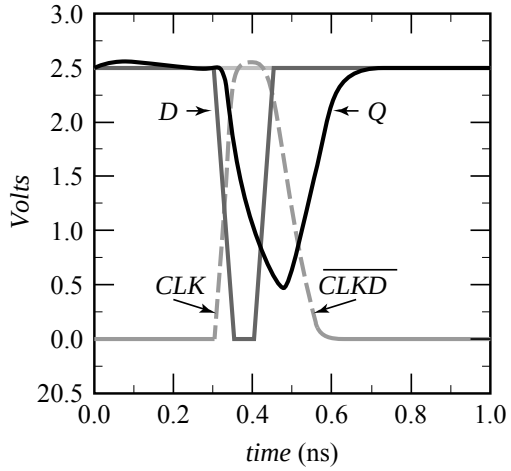
(c) glitch clock

Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :



Hybrid Latch-FF Timing



Latch-Based Pipeline