EECS 427
Lecture 17: Memory Reliability and Power

Readings: 12.4,12.5

Reminders

- Deadlines
  - HW4 is due Tuesday 11/17 at 11:59 pm (email submission)
  - CAD8 is due Saturday 11/21 at 11:59 pm
- Quiz 2 is on Wednesday 11/25
  - Extended office hours this week
    - Monday: 3–3:30 pm and after 5 pm
    - Wednesday office hour is cancelled
    - Sunday: noon–6 pm
  - Half-lecture review in class on Monday 11/23
  - Extended office hours next week
    - Monday 3–3:30 pm and after 5 pm
    - Tuesday 3–6 pm
- What is remaining after Quiz 2
  - 2.5 weeks to finish your project by 12/14

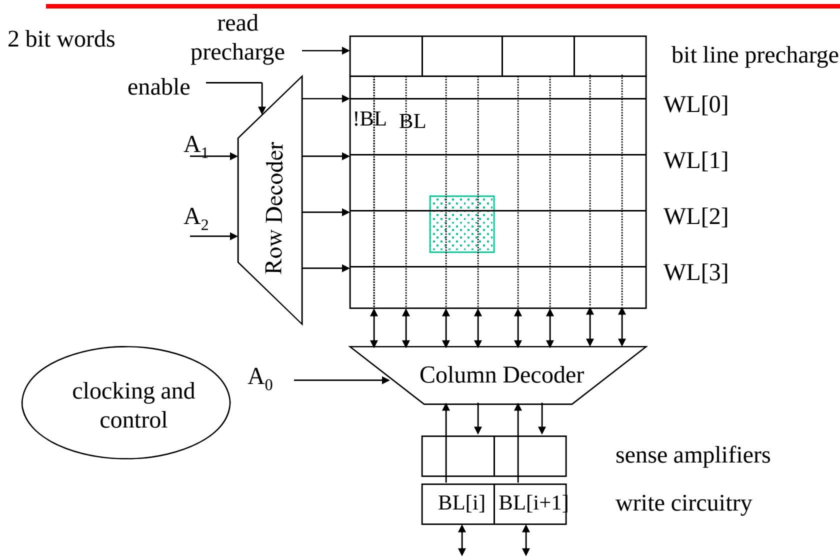
Last Time

- SRAM
  - – Configuration – row address decoding and column decoding
  - – Sizing for read and write – avoid read upset and ensure writability
  - – Address decoding – predecoding + final decoding

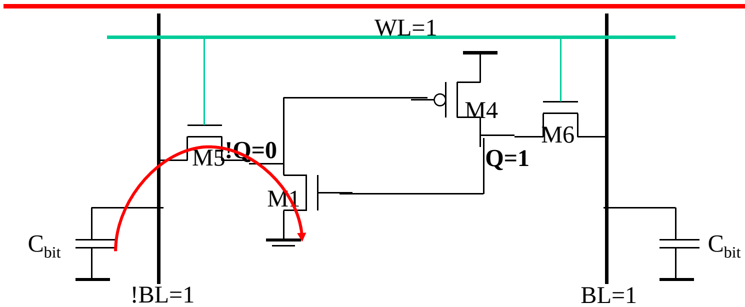
Outline

- SRAM review
- SRAM sense amplifiers
- DRAM overview (3T and 1T)
- Memory reliability and yield
- Memory power reduction

4x4 SRAM Memory

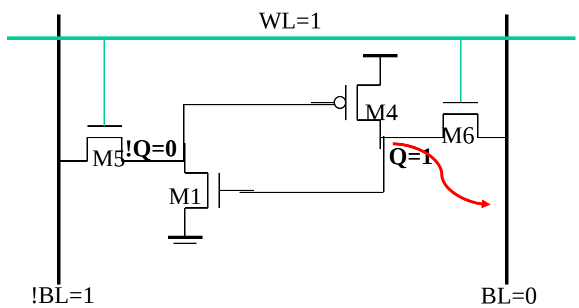


SRAM Cell Analysis (Read)



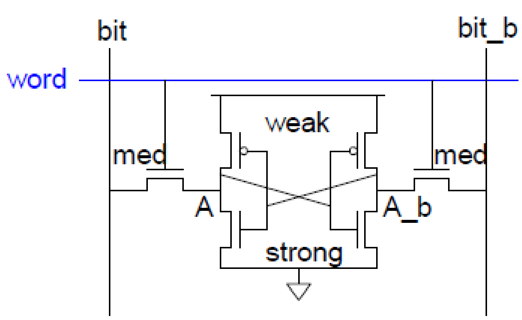
Cell Ratio (CR) = $(W_{M1}/L_{M1})/(W_{M5}/L_{M5})$

SRAM Cell Analysis (Write)



Pullup Ratio (PR) = $(W_{M4}/L_{M4})/(W_{M6}/L_{M6})$

Cell Sizing



Row Decoders

Collection of 2^M complex logic gates
Organized in regular and dense fashion

(N)AND Decoder

$$WL_0 = A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

$$WL_{511} = \bar{A}_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

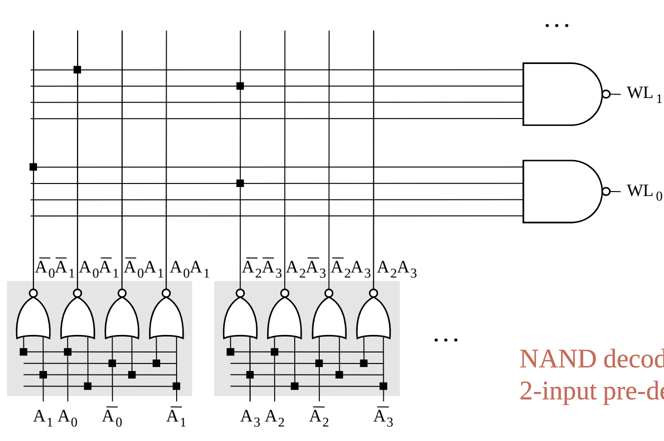
NOR Decoder

$$WL_0 = \overline{A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8 + A_9}$$

$$WL_{511} = \overline{A_0 + \bar{A}_1 + \bar{A}_2 + \bar{A}_3 + \bar{A}_4 + \bar{A}_5 + \bar{A}_6 + \bar{A}_7 + \bar{A}_8 + \bar{A}_9}$$

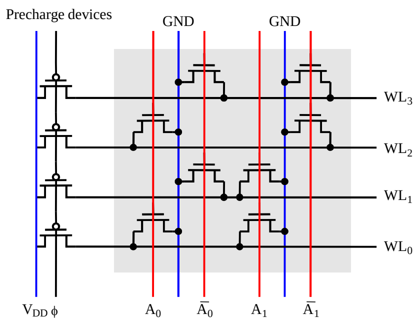
Hierarchical Decoders

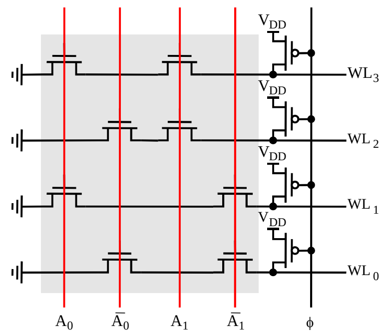
Multi-stage implementation improves performance



NAND decoder using
2-input pre-decoders

Dynamic Decoders





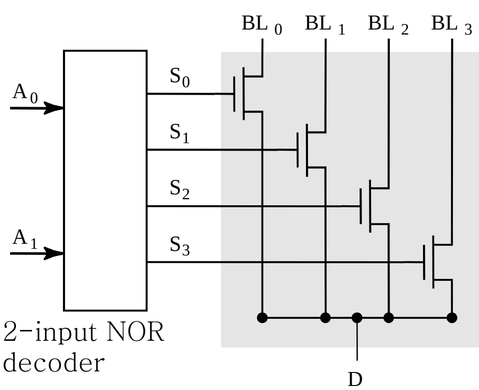
2-input NOR decoder

Active high
All WL's except one is pulled down

2-input NAND decoder

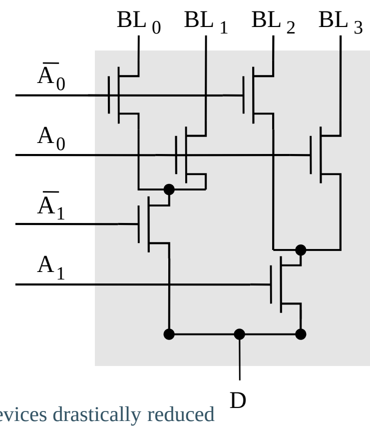
Active low
Only one WL is pulled down

Pass-transistor based column decoder



Advantages: speed (t_{pd} does not add to overall memory access time)
Only one extra transistor in signal path
Disadvantage: Large transistor count

Tree based column decoder



Number of devices drastically reduced
Delay increases quadratically with # of sections; prohibitive for large decoders
Solutions: buffers
progressive sizing
combination of tree and pass transistor approaches

Sense Amplifiers

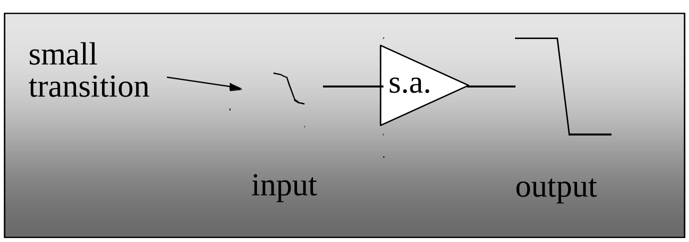
$$t_p = \frac{C \times \Delta V}{I_{av}}$$

make ΔV as small as possible

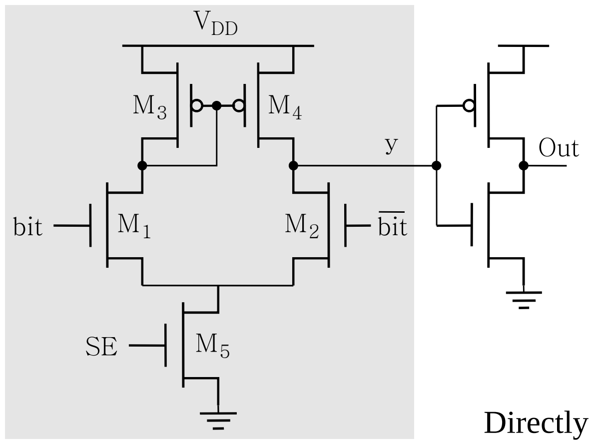
large

small

Idea: Use Sense Amplifer

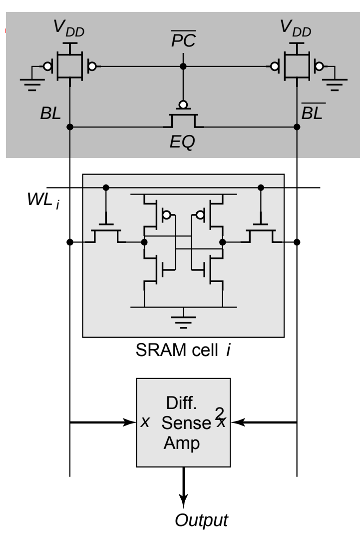


Differential Sense Amplifier

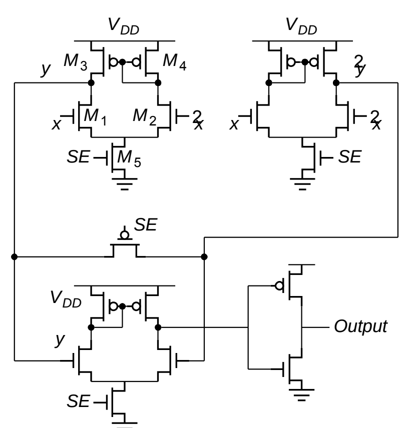


Directly applicable to SRAMs

Differential Sensing — SRAM

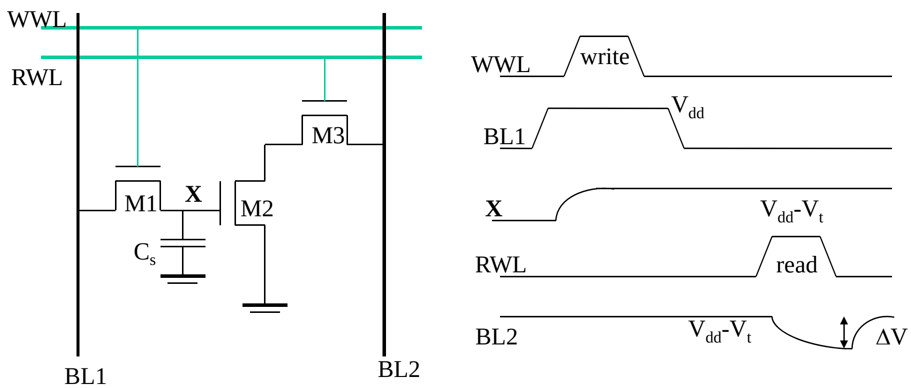


(a) SRAM sensing scheme



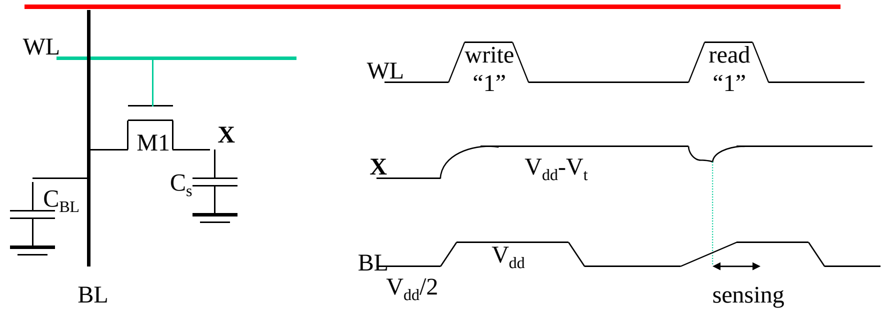
(b) two stage differential amplifier

3-Transistor DRAM Cell



No constraints on device sizes (ratioless)
Reads are non-destructive
Value stored at node X when writing a "1" is V_{WWL} - V_{tn}

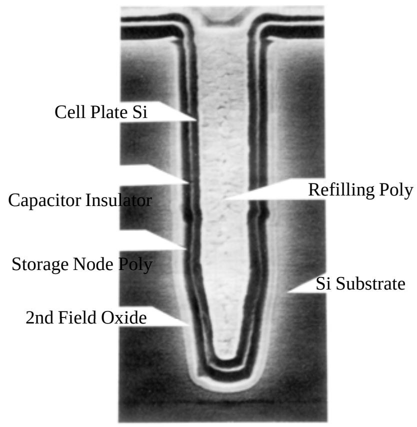
1-Transistor DRAM Cell



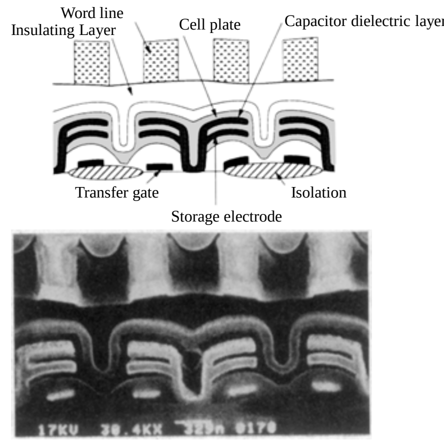
Write: C_s is charged (or discharged) by asserting WL and BL
Read: Charge redistribution occurs between C_{BL} and C_s

Read is destructive, so must refresh after read

Advanced 1T DRAM Cells



Trench Cell



Stacked-capacitor Cell

DRAM Cell Observations

- DRAM memory cells are single ended (complicates the design of the sense amp)
- 1T cell requires a sense amp for each bit line due to charge redistribution read
- 1T cell read is destructive; refresh must follow to restore data
- 1T cell requires an extra capacitor that must be explicitly included in the design
- A threshold voltage is lost when writing a 1 (can be circumvented by bootstrapping the word lines to a higher value than V_{dd})

Reliability and Yield

- Semiconductor memories trade off noise-margin for density and performance

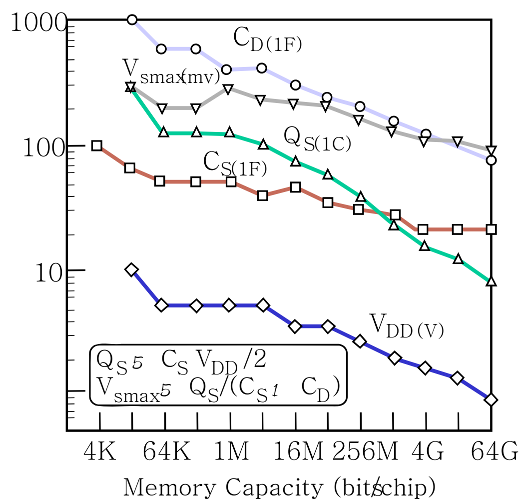
Highly Sensitive to Noise (Crosstalk, Supply Noise)

- High Density and Large Die size cause Yield Problems

$$Y = 100\frac{Number\ of\ Good\ Chips\ on\ Wafer}{Number\ of\ Chips\ on\ Wafer}$$

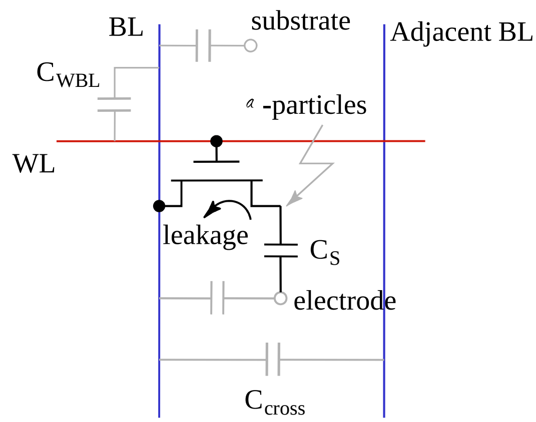
Increase Yield using Error Correction and Redundancy

Sensing Parameters in DRAM

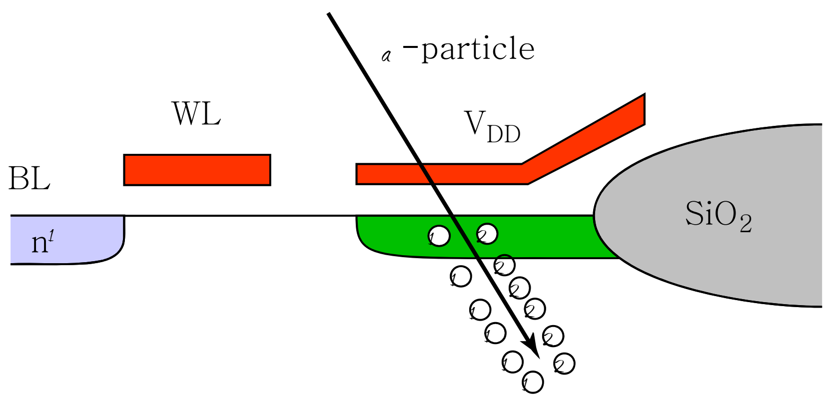


From [Itoh01]

Noise Sources in 1T DRAM

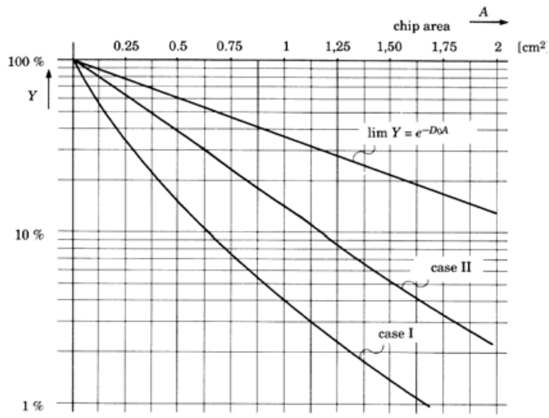


Alpha-particles (or Neutrons)



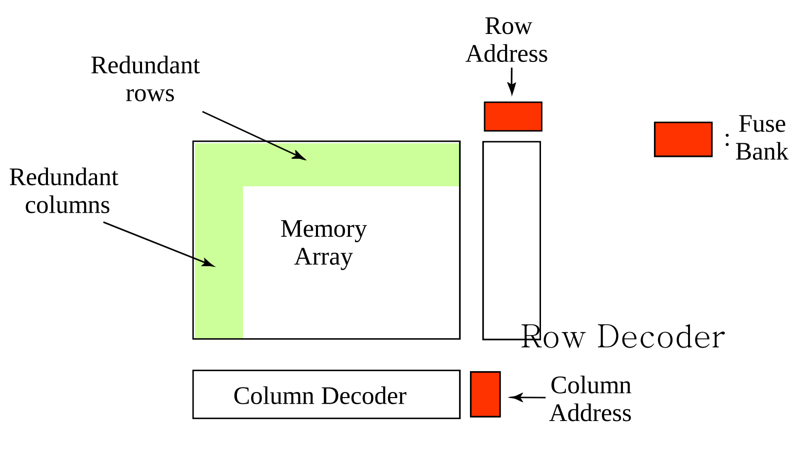
1 Particle ~ 1 Million Carriers

Yield



Yield curves at different stages of process maturity (from [Veendrick92])

Redundancy



Error-Correcting Codes

Example: Hamming Codes

$$P_1 P_2 B_3 P_4 B_5 B_6 B_7$$

with

$$P_1 \oplus B_3 \oplus B_5 \oplus B_7 = 0$$

$$P_2 \oplus B_3 \oplus B_6 \oplus B_7 = 0$$

$$P_4 \oplus B_5 \oplus B_6 \oplus B_7 = 0$$

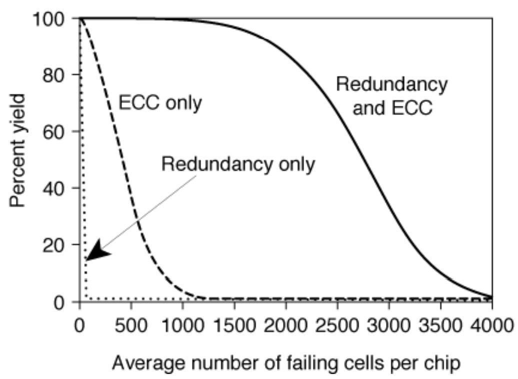
e.g. B3 Wrong

1

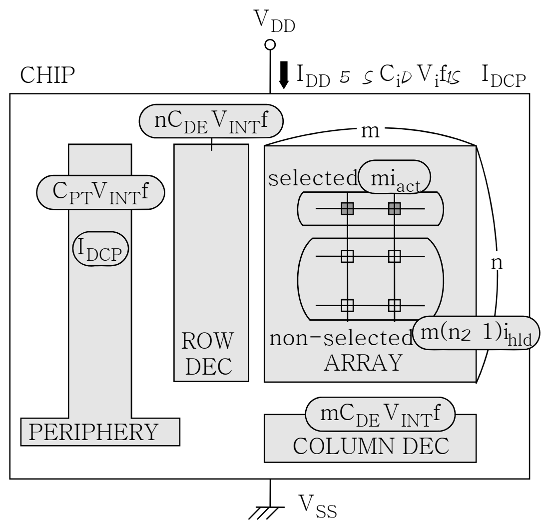
1 = 3

0

Redundancy and Error Correction

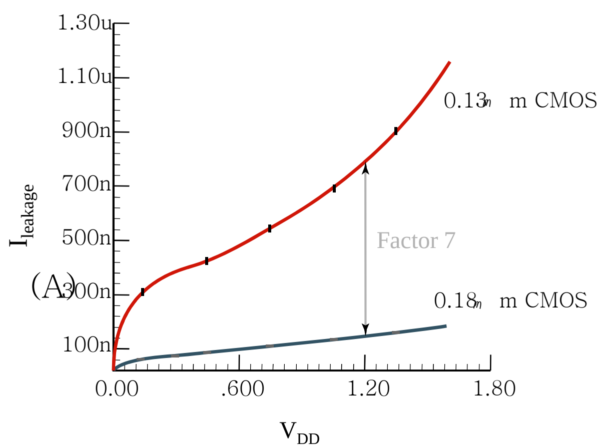


Power Dissipation in Memories



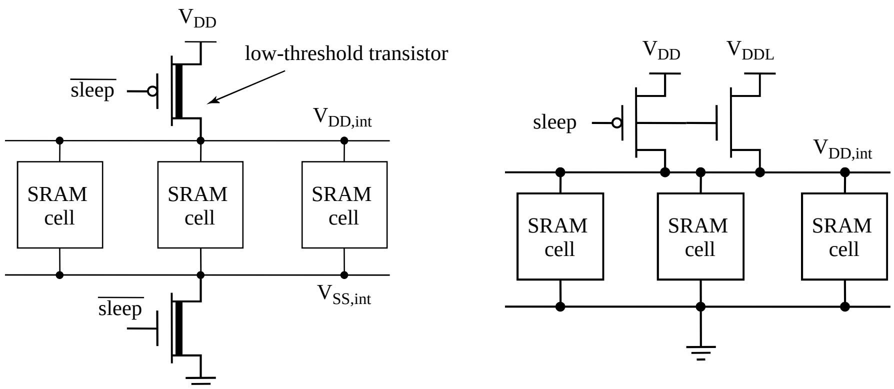
From [Itoh00]

Data Retention in SRAM



SRAM leakage increases with technology scaling

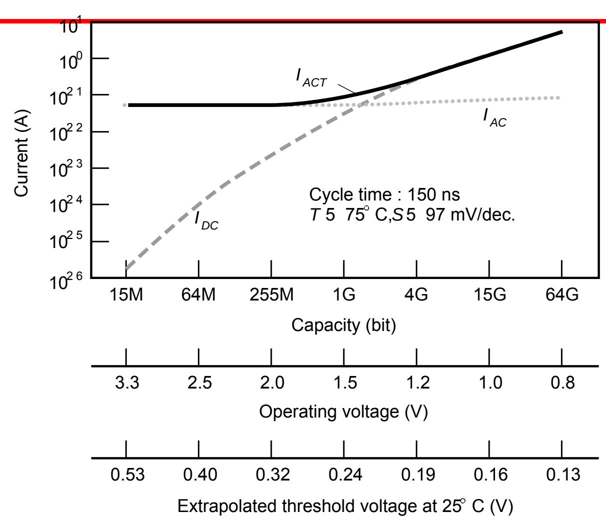
Suppressing Leakage in SRAM



Inserting Extra Resistance

Reducing the supply voltage

Data Retention in DRAM



From [Itoh00]